METHODOLOGY FOR OPTIMIZING PHASE-SHIFTED FULL-BRIDGE CONVERTERS
EMPLOYING WIDE BAND-GAP SEMICONDUCTORS

by

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ABSTRACT

Switching loss is a major factor in determining the performance of modern power electronics converters. Soft-switching-based converters are, consequently, developed to mitigate this loss mechanism. The phase-shifted full-bridge (PSFB) converter is such a converter that is appealing in many high-power applications, such as datacenters. Understanding the underlying principles of the zero-voltage switching (ZVS) mechanism within this converter and fine-tuning the corresponding system parameters are necessary to achieve higher efficiency and power density. Despite the importance of this subject, there is a lack of broad studies that investigate the interdependence effects of system parameters on ZVS realization and modeling the ZVS transitions accordingly. This dissertation identifies the switching deadtime values as parameters of particular sensitivity for this topology. Subtle changes to the switching deadtime values can result in dramatic changes to the overall system efficiency, especially for certain combinations of other system parameters. This dissertation provides a set of empirically validated analytical tools that provide new insight into the interdependence of these parameters and offer useful guidance to practitioners seeking to maximize the performance of this topology, especially for implementations that utilize Wide Band-Gap (WBG) semiconductors in their structure. A set of practical guidelines is also provided to assist with fine-tuning this topology for maximum performance. Moreover, these sets of analytical tools are employed in this dissertation to design and implement a 10-kW, SiC-based, synchronous-rectified PSFB converter, which is optimized for efficiency and power density.
DEDICATION

To My Parents
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
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<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
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<tr>
<td>CCM</td>
<td>Continuous-Conduction-Mode</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
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<tr>
<td>DCM</td>
<td>Discontinuous-Conduction-Mode</td>
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<tr>
<td>FEA</td>
<td>Finite Element Analysis</td>
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<tr>
<td>GA</td>
<td>Genetic Algorithm</td>
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<tr>
<td>GaN</td>
<td>Gallium-Nitride</td>
</tr>
<tr>
<td>HVAC</td>
<td>High-Voltage Alternating Current</td>
</tr>
<tr>
<td>HVDC</td>
<td>High-Voltage Direct Current</td>
</tr>
<tr>
<td>HEMT</td>
<td>High-Electron-Mobility Transistor</td>
</tr>
<tr>
<td>IGSE</td>
<td>Improved Generalized Steinmetz Equation</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PCM</td>
<td>Peak Current Mode</td>
</tr>
<tr>
<td>PCMC</td>
<td>Peak-Current-Mode Control</td>
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<tr>
<td>PFC</td>
<td>Power Factor Correction</td>
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<tr>
<td>POL</td>
<td>Point-Of-Load</td>
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<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
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<td>----------------------------------</td>
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<tr>
<td>PQA</td>
<td>Power Quality Analyzer</td>
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<tr>
<td>PSM</td>
<td>Phase-Shift Modulation</td>
</tr>
<tr>
<td>PSU</td>
<td>Power Supply Unit</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
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<tr>
<td>SiC</td>
<td>Silicon-Carbide</td>
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<tr>
<td>RMS</td>
<td>Root Meas Square</td>
</tr>
<tr>
<td>UPS</td>
<td>Uninterruptable Power Supply</td>
</tr>
<tr>
<td>WBG</td>
<td>Wide Band-Gap</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero-Current Switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
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CHAPTER 1
INTRODUCTION

1.1. Background

In general terms, power electronics is the process of converting and controlling the power flow in electrical systems and appliances by leveraging semiconductor devices. This process often requires meeting specific requirements, demanded by the user or the utility. The hardware that performs the process of power conversion is called “power converter” or simply a “converter”. Power converters can perform different tasks, such as inverting (DC-to-AC), rectifying (i.e. AC- to-DC), AC-to-AC conversion, and DC-to-DC conversion. Power converters are available in a broad power range: from a few tens of watts for household and office systems to a few megawatts for grid-integrated systems.

Nowadays, power electronics converters make up the core of most power conversion systems that are tasked with processing and delivering electric power. In fact, power converters often serve as a delivery link between the source of electric energy and the end-user. The share of electric power processed through power converters and, consequently, the power electronics market value has been rising rapidly over the past several decades. In 2005, approximately 30% of electric power in the United States was processed by power electronics systems, and this share is expected to rise to 80% by 2030 [1]. Likewise, the global power electronics market was valued at $36.35 billion in 2017 and is expected to reach $55.07 billion by 2025 [2]. Consequently, there exists a tremendous economic motivation to optimize these systems. Without high conversion
efficiency, a considerable amount of electric energy is inevitably dissipated in this conversion process. Therefore, as the electric power processing via power converters becomes more common, the need for implementing power converters with high efficiency is becoming more urgent. As a result, high efficiency over a wide range of loads is often required by regulatory organizations, such as Climate Savers [4], the U.S. Energy Star [5], German Blue Angel [6], and 80 Plus [7]. On the other hand, there is also widespread motivation to implement power converters with higher power density in order to reduce overall system size. This trend is depicted in Figure 1-1 for a few types of commercial power converters. Higher power density allows system designers to integrate more equipment into a given enclosure or rack and often leads to lower overall manufacturing cost. Therefore, it is desired to simultaneously increase both the efficiency and power density of power converters.

Figure 1-1: Power density- efficiency trends for some power converters over the years. Adapted from [3].
Due to the ongoing digitalization of modern society, datacenters are on the rise. A huge amount of electric energy is consumed for data storage and cloud computing [8] and more demand is expected in the future as digital technology evolves further. In the U.S. alone, the annual cost to operate datacenters has been on the rise since 1980 [9]. In 2000, it was estimated that roughly 30 billion kWh of energy was consumed by datacenters [10]. In a 2007 report to Congress [11], it was estimated that the datacenter sector consumed about 61 billion kWh of energy in 2006 for a total cost of about $4.5 billion. In 2014, this consumption increased to approximately 70 billion kWh, which is about 1.8% of the domestic electric energy consumption in the U.S. [10]. It is projected that this electric energy demand will increase even faster in the future. Therefore, due to the huge power consumption, there is significant motivation for investigating and implementing more sophisticated hardware and new technologies to improve the efficiency of power conversion within datacenters and reap the resulting cost-saving benefits. Moreover, it is also desirable to increase the power density of converters used in datacenters. This reduces the cost related to space allocation and storage of such systems. Therefore, similar to the general tendency in power electronics, the trend is to move towards more efficient and more dense converters for datacenter applications. Due to the recent commercialization of a new generation of power semiconductors, namely Wide Band-Gap (WBG) semiconductors, this goal is now more achievable than ever.

1.2. The Dilemma of Efficiency vs. Power Density

Modern power electronics has been revolutionized in recent decades by the commercialization of WBG semiconductors. Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) HEMTs are two examples of this new semiconductor technology that have substantially shifted the conventional paradigms in power electronics. Thanks to lower
conduction and switching losses (compared to their Silicon counterparts) [12]-[16], these devices have opened new possibilities for improving the efficiency and power density of power converters beyond the limits imposed by traditional devices. Therefore, these devices further expedite the evolution of power converters towards more efficient and more dense systems. However, as designers move towards more efficient and more dense converters, there are remaining challenges that need to be addressed. One main challenge is simultaneously optimizing system efficiency and power density. In fact, oftentimes within a certain converter category, efficiency and power density have opposing trends. In other words, in most cases, the most efficient implementation of a converter requires making sacrifices in power density and vice versa.

For power converters operating above a few kilowatts, the system volume is often dominated by two main categories of components:

1. Passive power components such as inductors, capacitors, and transformers
2. Thermal management equipment such as heatsinks and fans

In order to reduce the size of passive components, a well-known solution is to increase the switching frequency of the system. The inductors and capacitors used in converters are often utilized as filters (for removing undesired frequency content) or as reservoirs of energy for each operation cycle. Increasing the switching frequency causes the undesired frequency content to also move to higher frequencies, where smaller inductors and capacitors are needed for filtering. Similarly, increasing the switching frequency leads to the need for a smaller amount of stored energy during each operating cycle. This also leads to a smaller size for inductors and capacitors that are utilized as reservoirs of energy. In a similar fashion, the overall size for power transformers is also reduced when switching frequency is increased.
On the other hand, reducing the thermal management equipment size requires reducing the overall dissipated power within the system. Heat sinks are often used for managing the thermal behavior of power semiconductors. Conduction and switching losses are the two main constituents of dissipated power in semiconductors. While the conduction loss is frequency-independent, the switching loss is mainly governed by the switching frequency. In other words, increasing the switching frequency causes proportionally higher switching loss. If this trend is not counteracted in some manner, this leads to larger heatsinks and thermal management equipment.

In this sense, increasing the switching frequency, on one hand, reduces the size of passive components and, on the other hand, leads to larger thermal management equipment. The presence of these competing effects makes it difficult to predict the impact of increasing switching frequency in a general sense. However, it is clear that increasing switching frequency has a deleterious effect on the size of the thermal management system due to increased switching loss. It is also clear that increasing switching frequency has a negative impact on system efficiency. In order to achieve both high power density and high system efficiency, switching loss must be limited in some manner.

1.3. Soft-Switching Converters: A Necessity for Efficient and Dense Solutions at High Power

The solution to the aforementioned problem, and the key to unleashing converter performance at high switching frequency, is realizing “soft-switching”. Soft-switching is defined in contrast to “hard-switching”, which describes a situation in which the current and voltage of a switch experience substantial “overlap” during switching transitions. This substantial overlap, in return, leads to switching loss, as depicted in Figure 1-2. Soft-switching techniques, in essence, strive to reduce or even eliminate this overlap, as depicted in the notional diagram of Figure 1-3.
Realizing soft-switching is an essential step to realize highly efficient and highly dense power converters due to the reasons mentioned in section 1.2. Converter topologies that work under the concept of soft-switching are often the only choice in applications that seek the simultaneous realization of high efficiency and high power density.

The basic idea that enables soft-switching is leveraging resonant action between electrical elements of the circuit in order to make either the current or the voltage for a given switch zero (or nearly zero) during the switching transitions. This leads to the definition of the terms “Zero-
Voltage Switching” (ZVS) and “Zero-Current Switching” (ZCS). Realizing ZVS, for example, leads to a significant reduction of switching loss because the stored charge in the output capacitance of the switch is not dissipated in the channel of the device each time it turns on. As a matter of fact, prior to turning the device on, the charge in the output capacitance is removed and returned to the supply or other energy storing components, leading to no (or minimal) output capacitance charge to be dissipated at the time of turn-on.

Accordingly, based on the elements that take part in the resonant action, two major categories of soft-switching converters can be identified:

1. Resonant converters
2. Quasi-resonant converters

In resonant converters [18]-[20] discrete inductors and capacitors are often employed as the constituents of an easily-distinguishable resonant tank in order to make sinusoidal (or semi-sinusoidal) current waveforms that pass through the switches. By switching each device at instances during which the relevant current or voltage waveform crosses zero, ZCS or ZVS, respectively, can be achieved. Very high efficiency can be obtained as a result of this scheme. However, a variable switching frequency is often required to regulate the output voltage in this category of converters [20]. This complicates designing the EMI filter necessary to comply with EMI standards. Moreover, the control characteristics of these converters are complicated due to the dynamics of the resonant tank [21]. Furthermore, implementing over-current protection is often more complex for these converters as well [22].

On the other hand, in the quasi-resonant converter category, the resonant tank is less distinctive. In topologies of this category, the output capacitance of the switches is often utilized as the capacitance portion of the resonant tank instead of discrete capacitors. The required
inductance can be realized by either a discrete inductor component or the stray inductances of the circuit (e.g. leakage inductance of the transformer). Unlike the resonant converters, only limited resonant action takes place between the resonant tank elements within a quasi-resonant converter. This quasi-resonance mechanism is utilized to achieve ZVS or ZCS in these topologies. Although a resonant converter often has a slight advantage in terms of efficiency, a comparable quasi-resonant converter has other advantages. Unlike resonant converters, quasi-resonant converters operate with fixed switching frequency. Therefore, the required EMI filters are smaller and simpler to design. Moreover, the control scheme used in quasi-resonant converters is often simpler than that employed for fully resonant converters.

Soft-switching techniques are especially important in the context of high-power DC-DC converters, which provide DC voltage level change. Such systems play an important role in datacenters, energy storage, and high-voltage direct current (HVDC) applications. These converters are often required to provide galvanic isolation in order to comply with safety standards. Soft-switching techniques are highly beneficial in such systems to reduce total power loss and support system size reduction by enabling operation at higher switching frequencies. The most popular soft-switching topologies for high-power DC-DC converter applications are the LLC converter [20] and phase-shifted full-bridge (PSFB) converter [23], which are shown in the schematics of Figure 1-4(a) and Figure 1-4(b), respectively. The LLC converter belongs to the resonant converter category and the PSFB converter belongs to the quasi-resonant converter category. Both LLC and PSFB converters are popular topologies in the datacenter applications since they meet the demands of efficient power conversion and high power density. While the LLC converter is often employed at the Point-of-Load (POL) in the conventional architecture of power distribution in datacenters [24][25], the PSFB converter is often employed as the main
DC-DC power supply unit (PSU) [26][27]. This power supply unit is tasked with providing a lower DC-bus voltage for the POL units. Accordingly, the focus of this dissertation is the modeling and optimization of the PSFB topology with a focus on the specifications for datacenter applications.

1.4. Literature Review

The PSFB converter was invented in the late 1980s [23] and since has been the subject of many studies seeking to improve its performance. Efficiency optimization of this converter has many degrees of freedom that collectively influence the system efficiency. This complicates the selection of component values and control parameters and makes it difficult to achieve an
optimized solution. The most widely studied parameters include the resonant inductor value \((L_r)\), the switch output capacitance \((C_{oss})\), the switch deadtime values, and the converter output power level. Numerous researchers have investigated the efficiency improvement of this converter by either modifying the structure of the converter or by tuning the original structure parameters, such as deadtime values and the size of the resonant inductor.

To improve efficiency, some studies have proposed extending the ZVS range of the converter by adding auxiliary circuits to the original converter. For example, P. Jain \textit{et al} \cite{Jain2014} proposed employing an asymmetrical auxiliary circuit, formed by a few passive components, in order to achieve ZVS under all load and line conditions. A. Safae \textit{et al}. \cite{Safaee2015} suggested adding an auxiliary resonant circuit to the primary side of the PSFB converter that can extend the ZVS range with reduced RMS current in the auxiliary circuit. Z. Chen \textit{et al}. \cite{Chen2016} also proposed an auxiliary circuit, consisting of capacitors and inductors, that can realize ZVS for all primary switches across the entire load range. In another investigation \cite{Yu2017}, these authors also proposed an active auxiliary circuit with self-regulating current in order to extend the ZVS range of the lagging switches to the full load range. This configuration is demonstrated to improve the overall system efficiency profile. M. Yu \textit{et al}. \cite{Yu2018} proposed a hybrid PSFB converter, which is assisted by an auxiliary half-bridge LLC circuit for the lagging switches. This configuration is demonstrated to improve ZVS for the lagging switches in applications with low-voltage, high-current output. Y. Kim \textit{et al}. \cite{Kim2019} also proposed including two auxiliary switches along with a large resonant inductor to reduce the conduction losses caused by circuiting currents on the primary side of the PSFB converter. In another effort, Y. Jang \textit{et al}. \cite{Jang2020} proposed an auxiliary circuit consisting of two magnetic components to improve ZVS for all switches over a wide range of input voltage and output load conditions. The authors later proposed another auxiliary
circuit [35] with adaptive energy storage that offers ZVS for the primary switches across a wide range of loads along with reduced duty-cycle-loss and reduced no-load circuiting energy. S. Jeon and G. Cho [36] proposed an auxiliary circuit consisting of a transformer along with two diodes in order to obtain ZCS for the leading switches of the PSFB converter. In a similar approach, M. Borage et al. [37] suggested a passive auxiliary circuit along with an auxiliary transformer that extends ZVS to the entire load range with decreasing effect on conduction losses as the output power increases. J. Dudrik et al. [38] proposed employing a secondary-side controlled switch along with a custom control algorithm in order to achieve full-load-ZVS and to reduce circulating current in the converter. X. Wu et al. [39] proposed an auxiliary circuit consisting of two coupled inductors and two clamped diodes on the primary side of the converter. This modification is demonstrated to extend the ZVS range of the PSFB converter from no load to full load and to reduce both conduction losses and switch voltage oscillation. A. Mousavi et al. [40] proposed an auxiliary circuit consisting of an active switch, a diode, a capacitor, and an inductor to achieve ZCS along with ZVS for the primary switches. M. Borage et al. [41] also proposed employing two power transformers to extend the ZVS range without significantly increasing the full-load conduction loss. Although these solutions may improve the performance of the PSFB topology, the additional complexity introduced into the system can reduce applicability for industrial applications, for which reliability and cost are important factors.

On the other hand, some studies have sought to improve the system efficiency without additional auxiliary components and by leveraging the basic structure of the PSFB converter. In one of the first studies on this topology, J. A. Sabate et al. [42] discussed important PSFB design parameters, including the selection of the resonant inductor value and identification of the critical load current below which ZVS is lost. R. Redl et al. [43] studied the selection of the transformer
magnetizing inductance and the resonant inductor value to maintain ZVS for an extended range of loads. Zhao et al. [44] provided an analytical method to optimize the deadtime as a function of load current. Kim et al. [45], [46] investigated efficiency improvement at light-load conditions by implementing variable deadtimes and modifying the switching strategy. B. Chen and Y. Lai [47] demonstrated that under light-load and standby conditions, changing the switching control scheme from phase-shifting to pulse-width modulation (PWM) can further improve the PSFB converter efficiency. Hallworth et al. [48] presented a method for calculating the required resonant inductor value for achieving ZVS, considering the effects of deadtime and transformer magnetizing inductance. Other studies have proposed employing saturable inductors in the structure of the PSFB converter to extend the ZVS range [49]-[52]. However, this method has disadvantages, such as increased complexity, increased circulating currents, and potential thermal problems [53]. For these reasons, this method not been widely implemented. Most of these studies, although contain some description of the influence of individual system parameters, do not investigate the collective influence of design parameters on the system efficiency.

1.5. Dissertation Objectives and Outline

This dissertation aims to methodically investigate optimizing the PSFB converter for higher efficiency and higher power density. Specifically, the main objectives of this work are summarized in the following subsections.

1.5.1. Empirically validated theoretical model of ZVS transitions

As mentioned, although the literature contains some description of the influence of the individual parameters that collectively influence the performance of the PSFB topology, the coupled influence of these parameters has not been thoroughly explored. Understanding the
interdependence of the various parameters of influence within the PSFB converter is critical for performing an effective performance optimization of this topology. This is true for two reasons. First, this topology is sufficiently complex that variations in multiple parameters can produce behavior that is either combinatorial or complementary in nature. That is, variation in a given parameter may not have the expected influence when combined with variations in another parameter. Second, there are subtle influences that affect the performance of the PSFB converter that have not been detailed in the literature to date. One example is the impact of gate-drive circuit behavior on the presence of MOSFET $C_{oss}$ charging/discharging losses, which can be significant. Ignoring this parameter of sensitivity can lead to overprediction of expected system efficiency and suboptimal performance once a given design is reduced to practice.

Therefore, the first main contribution of this dissertation is an empirically validated theoretical model of ZVS transitions that addresses the major sources of performance sensitivity within the PSFB topology as well as the collective effect of system parameters on achieving ZVS. This model is the cornerstone for understanding the underlying cause and effect phenomena that govern the efficiency of the PSFB converter through the ZVS mechanism and can be used to optimize the efficiency and power density of PSFB converters.

1.5.2. Multi-objective optimization framework for the PSFB topology

The second main contribution of this dissertation is a MATLAB-based optimization framework for optimizing the PSFB converter with regard to efficiency and power density. By leveraging loss models and volumetric models of various system components, this optimization framework can perform a systematic multi-objective optimization for the PSFB topology. This optimization enables designers of this topology to quantify the trade-off between efficiency and power density and assess the impact of specific component selection decisions. One critical
component of this optimization framework is the theoretical ZVS model developed herein for tuning the ZVS mechanism. By employing this optimization framework, the capability of the PSFB topology for simultaneously achieving high efficiency and high power density can be realized.

1.5.3. Practical application guidelines for the PSFB topology

The third main contribution of this dissertation is a set of practical guidelines and suggestions that provide insight into the practical aspects of tuning this converter topology. As will be discussed, some of the system mechanisms have specific and sometimes surprising implications for system performance once a design is reduced to practice. In discussing such nuances and presenting the associated guidelines, this dissertation sets a foundation that system designers can utilize to obtain the full performance entitlement of the PSFB topology in practical designs.

1.5.4. Dissertation outline

The remainder of this dissertation is organized as follows. CHAPTER 2 presents the operation analysis of the PSFB converter at each operation mode. The fundamental and important relations between different system parameters are also presented in this chapter. CHAPTER 3 presents a detailed description of the ZVS mechanism used in the PSFB converter and introduces a theoretical model of the ZVS transitions for this topology. Furthermore, the major sources of sensitivity for the ZVS phenomenon are identified and studied in this chapter. CHAPTER 4 presents the details of a 10 kW prototype PSFB converter that serves as the primary test platform for this research. This chapter also includes empirical validation of the predictions of the analytical ZVS model presented in CHAPTER 3. CHAPTER 5 presents the details of a MATLAB-based framework designed to perform pareto-based optimization of the
PSFB topology in consideration of the inherent trade-off between efficiency and power density in this topology. This chapter concludes with the identification of an optimized 10 kW PSFB converter design to improve upon the performance of the original prototype PSFB converter described in CHAPTER 4. CHAPTER 6 presents the implementation and empirical evaluation of the optimized 10 kW prototype PSFB converter and validates the performance improvements projected in Chapter 5. Finally, CHAPTER 7 summarizes the contributions and significance of this work and proposes possible future work.
CHAPTER 2
OPERATION ANALYSIS OF THE PSFB CONVERTER

2.1. Introduction

Analysis of the PSFB converter is an involved task due to the complexity of the system and the number of modes involved. However, an in-depth understanding of the operating modes of the system establishes a clear path towards designing and optimizing this topology. Therefore, a thorough analysis of the system operating modes and the system behavior is presented in this chapter. The PSFB converter is analyzed at each operating mode and equivalent circuits are presented, wherever necessary, in order to simplify the analysis. Moreover, important relations between system variables and parameters that will be needed in the following chapters are presented here as well.

2.2. The PSFB Converter Circuit Topology and Control Scheme

The PSFB converter schematic is shown in Figure 2-1. This configuration of the PSFB converter is based on the original form described in [23]. A full-bridge inverter (formed by switches $Q_1$, $Q_2$, $Q_3$, and $Q_4$) converts the DC voltage, supplied by the source $V_{in}$, to a bipolar square-wave voltage and supplies it to the high-frequency transformer, $T_r$. The transformer $T_r$ provides galvanic isolation, which is often required by safety standards, between the primary and secondary sides of the circuit and delivers power to the secondary-side rectifier. $L_m$ and $L_{lk}$ represent the magnetizing and leakage inductances of the transformer, respectively. The secondary-side rectifier (formed by diodes $D_{R1}$, $D_{R2}$, $D_{R3}$, and $D_{R4}$) rectifies the delivered
Depending on the application, a center-tapped full-wave rectifier (which requires a center-tapped transformer) can also be used for this section. A low-pass filter (formed by $L_o$ and $C_o$) filters the rectified voltage and provides a DC voltage at the system output.

The structure shown in Figure 2-1 includes several minor changes in the primary side of the original PSFB converter design [23] to improve its performance. The first modification is necessary to address the excessive voltage stress on the secondary-side diodes due to the resonance caused by the junction capacitances of those diodes with the transformer leakage inductance and the resonant inductor $L_r$. Without managing this voltage stress, the reliability of the converter is compromised, especially in high-voltage, high-power applications. To overcome this issue, various modifications to the original converter structure have been proposed, such as employing auxiliary components [29][51][54][55] or snubbers [46][56][57]. However, in spite of being effective in controlling this voltage stress, most of these schemes add to the cost and complexity of the system and/or introduce considerable losses. Therefore, among all these schemes, the method that uses two diodes in the primary side to clamp the transformer voltage to the positive and negative bus rails is generally preferred [43][58]. The implementation of this method is illustrated by the inclusion of diodes $D_{p1}$ and $D_{p2}$ in Figure 2-1. This method is very
effective, simple, and inexpensive to implement. The second modification is the inclusion of a so-called resonant inductor \( L_r \) in series with the transformer primary winding. This inductor increases the energy available to drive pseudo-resonant switching transitions and extends the ZVS range of the converter to lower output power levels. It should be mentioned that a transformer with high leakage inductance can also be employed to eliminate the need for the resonant inductor \( L_r \). While this method may be attractive volume-wise, voltage stress on the secondary-side diodes remains an issue due to the high leakage inductance. Unfortunately, damping diodes \( D_{p1} \) and \( D_{p2} \) are not very effective in this configuration. In this case, other methods of managing this voltage stress, such as auxiliary circuits or snubbers, must be employed. Unfortunately, these methods usually increase the cost and/or losses of the system and can compromise the benefits of using a transformer with high leakage inductance. The third modification is the inclusion of a DC-blocking capacitor \( C_b \) to guarantee the volt-second balance of the transformer and avoid staircase saturation of the transformer core. Use of this capacitor is optional if reliable peak-current mode (PCM) control and cycle-by-cycle current limiting features are implemented. However, employing this capacitor can add a measure of redundancy that may prove helpful in the case of controller malfunction or current sensor failure. This is especially useful for industrial applications in which a converter may be subject to harsh environmental effects and/or interactions with upstream or downstream power conversion stages. \( C_b \) is typically selected to be large enough that its impedance is low at the designed operating frequency of the converter and that it does not increase the voltage stress of the secondary diodes [59].
Figure 2-2: Important waveforms of the PSFB converter.
The switching methodology of the PSFB converter distinguishes this topology from the hard-switched full-bridge converter [60] and facilitates realizing ZVS for the primary side switches. The PSFB converter utilizes a distinctive switching scheme called phase-shift modulation (PSM). Figure 2-2 shows the gate-drive signal diagram for the PSM scheme along with the most important waveforms of the PSFB converter. In this scheme, all switches maintain a constant duty ratio of approximately 50%. In addition, the two switches in each leg of the converter are switched in a complementary fashion with an interposed deadtime interval. The converter duty cycle and the voltage applied to the transformer primary winding are controlled by the overlap between the conduction time of the diagonal switches. As shown in Figure 2-2, the switching commands for the switches in one leg always precede the switching commands for the switches in the other leg by a short interval \([t_1, t_4]\). The switches that operate near the beginning of this interval are called the “leading switches”; while those that that operate near the end of this interval are called the “lagging switches”. In the schematic of Figure 2-1, \(Q_2\) and \(Q_4\) are the leading switches and \(Q_1\) and \(Q_3\) are the lagging switches, as demonstrated by the timing diagram of Figure 2-2.

As in the traditional PWM method, the transformer primary winding is alternately excited with positive and negative voltage pulses during certain intervals. During each of these “power transfer” intervals, one pair of diagonal switches is excited simultaneously. This power transfer period is distinguished by the red shaded area in the \(V_{AB}\) diagram of Figure 2-2. The difference between PSM and the traditional PWM scheme relates to how the system behaves in the “freewheeling” interval. During the PSFB freewheeling interval, either the two top switches (or their corresponding body diodes) are on while the two bottom switches are off, or the two bottom switches (or their corresponding body diodes) are on while the two top switches are off. In either
case, the current that was flowing in the primary winding of the transformer immediately before
the freewheeling interval is forced to continue flowing in a circulating manner. This current will
circulate in the path $Q_1\cdot L_r \cdot D_{P1}/Q_2$ or the path $Q_4\cdot D_{P2} \cdot L_r \cdot Q_3$ depending on the polarity of the
primary current during the preceding power transfer interval. These two paths are annotated in
Figure 2-2 with blue and red dashed arrows, respectively. In this topology, the energy that is
captivated in these circulating paths is then leveraged to achieve ZVS.

2.3. Modal Analysis of the PSFB Converter Operation

This section takes a close look at the detailed operating principle of the PSFB converter
by studying each operating mode individually. This study makes a solid foundation for modeling
and optimization of the ZVS mechanism in this converter topology. The steady-state operation
waveforms of Figure 2-2 are considered and referred to in the following modal analysis. This
includes modes of operation within the $[t_0 \ t_8]$ time range, which corresponds to eight distinct
modes. Since the waveforms in the second half of the switching period repeat in a similar fashion
but in reverse polarity, only the modes of the first half switching cycle are discussed.

2.3.1. Mode 0: $[t_0 \ t_1]$

The primary and secondary side conduction paths of mode 0 are indicated with red lines
in the schematic of Figure 2-3. In this mode, power is transferred from the input to the output.

![Figure 2-3: The PSFB converter schematic in mode 0 ($[t_0 \ t_1]$).](image-url)
The switches $Q_1$ and $Q_4$ conduct and a positive voltage, which is almost equal to the input voltage $V_{in}$, is applied to the transformer primary. Diodes $D_{R1}$ and $D_{R4}$ also conduct in this mode and deliver a rectified voltage to the output filter. As a result, the transformer primary current rises with a constant slope during this period. If the resonant inductor $L_r$ is relatively large, this inductor current remains almost constant during this time interval. The damping diode $D_{p1}$ fully or partially conducts during this time interval and bypasses some of the resonant inductor current, $i_{Lr}$. As long as this diode conducts, the resonant inductor current is higher than the transformer primary current, $I_p$.

2.3.2. Mode 1: $[t_1, t_2]$

The primary and secondary side conduction paths of mode 1 are indicated with red lines in the schematic of Figure 2-4. In mode 1, the drain-source capacitance of a leading switch is discharged, and that switch is prepared to be turned on under ZVS conditions. This mode starts with turning off switch $Q_4$, which is a leading switch, at time $t_1$. Meanwhile, switch $Q_1$, which is a lagging switch, remains on. The primary current starts flowing through the drain-source capacitances of switches $Q_2$ and $Q_4$. This means that $C_{DS4}$ starts charging and $C_{DS-2}$ starts discharging. If enough energy is provided by the inductive elements of the circuit, current flows into these capacitances until $C_{DS4}$ is charged to the input voltage value $V_{in}$, and $C_{DS2}$ is

![Figure 2-4: The PSFB converter schematic in mode 1 ($[t_1, t_2]$).](image-url)
discharged to zero. Subsequent to this, the voltage across drain-source of switch $Q_2$ reaches zero and the time window for ZVS turn-on of this switch begins. During this interval, the voltage at node $B$ rises from nearly $0\, V$ to $V_{in}$, which causes the transformer primary voltage $V_p$ to decreases from $V_{in}$ to $0\, V$. It is noted that node $A$ remains at $V_{in}$ during this interval due to the conduction of $Q_1$. Meanwhile, since the primary transformer voltage is decreasing to zero, the transformer secondary voltage also starts decreasing to zero. Consequently, the junction capacitance of inactive diodes $D_{R2}$ and $D_{R3}$ start discharging. Discharging the junction capacitances of $D_{R2}$ and $D_{R3}$ sets the stage for these diodes to be turned on. Since this mode only involves capacitance charging and discharging, it only lasts for a short period of time, i.e. from $t_1$ to $t_2$.

In this mode, the total required energy to charge $C_{DS4}$ and discharge $C_{DS_2}$ is mainly provided by the output filter inductor $L_o$, and to a lesser degree by the transformer leakage inductance $L_{lk}$ and the magnetizing inductance $L_m$. Usually, the output filter inductor is the largest of these three components. Therefore, the charging and discharging of the affected switch capacitances is mainly fueled by this inductor during this mode. Moreover, since this transition happens right after the power transfer period, there is often enough energy stored in the output filter inductor to discharge the corresponding leading switch $C_{DS}$ (in this mode $C_{DS2}$) even at low output power levels. This means that the conditions for realizing ZVS of the leading switches are easily met under most operating conditions for practical converter implementations.

2.3.3. Mode 2: $[t_2 \, t_3]$

The primary and secondary conduction paths of mode 2 are indicated with red lines in the schematic of Figure 2-5. In this mode, the body diode of switch $Q_2$ (i.e. $D_2$) is turned on as a result of its $V_{DS}$ reaching zero at the end of mode 1. Conduction of this body diode clamps the
$V_{DS}$ of switch $Q_2$ to (almost) 0 V. As shown in Figure 2-5, the primary current circulates in a freewheeling fashion in a minimally dissipative path, consisting of $Q_1$-$L_r$-$D_{p1}/D_2$. In this mode, power is not transferred from the input to the output and the transformer primary and secondary winding voltages are negligibly small. On the secondary side, all diodes are conducting and share a portion of the output inductor current, $i_{L_o}$. Moreover, during this interval, the output power is solely supplied by the filter inductor and capacitor, $L_o$ and $C_o$, respectively.

2.3.4. Mode 3: [$t_3$-$t_4$]

The primary and secondary conduction paths of mode 3 are indicated with red lines in the schematic of Figure 2-6. At $t_3$, switch $Q_2$ is turned on. Right before this instance, the body diode of this switch (i.e. $D_2$) was conducting. Therefore, the voltage across drain-source of $Q_2$ is clamped at zero. Consequently, this switch is turned on with ZVS and incurs nearly zero turn-on
switching loss. During this interval, the primary current continues freewheeling in the minimally dissipative path, consisting of $Q_1 - L_r - D_{P1}/Q_2$. Similar to mode 2, no power is transferred from the input to the output and all secondary diodes conduct a portion of the output inductor current. The filter inductor and filter capacitor continue supplying power to the output in this mode.

2.3.5. Mode 4: [$t_4 \, t_5$]

The primary and secondary conduction paths of mode 4 are indicated with red lines in the schematic of Figure 2-7. In mode 4, the drain-source capacitance of a lagging switch is discharged, and that switch is prepared to be turned on under ZVS conditions. At time $t_4$, switch $Q_1$, which is a lagging switch, is turned off. The resonant inductor current, $i_{Lr}$, which in mode 3 was flowing through the channel of switch $Q_1$, starts flowing through drain-source capacitances of switches $Q_1$ and $Q_3$. This means that $C_{DS1}$ starts charging and $C_{DS3}$ starts discharging. If enough inductive energy is stored in the resonant inductor $L_r$, current flows through these capacitances until $C_{DS1}$ is charged to $V_{in}$ and $C_{DS3}$ is discharged to zero. This means that the energy stored in $C_{DS3}$ is transferred back to the input source. Subsequent to this, the time window for ZVS turn-on begins for the switch $Q_3$. It is noted that during this interval, the voltage at node $A$ falls from $V_{in}$ to 0 V.

Figure 2-7: The PSFB converter schematic in mode 4 ($[t_4 \, t_5]$).
In this mode, the resonant inductor \( L_r \) is solely responsible for providing the required inductive energy to discharge the drain-source capacitance of switch \( Q_3 \). The stored energy in this inductor is a function of load current and the resonant inductor value, \( L_r \). Since the reflected secondary current does not participate in this transition, the lagging switches are susceptible to losing ZVS at light load. Therefore, if sufficient inductive energy is not available for a full discharge, a partial discharge of \( C_{DS3} \) may take place. In this case, ZVS does not occur but some reduction in switching loss is achieved compared to hard switching. A more detailed description of this scenario is presented in CHAPTER 3. Also, similar to the previous mode, no power is transferred from the input to the output in mode 4. All output diodes conduct a portion of the output inductor current and the output power is solely supplied by the output filter inductor and capacitor.

2.3.6. Mode 5: \([t_5 \: t_6]\)

The primary and secondary conduction paths of mode 5 are indicated with red lines in the schematic of Figure 2-8. At time \( t_5 \), the drain-source voltage of switch \( Q_3 \) reaches zero. Consequently, the corresponding body diode \( D_3 \) starts conducting the resonant inductor current \( i_{L_r} \). Therefore, at \( t_5 \), the time window for ZVS turn-on of switch \( Q_3 \) begins. Moreover, due to the conduction of \( D_3 \) and \( D_{P1} \), almost the full input voltage \( V_{in} \) is applied across \( L_r \). Consequently,

![Figure 2-8: The PSFB converter schematic in mode 5 \((t_5 \: t_6)\).](image)
$i_{L_r}$ decreases rapidly during this interval. Similar to the previous mode, no power is transferred from the input to the output and all secondary diodes share the filter inductor current $i_{Lo}$. The output power is still solely supplied by the output filter inductor and capacitor in this mode.

2.3.7. Mode 6: [$t_6 \rightarrow t_7$]

The primary and secondary conduction paths of mode 6 are indicated with red lines in the schematic of Figure 2-9. At time $t_6$, switch $Q_3$ is turned on. Since in the previous mode the corresponding body diode (i.e. $D_3$) was conducting, $Q_3$ is tuned on with ZVS and incurs almost zero turn-on switching loss. The resonant inductor current, $i_{Lr}$, flows from source to drain of $Q_3$ and continues to decline rapidly because the input voltage is applied directly across this inductor. This mode continues until $i_{Lr}$ reaches zero and starts flowing in the opposite direction. Similar to the previous mode, no power is transferred from the input to the output, and the output power is solely supplied by the output filter inductor and capacitor. Also, all secondary diodes continue to share the filter inductor current.

2.3.8. Mode 7: [$t_7 \rightarrow t_8$]

The primary and secondary conduction paths of mode 7 are indicated with red lines in the schematic of Figure 2-10. At time $t_7$, the direction of $i_{Lr}$ and $i_p$ change and the damping diode
$D_{p1}$ turns off. The transformer primary current continuously increases until it is equal to the filter inductor current value reflected to the primary side. In the meantime, no power is transferred from the input to the output and all the secondary diodes share the filter inductor current. At time $t_B$, $i_p$ reaches the inductor current value reflected to the primary side, and diodes $D_{R1}$ and $D_{R4}$ turn off, while diodes $D_{R2}$ and $D_{R3}$ continue conducting the filter inductor current. Consequently, a new power transfer interval begins, and power is transferred from the input to the output through the transformer once again. After time $t_B$, the second half of the switching cycle begins. The operating principals of the second half are identical to the sequence of modes described previously, only the involved switches and diodes are different.

2.4. Important Relations of the PSFB Converter

This section presents some important expressions between different system variables and parameters that arise from the modal analysis presented in the previous section. These expressions will be leveraged in the later chapters to study the ZVS mechanisms of this topology and to optimize its design.

The PSFB converter is a step-down and galvanically isolated DC-DC converter. The relation between input and output voltages is regulated by adjusting the effective duty cycle, $D_{eff}$. This relationship is given by:
\[ V_o = \frac{D_{eff}}{n} \times V_{in} \]  \hspace{1cm} (2-1)

where \( n \) is transformer primary to secondary turns ratio (i.e. \( \frac{n_p}{n_s} \)). The actual duty cycle, \( D_o \), is defined as the ratio of the overall simultaneous conduction time of diagonal switch pairs (i.e. \( Q_1/Q_4 \) and \( Q_2/Q_4 \)) to the switching period, \( T_{sw} \).

\[ D_o = \frac{T_{on}}{T_{sw}} \]  \hspace{1cm} (2-2)

However, due to time interval \([t_5 \ t_8]\), which is required for the resonant inductor current to change direction, a portion of \( D_o \) does not contribute to transferring power from the input to the output during each cycle. In other words, some duty cycle is lost. Therefore, the term “duty cycle loss”, \( D_{loss} \), is often used, which defines the amount of duty cycle that is lost during each switching period. Therefore, the effective duty cycle, during which power is transferred from the input to the output, is defined as:

\[ D_{eff} = D_o - D_{loss} \]  \hspace{1cm} (2-3)

The amount of duty cycle loss is determined by several system parameters. Duty cycle loss is defined as:

\[ D_{loss} = \frac{4 \times I_{p,max} \times f_{sw} \times (L_r + L_{lk})}{V_{in}} \]  \hspace{1cm} (2-4)

where \( L_r \) and \( L_{lk} \) are the resonant inductor and transformer leakage inductance, respectively; \( f_{sw} \) is the switching frequency; and \( V_{in} \) is the input voltage. Also, \( I_{p,max} \) is the maximum transformer primary current, which can be defined as follows:

\[ I_{p,max} = \frac{I_o}{n} + \frac{(1 - D_{eff}) \times V_o}{4 \times n \times L_o \times f_{sw}} \]  \hspace{1cm} (2-5)

where \( I_o \) is the output current, \( n \) is the transformer primary to secondary turns ratio, \( D_{eff} \) is the effective duty cycle, \( V_o \) is the output voltage, \( L_o \) is the output filter inductor, and \( f_{sw} \) is the
switching frequency. As can be deduced from (2-4) and (2-5), multiple system parameters affect
the amount of duty cycle loss. As the output power increases, more duty cycle loss is expected.
Similarly, increasing the value of the resonant inductor and the transformer leakage inductance
leads to increased duty cycle loss. On the other hand, a larger filter inductor or higher switching
frequency can slightly reduce the duty cycle loss.

The transformer maximum magnetizing current, \( i_{m,\text{max}} \), can be estimated as follows:

\[
i_{m,\text{max}} \approx \frac{D_{\text{eff}} \times V_{\text{in}}}{4 \times L_m \times f_{\text{sw}}} \tag{2-6}
\]

where \( D_{\text{eff}} \) is the effective duty cycle, \( V_{\text{in}} \) is the input voltage, \( L_m \) is the transformer magnetizing
inductance, and \( f_{\text{sw}} \) is the switching frequency.

The resonant inductor maximum current, \( i_{\text{lr, max}} \), is equal to:

\[
i_{\text{lr, max}} = \frac{I_o}{n} + \frac{(1 - D_{\text{eff}}) \times V_o}{4 \times n \times L_o \times f_{\text{sw}}} + i_{m,\text{max}} \tag{2-7}
\]

where \( I_o \) is the output current, \( n \) is the transformer primary to secondary turns ratio, \( D_{\text{eff}} \) is the
effective duty cycle, \( V_o \) is the output voltage, \( L_o \) is the output filter inductor, \( f_{\text{sw}} \) is the switching
frequency, and \( i_{m,\text{max}} \) is the maximum magnetizing current.

The current in the output filter inductor, \( L_o \), has an average value equal to the output
current, \( I_o \). The ripple current of this inductor is expressed as:

\[
\Delta I_{L_o} = I_{L_o,\text{max}} - I_{L_o,\text{min}} = \frac{(1 - D_{\text{eff}}) \times V_o}{2 \times L_o \times f_{\text{sw}}} \tag{2-8}
\]

where \( D_{\text{eff}} \) is the effective duty cycle, \( V_o \) is the output voltage, \( L_o \) is the output filter inductor,
and \( f_{\text{sw}} \) is the switching frequency. Accordingly, the maximum and minimum values of the
output filter inductor current are defined as follows:
Assuming that the output filter capacitor, $C_o$, has negligible equivalent series resistance (ESR), the output ripple voltage is expressed as:

$$\Delta V_o = \frac{\Delta I_{Lo}}{16 \times C_o \times f_{sw}}$$

(2-11)

where $\Delta I_{Lo}$ is the output inductor ripple current, $C_o$ is the output filter capacitor, and $f_{sw}$ is the switching frequency. Note that if the output capacitor ESR is not negligible, the output ripple voltage increases due to the contribution of this resistance.

The RMS current in the primary switches during steady-state operation can be approximated as:

$$I_{sw, prim} \approx \frac{\sqrt{2}}{2} \times I_{lr, max}$$

(2-12)

Similarly, the RMS current in the secondary-side diodes (or switches, if synchronous rectification is employed) can also be estimated as:

$$I_{sw, sec} \approx \sqrt{\frac{I_o^2 + \frac{\Delta I_{Lo}^2}{3}}{2}}$$

(2-13)

where $I_o$ is the output current and $\Delta I_{Lo}$ is the output inductor ripple current.

This chapter has provided a detailed analysis of the PSFB converter operation and has identified important relationships between various variables within this system. By leveraging this understanding, it is possible to perform a detailed investigation of the ZVS mechanism and
the elements that govern this phenomenon in the PSFB converter. Such an analysis is the subject of the next chapter.
CHAPTER 3
MODELING OF ZVS TRANSITIONS FOR EFFICIENCY OPTIMIZATION OF THE PSFB CONVERTER

3.1. Introduction

Within the PSFB converter topology, the operation of the ZVS mechanism is the key factor to consider for maximizing efficiency and optimizing performance. This mechanism contains many degrees of freedom that collectively govern system efficiency. However, the interdependence of these parameters often complicates tuning of the ZVS mechanism. That is to say, considering a subset of the parameters of influence when tuning the ZVS mechanism may not lead to the best possible design. Consequently, a system designed in this manner will achieve suboptimal performance once reduced to practice.

This chapter presents a detailed description of the ZVS mechanism within the PSFB converter, followed by a theoretical framework that models the associated ZVS transitions and addresses the major sources of sensitivity for achieving ZVS within this topology. This unified approach takes into account the effect of major parameters of influence as well as their interdependence for the purpose of tuning the ZVS mechanism.
3.2. ZVS Realization in the PSFB Converter

In the PSFB converter, the primary switches have the opportunity to turn on with ZVS. During the freewheeling interval (i.e. from time $t_1$ to $t_6$ in Figure 2-2) a portion of the energy stored in the inductive elements of the system during the preceding power transfer interval is captive in a minimally dissipative primary-side path. At the end of the freewheeling interval, this stored energy is used to charge the $C_{oss}$ of the switch that is turning off and to discharge the $C_{oss}$ of the complementary switch that will be turned on. In the case of complete discharge of the complementary device $C_{oss}$, this switch can subsequently be turned on with almost zero turn-on switching loss. This phenomenon is called ZVS. Figure 3-1 shows an example drain–source voltage ($V_{DS}$) waveform for the switch that is turning on during the deadtime period. Due to the resonant action between the switch $C_{oss}$ and the corresponding inductive elements of the system, $V_{DS}$ swings from the input bus voltage to zero. The time required for this process to complete is

![Figure 3-1: Example of $V_{DS}$ waveform showing the ZVS opportunity time window.](image)
denoted in this figure by $T_d(min)$. At this point, the switch body diode starts conducting, $V_{DS}$ remains clamped near 0 V, and the ZVS opportunity time window begins. At this point, the switch can be turned on with almost zero turn-on switching losses. However, as shown in Figure 3-1, this time window is limited. At time $T_d(max)$, $V_{DS}$ starts rising back to the input bus voltage again due to the lack of available circulating current to keep the body diode conducting. Therefore, the $T_d(min)$ and $T_d(max)$ values, which depend on circuit element values and the system operating conditions, are very important. To achieve ZVS, the actual switch deadtime $T_d(ZVS)$ should be selected to fall between these two values:

$$T_d(min) \leq T_d(ZVS) \leq T_d(max)$$  \hspace{1cm} (3-1)

In some cases, however, the inductive energy stored in the freewheeling path is not sufficient to fully discharge $C_{oss}$ and achieve ZVS for the switch that is turning on. In this situation, the device $C_{oss}$ may be partially discharged such that $V_{DS}$ is reduced from the input bus voltage to a minimum value $V_{DS(min)}$ that is greater than 0 V. This scenario is shown in Figure 3-2. Even though ZVS is not achieved in this condition, turning the device on while $V_{DS}$ is lower than the input voltage is not without benefit. When this occurs, the turn-on switching event is not lossless, but the loss is reduced compared to the hard-switched condition. In such cases, it is important to turn the device on at the lowest voltage point (i.e., the valley point) in order to minimize the turn-on switching loss. Such switching cases are called “valley-switched” transitions, in contrast to full-ZVS transitions, for which the turn-on switching loss is almost zero. Therefore, particularly at light loads when insufficient energy is available for realizing ZVS, the valley-switching approach may be considered to minimize the turn-on switching loss.
In section 4.6.2 of this dissertation, adjusting the deadtime values to implement valley-switching is briefly discussed.

It is well known that the efficiency of the PSFB converter is strongly influenced by the achievement of ZVS. To ensure optimum efficiency, ZVS must be maintained across a broad operating envelope and especially at the operating conditions that are most commonly encountered in practice. Achievement of ZVS is determined by the combination of a large number of factors, including component parameter values, parasitic parameter values, switching deadtimes, and the converter operating conditions such as the output power level. In order to effectively optimize the system performance for a practical converter design, some means of predicting ZVS is needed during the design process. The next section of this dissertation provides an analytical model that predicts the achievement of ZVS for both the leading and lagging switches based on a set of values that are possible to determine or estimate at design-

Figure 3-2: Example of $V_{DS}$ waveform during an incomplete $C_{oss}$ discharge.
time. This model can be used to identify and implement an optimization strategy for a particular PSFB converter design, even before a prototype is constructed and evaluated.

3.3. Analytical Treatment of The ZVS Mechanism

Historically, the resonant inductor value and the switching deadtime values have been the primary parameters employed to adjust the ZVS mechanism within the PSFB topology. Both parameters have a significant influence over the ZVS mechanism. The resonant inductor provides the required energy to extend the ZVS region to low output power levels, while a suitable deadtime is needed to provide the required interval to discharge the switch $C_{oss}$ for ZVS. However, the designer needs to be aware of the collective interaction of these and other parameters in order to properly optimize the ZVS mechanism. For example, the effect of switching deadtime on efficiency can be different for the lagging leg and leading leg switches. Another potential concern is that a large resonant inductor, as a side effect, may increase conduction losses due to increased circulating current during the freewheeling interval. Another effect that is often neglected in analytical treatments is the presence of losses associated with charging and discharging the MOSFET $C_{oss}$. Some studies [61]-[64] have revealed that the process of charging and discharging $C_{oss}$ involves a hysteresis effect, which implies that even full-ZVS switching transitions can incur losses.

To accurately model the ZVS mechanism, all these factors must be considered, not just the resonant inductor value and the switching deadtime values. It is particularly important that the MOSFET output capacitance be represented properly. It is well known that the intrinsic output capacitance of a MOSFET shows a nonlinear dependence on the applied drain-source voltage, $V_{DS}$. In order to simplify modeling of MOSFETs, this capacitance is sometimes represented in the literature by an energy-equivalent capacitance. An energy-equivalent
capacitance, $C_{E, equ}$, is a linear capacitor that stores the same amount of energy as the nonlinear MOSFET $C_{oss}$ at a given drain-source voltage, i.e.,

$$C_{E, equ}(V_{DS}) = \frac{2 \times E_{oss}(V_{DS})}{V_{DS}^2} = \frac{2 \int_0^{V_{DS}} \nu \times C_{oss}(\nu) d\nu}{V_{DS}^2}$$  \hspace{1cm} (3-2)$$

$C_{E, equ}$ is often used in the literature when modeling the MOSFET $C_{oss}$ for ZVS analysis [45][64][66]. However, Kasper et al. [67] recently showed that using a charge-equivalent capacitance, $C_{Q, equ}$, is a better approach when studying the ZVS mechanism. A charge-equivalent capacitance is a linear capacitor that stores the same amount of charge as the nonlinear MOSFET $C_{oss}$ at a given drain-source voltage, i.e.,

$$C_{Q, equ}(V_{DS}) = \frac{Q_{oss}(V_{DS})}{V_{DS}} = \frac{\int_0^{V_{DS}} C_{oss}(\nu) d\nu}{V_{DS}}$$  \hspace{1cm} (3-3)$$

In this dissertation, the $C_{Q, equ}$ representation is employed for representing the MOSFET nonlinear output capacitance.

All these factors point to the complexity of the ZVS mechanism in the PSFB converter. Fortunately, it is possible to create a simplified model to quantitatively predict the parameter values for which ZVS will be achieved in a given design. Such a model provides a means for evaluating the trends and tradeoffs that should be collectively considered when optimizing the PSFB converter for efficiency. However, this modeling effort must be performed separately for the leading and lagging switches, since the circuit elements involved in the ZVS process differ in these two cases. An analytical treatment of the ZVS mechanism for each of these switch sets is presented in sections 3.3.1 and 3.3.2.
3.3.1. Lagging Switch ZVS Model

This subsection details a theoretical formulation that describes the behavior of the ZVS mechanism for the lagging switches of the PSFB converter. With respect to the waveforms shown in Figure 2-2, time interval \([t_4 \, t_5]\) corresponds to the lagging switch \(C_{oss}\) discharging interval when the current commutates from \(Q_1\) to \(Q_3\). It should be noted that there is an identical transition that occurs in the opposite fashion – from \(Q_3\) to \(Q_1\). Since this second transition is identical to the first, it is not detailed here. For the \(C_{oss}\) of \(Q_3\) to be fully discharged during the \([t_4 \, t_5]\) interval, the energy stored in the resonant tank at \(t_4\) must be used to swing the lagging leg mid-point voltage from the positive DC bus rail to the negative DC bus rail. This implies that the output capacitance of \(Q_1\) must be charged to the DC bus voltage, and the output capacitance of \(Q_3\) must be discharged to zero volts. If this occurs, then \(Q_3\) can be turned on under ZVS at \(t_5\).

Immediately prior to time \(t_4\), the top two switches (\(Q_1\) and \(Q_2\)) are conducting, and freewheeling current circulates in the primary path. The transformer primary winding is shorted out at the beginning of this interval. Thus, the output inductor and inductive elements of the transformer do not contribute any inductive energy to the ZVS mechanism for the lagging switches. Instead, the resonant inductor \(L_r\) is the only source of inductive energy available for

\[
\begin{align*}
&\text{Figure 3-3: The equivalent circuits for a lagging switch } C_{oss} \text{ discharging interval } [t_4, t_5].
\end{align*}
\]
ZVS realization of these switches. Thus, the equivalent circuit that is in effect during this interval is shown in Figure 3-3. This circuit consists only of the resonant inductor and a charge-equivalent capacitor that represents the effective value of two MOSFETs ($Q_1$ and $Q_3$). By solving the equivalent circuit of Figure 3-3, the minimum required deadtime $T_{d(min)}$ for completing this transition of charge can be derived as:

$$T_{d,lag}(\text{min}) = \frac{1}{\omega_1} \times \sin^{-1} \left( \frac{V_{in}}{\sqrt{\frac{L_r}{2 \times C_{Q,\text{equ}} \times I_{Lr1}}}} \right)$$

(3-4)

where $V_{in}$ is the input DC voltage, $L_r$ is the resonant inductor, $C_{Q,\text{equ}}$ is the charge-equivalent capacitance of the switch output capacitance at the DC input voltage, $\omega_1$ is the natural frequency of the resonant tank, and $I_{Lr1}$ is the resonant inductor current at the start of this transition (i.e. $t_4$).

The resonant tank natural frequency is found to be:

$$\omega_1 = \frac{1}{\sqrt{2 \times C_{Q,\text{equ}} \times L_r}}$$

(3-5)

The initial condition for the resonant inductor current can be estimated as follows:

$$I_{Lr1} \approx \frac{I_o}{n} + \left[ \frac{1 - D_{eff}}{4 \times n \times L_o \times f_{sw}} \right] \times V_o + i_{m,max}$$

(3-6)

where $I_o$ is the output current of the converter, $V_o$ is the output voltage of the converter; $f_{sw}$ is the switching frequency, $n$ is the transformer primary to secondary turns ratio, $L_o$ is the output inductor value, $i_{m,max}$ is the maximum current of the magnetizing inductance $L_m$, and $D_{eff}$ is the effective duty cycle. $D_{eff}$ and $i_{m,max}$ have already been defined in expressions (2-1) and (2-6), respectively.

When the voltage across $Q_3$ drops to zero due to resonant action, the body diode conducts and the ZVS opportunity window begins, as illustrated in Figure 3-1. However, as soon as the
body diode starts conducting, a reverse voltage, which is almost equal to the input voltage in amplitude, is applied to the resonant inductor. This causes the resonant inductor current \(i_{Lr}\) to rapidly decrease toward zero, as shown in Figure 2-2 during the time interval of \([t_5 \ t_7]\). When \(i_{Lr}\) reaches zero at \(t_7\), the body diode of \(Q_3\) goes through reverse recovery and then enters into the blocking mode again. If \(Q_3\) is not turned on by the end of the reverse recovery time, the output capacitance of \(Q_3\) starts charging up to the input bus voltage again and the ZVS opportunity is lost. By considering these factors, the maximum acceptable deadtime, \(T_{d(max)}\), for achieving ZVS for the lagging leg switches can be formulated as:

\[
T_{d,\text{lag}}(\text{max}) = T_{d,\text{lag}}(\text{min}) + \frac{L_r}{V_{\text{in}}} \sqrt{l^2_{Lr1} - \frac{2 \times C_{Q,\text{equ}} \times V_{\text{in}}^2}{L_r}} + T_{r,\text{bd}} \quad (3-7)
\]

where \(T_{d,\text{lag}}(\text{min})\) is the minimum required deadtime value for the lagging switch and \(T_{r,\text{bd}}\) is the reverse recovery time of the body diode of the MOSFET. The intrinsic P-N body diode in a SiC MOSFET has reverse recovery time on the same order as the deadtime values commonly used in SiC-based converters. The reverse recovery time for Si and Superjunction MOSFETs is even larger [68]. Therefore, it is important to take this reverse recovery time into account in order to get an accurate estimation of the maximum acceptable deadtime for the lagging switches. Although accurate determination of the reverse recovery time can be tedious [68]-[70], the designer can usually obtain a reasonable approximation of this parameter using the device datasheet.

It should be noted that the lagging leg switches are susceptible to losing ZVS at light load. This is because the only source of resonant energy for this transition is the energy stored in the resonant inductor \((L_r)\), which ultimately is a function of the load current. This highlights the importance of \(L_r\) as a design parameter for the PSFB converter, particularly for light load conditions. Also, due to the small capacitive and inductive elements involved, the lagging leg
transition happens more quickly than the leading leg transition. This implies that the window of
ZVS opportunity is more constricted for the lagging leg switches compared to the leading leg
switches, which makes deadtime selection for these switches more critical as well.

3.3.2. Leading Switch ZVS Model

This subsection details a theoretical formulation that describes the behavior of the ZVS
mechanism for the leading switches of the PSFB converter. With respect to the waveforms
shown in Figure 2-2, time interval \([t_1 \ t_2]\) corresponds to the leading switch \(C_{oss}\) discharging
interval when the current commutates from \(Q_4\) to \(Q_2\). It should be noted that there is an identical
transition that occurs in the opposite fashion – from \(Q_2\) to \(Q_4\). Since this second transition is
identical to the first, it is not detailed here. For the \(C_{oss}\) of \(Q_2\) to be fully discharged during the
\([t_1 \ t_2]\) interval, the energy stored in the resonant tank at \(t_1\) must be used to swing the leading leg
mid-point voltage from the negative DC bus rail to the positive DC bus rail. This implies that the
output capacitance of \(Q_4\) must be charged to the dc bus voltage, and the output capacitance of \(Q_2\)
must be discharged to zero volts. If this occurs, then \(Q_2\) can be turned on under ZVS at \(t_2\).

During the \([t_1 \ t_2]\) interval, the converter is transitioning from a power transfer period to a
freewheeling period. Since the transformer primary winding is not yet shorted out during this
transition, the secondary-side elements of the converter are reflected to the primary side. The
equivalent circuit that is in effect during this interval is shown in Figure 3-4. As shown in this
figure, the output inductor \(L_o\) takes part in the resonant transition for the leading leg and
contributes a large portion of the required energy. The leakage inductance, \(L_{lk}\), and the
magnetizing inductance, \(L_m\), of the transformer contribute some energy as well, although at a
smaller scale. During this transition, the secondary diodes also start commutating the output
current; therefore, the junction capacitance of the two secondary diodes is also involved. The
A linear charge-equivalent capacitance model is employed to represent the nonlinear capacitance of these devices in the equivalent circuit of Figure 3-4. In this circuit, \( C_p \) represents the linear equivalent capacitance of one secondary diode. The prime superscript on each element name in the circuit of Figure 3-4 indicates that the associated element is reflected to the transformer primary. Finally, the parasitic interwinding capacitance of the transformer, \( C_T \), is also involved in this transition. From the AC signal standpoint, this element appears in parallel with the capacitance of the switches, each of which is represented in charge-equivalent form as \( C_{Q,equ} \).

The ZVS transition process for the leading leg follows the same concept as previously discussed for the lagging leg. However, as seen in the equivalent circuit of Figure 3-4, the leading leg transition involves more elements than the lagging leg transition and, therefore, is more complex. It should be mentioned that the equivalent circuit shown in Figure 3-4 is only valid for the continuous-conduction-mode (CCM) operation of the PSFB converter. Modeling the ZVS mechanism for the leading leg in discontinuous-current mode (DCM) requires a separate treatment, which is not presented here. Also, as previously stated, the blocking capacitor \( C_b \) is often selected such that its impedance is negligible at typical frequencies of the converter. For this reason, especially in the transition period represented by the equivalent circuit of Figure 3-4, the effect of \( C_b \) can be safely neglected to simplify the analysis.

**Figure 3-4:** The equivalent circuits for a leading switch \( C_{oss} \) discharging interval \([t_1, t_2]\).
The equivalent circuit of Figure 3-4 can be solved to obtain $T_d(min)$ for the leading leg. Unfortunately, due to the complexity and the large number of elements involved, deriving a closed-form time-domain expression for the minimum required deadtime is very involved. However, the switch voltage in the $S$-domain can be readily derived from the equivalent circuit of Figure 3-4, which can then be leveraged to obtain $T_d(min)$. The leading switch voltage during this transition in the $S$-domain can be expressed as:

$$V_{sw,lead}(s) = \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s(b_4 s^4 + b_2 s^2 + b_1 s)}$$  \hspace{1cm} (3-8)

The coefficients of equation (3-8) are given as:

$$a_4 = 2(2C_{Q,\text{equ}} + C_T)C_D' L'_o L_{lk} L_m V_{in}$$

$$a_3 = -2C_{D,\text{equ}}' L'_o L_{lk} L_m I_{p,\text{max}}$$

$$a_2 = Vin\{(2C_{Q,\text{equ}} + C_T)(L'_o L_{lk} + L'_o L_M + L_{lk} L_m) + 2C'_D L'_o L_m\}$$

$$a_1 = -(I_{m,max} + I'_V)L'_o L_m + (L'_o + L_M)L_{lk} I_{p,\text{max}}$$

$$a_0 = L_m V'_o$$  \hspace{1cm} (3-9)

$$b_4 = 2(2C_{Q,\text{equ}} + C_T)C_D' L'_o L_{lk} L_m$$

$$b_2 = 2 \left( C_{Q,\text{equ}} + C'_D + \frac{C_T}{2} \right) L'_o L_m$$

$$+ (2C_{Q,\text{equ}} + C_T)(L'_o + L_m)$$

$$b_1 = L_m + L'_o$$

where $L_m$ is the transformer magnetizing inductance; $L_{lk}$ is the transformer leakage inductance; $L'_o$ is the output inductor reflected to the primary side; $C_{Q,\text{equ}}$ is the charge-based equivalent capacitance of the MOSFET $C_{oss}$; $C'_D$ is the charge-based equivalent capacitance of the secondary diode junction capacitance reflected to the primary side; $C_T$ is the parasitic interwinding capacitance of the transformer; $I_{p,\text{max}}$ is the maximum primary current; $I'_V$ is the peak output
inductor current reflected to the primary side, and $V'_o$ is the output voltage reflected to the primary side. In this work, MATLAB is utilized to determine the inverse Laplace transform of equation (3-8). The resulting expression is solved for the time variable, $t$, that results in zero switch voltage in the time domain (i.e. $V_{sw, lead}(t) = 0$). This process can be used to identify $T_{d,lead}(min)$, the first time at which the switch voltage becomes zero.

The complexity of this transition also makes it difficult to analytically derive the maximum acceptable deadtime $T_{d,lead}(max)$ for the leading leg. However, the maximum acceptable deadtime is much less important for the leading leg compared to the lagging leg. This is due to several factors. First, due to the reflection of the load current to the primary side during the leading leg transition, there is far more available energy for driving this transition. This means that it is much less likely that the leading switches will lose ZVS at light loads compared to the lagging switches. Indeed, ZVS is generally maintained for the leading leg at very low output power levels [71][72]. Second, due to the large capacitive and inductive elements involved in this transition, the leading leg transition happens more slowly than the lagging leg transition. This implies that the window of ZVS opportunity for the leading leg is primarily constrained by the minimum value rather than the maximum value. For these reasons, it is expected that $T_{d,lead}(max)$ is not a parameter of sensitivity for most practical PSFB implementations. Therefore, analytical treatment of $T_{d,lead}(max)$ for the leading leg is not presented here.

3.4. ZVS Achievement Trends and Observations

In section 3.3, the impact of timing between switching commands for the leading and lagging switches was studied, and a modeling framework was introduced to assist in quantifying these dependencies. Expressions (3-4), (3-7), and (3-8) can be leveraged to obtain the range of
acceptable deadtime values (for either leading or lagging switches) that can realize ZVS under different operating conditions and/or different system parameter values. This section utilizes this modeling framework to predict ZVS achievement trends due to the collective influence of these factors. The plots presented in this section are based on the system parameters of the 10 kW PSFB prototype converter detailed in CHAPTER 4. The experimental validation of these trends are also presented in CHAPTER 4.

3.4.1. ZVS Trends: Lagging Switches

Equations (3-4) and (3-7) can be used to predict the lower and upper deadtime boundaries, respectively, for the attainment of ZVS by the lagging switches. These models can

![Figure 3-5: ZVS achievement trends of lagging switches with different resonant inductor values and across a range of different deadtimes and output powers.](image-url)

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be leveraged to study the interdependence of ZVS attainment with regard to different system parameters. Figure 3-5 provides such a comparison for the lagging leg switches across a range of resonant inductor values, deadtime values, and output power levels. In this figure, deadtime values that are predicted to achieve ZVS for the lagging leg switches are depicted by the shaded regions, which are bounded on the top and bottom by the analytically derived minimum and maximum deadtime values. As expected, increasing the resonant inductor value, \( L_r \), leads to broader deadtime regions that realize ZVS for the lagging switches. Moreover, increasing the resonant inductor value, \( L_r \), also extends the ZVS region to lower output power levels because more energy is available to fuel the resonant transition of the device output capacitances. Also, as the converter output power increases, the lower boundary of the deadtime region converges to approximately the same value for all \( L_r \) values considered. This implies that the resonant inductor value is not a critical parameter for determining the lower boundary of the ZVS window for the lagging switches, especially at high output power. On the other hand, as the output power increases, the upper deadtime boundary increases in a consistent fashion. This implies that the resonant inductor value is a critical parameter for determining the upper boundary of the ZVS window for the lagging switches.

The result of a complementary analysis that demonstrates the effect of MOSFET output capacitance on the ZVS behavior of the lagging leg is presented in Figure 3-6. As before, deadtime values that are predicted to achieve ZVS for the lagging leg are depicted by the shaded regions, which are bounded on the top and bottom by the analytically derived minimum and maximum deadtime values. As expected, increasing the output capacitance of the device limits the extent of the ZVS range at light load due to the need for increased energy to fuel the transition of the device output capacitances. Moreover, the minimum deadtime needed to fully
transition the switch output capacitances at a given output power level increases with the output capacitance value. This trend is also expected because the charge/discharge time for the leg midpoint will be proportional to the total capacitive load, assuming that the resonant inductor is sufficiently large to behave like an ideal current source over this timescale. Finally, in contrast to the resonant inductor, the output capacitance of the MOSFET affects both the minimum and maximum deadtime values across a wide range of operating conditions. However, it appears that the minimum deadtime is influenced more strongly than the maximum deadtime by the device output capacitance, at least for the specific converter configuration studied here.

Figure 3-6: ZVS achievement trends of lagging switches with different charge-equivalent output capacitance values and across a range of different deadtimes and output powers.
Equation (3-8) can be used to predict the lower deadtime boundary for attainment of ZVS by the leading switches. Figure 3-7 provides the result of this analysis for the leading leg switches across a range of deadtime values and output power levels. It is noted that the upper deadtime boundary is not predicted for the leading switches by the theoretical derivation in section 3.3.2. It should also be mentioned that, unlike the lagging leg case, Figure 3-7 does not demonstrate the effect of sweeping the resonant inductor value, $L_r$. This sweep is omitted because the resonant transition of the leading leg is not influenced by the value of the resonant inductor. As before, the deadtime values that are predicted to achieve ZVS for the leading leg...
switches are depicted by the shaded region, which is bounded on the bottom by the analytically derived minimum deadtime values. It is noted that this figure only shows the predicted ZVS timing parameters in CCM (continuous-current mode) operation, which extends to approximately 4% of the rated output power level for the example converter under study. It is also possible for the leading leg switches to achieve ZVS in DCM [44], but this is not considered in the present study. Due to the contribution of the output inductor, the leading leg can achieve ZVS at very low output power levels (even as low as the DCM boundary) provided that sufficient deadtime is provided. One other salient observation can be made from Figure 3-7. In section 3.3.2 it was claimed that the leading leg requires a longer minimum deadtime value than the lagging leg, due to the larger inductive and capacitive elements involved in the resonant transition. This prediction is borne out by comparing the results of Figure 3-5 and Figure 3-7. Figure 3-5 demonstrates that the lagging leg needs as little as 10-15 ns to complete the resonant transition at 10 kW output power. Figure 3-7, on the other hand, demonstrates that the leading leg needs a minimum of 50 ns to complete the resonant transition at this power level.

The result of a complementary analysis that demonstrates the effect of MOSFET output capacitance on the ZVS behavior of the leading leg is presented in Figure 3-8. As before, deadtime values that are predicted to achieve ZVS for the lagging leg are depicted by the shaded regions, which are bounded on the bottom by the analytically derived minimum deadtime values. As in the case of the lagging leg, increasing the MOSFET output capacitance generally results in an increased minimum deadtime value for achieving ZVS. As in the case of the lagging leg, this trend is also dependent on the output power level. The impact of the MOSFET output capacitance is more pronounced at light load, due to the reduced energy available to fuel the resonant transitions in this load range. However, in contrast to the lagging leg case, ZVS can
still be realized for the leading leg switches at very low output power values, although very long deadtimes are required in this scenario.

This chapter presented a set of theoretical models that predict the ZVS behavior of the lagging and leading switches of the PSFB converter. As demonstrated herein, these models can be utilized to evaluate the sensitivity of the ZVS mechanism to variations in system parameter values and operating conditions. In the next chapter, the predictions of this model and the associated ZVS behavior trends will be empirically validated and discussed in the context of practical converter design.
CHAPTER 4

EMPIRICAL EVALUATIONS, EFFICIENCY TRENDS, AND APPLICATION DISCUSSIONS

4.1. Introduction

This chapter introduces the prototype PSFB converter that was designed and evaluated as part of this research. The ZVS model predictions and associated trends presented in CHAPTER 3 are empirically validated using this prototype converter. Attainment of ZVS for the leading and lagging switches directly affects the efficiency of the PSFB converter. This is especially important at elevated switching frequencies, as switching losses can make up a significant portion of the overall system losses if hard-switching occurs in this scenario. Therefore, the cumulative effect of the most important system parameters on the attainment of ZVS and the impact on system efficiency is considered in this chapter. Finally, this chapter presents a set of guidelines for tuning the ZVS mechanism in the context of practical converter design.

4.2. Prototype Converter Description

A prototype PSFB converter was designed and implemented in support of the analysis provided in this chapter. Specifically, this converter is utilized to validate the theoretical treatment of the ZVS mechanism provided in section 3.3 and to support the system parametric studies included in section 3.4. This prototype converter was originally designed to address the need for increased power density in datacenter applications, which is made possible by the commercial introduction of WBG semiconductors, particularly SiC MOSFET devices.
Introduction of these devices has led to the emergence of a newly proposed power architecture for datacenters. This new architecture exploits the characteristics of SiC MOSFETs in order to maximize the efficiency and power density of converters in this environment. Before presenting the details of the prototype PSFB converter, a short description of the newly proposed power architecture for datacenter applications is presented.

4.2.1. New Power Architecture for Datacenters

It is increasingly evident that datacenter energy costs are on the rise. While the server industry continues to make marginal improvements to system efficiency, this increased energy consumption is primarily a result of the immense escalation of cloud computing and social networking, rapidly increasing mobile activity, early implementation of cognitive computing, and a fast-growing expanse of structured and unstructured data [8][25]. In the U.S. alone, the annual cost of power to operate datacenters was $4.5 billion in 2007 [73]. This figure has increased every year since 1980 [74] and is projected to continue increasing very rapidly in the coming years [75]. In fact, these projections may have been underestimated, as many of the largest suppliers in the server market are experiencing challenges meeting the exceedingly high demand. As a consequence, there is tremendous economic and regulatory pressure to increase the performance of power subsystems and power distribution within the datacenter environment. The recent commercialization of WBG semiconductor technology provides a significant opportunity to improve the performance of these systems. However, a significant change to today’s power distribution architecture is required to reap the full benefits of WBG-based power conversion.
The majority of servers produced today are based on a power architecture similar to that of Figure 4-1(a) [76][77]. This architecture is built around an array of Power Supply Units (PSUs) that produce 2 kW or less at 12 VDC. This 12 VDC rail is distributed throughout the rack or drawer to point-of-load (POL) converters, which further regulate to voltages required by processors, memory, and I/O. In addition, an upstream Uninterruptable Power Supply (UPS) is necessary to ensure system reliability in the presence of utility power disturbances. This architecture has several disadvantages that accrue ultimately from the limitations of the semiconductors used to implement the PSU. The first challenge is that the input voltage that can be used with this architecture is limited; 220 VAC is most commonly used. The primary reason for this limitation is the use of 600 V Silicon MOSFETs in the power factor correction (PFC) and DC-DC stages of the PSU. This limits the intermediate bus voltage to around 400 V in

\[\text{(a)}\]

\[\text{(b)}\]

Figure 4-1: (a) Today’s server power architecture; (b) The new proposed server power architecture leveraging WBG devices.

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consideration of derating requirements. Moreover, if the PFC is to be operated in boost mode, which has significant advantages for limiting the size of the required EMI filter, this imposes an upstream limit on the input voltage that can be supported. This input voltage limitation is disadvantageous because it increases the conduction losses upstream of the server PSU, and it makes it difficult to implement this architecture worldwide without the use of additional transformers or an external UPS to down-convert to the PSU’s limited input range. The second challenge with this traditional architecture is that it results in significant conduction losses within the rack or drawer. Due to the cumulative power requirement of the processor cores within the rack, the 12 VDC rail is generally required to supply current in excess of 100 A. Thus, a significant portion of the loss budget for this architecture is allocated to conduction losses. Higher intermediate voltages, such as 48 VDC, have been proposed and could offer some improvements. However, this approach is not likely to offer sufficient advantage to offset the increasing demand for power consumption that the industry currently faces. The third challenge with the traditional architecture is the density of the final system packaging, which is convolved with the other two challenges previously discussed. Two of the main factors driving the size of these systems are the requirement for an external line-frequency UPS, and the size of the EMI and other filtering components required to meet offline conducted emission regulations. Both the input voltage limitation and the conduction loss problem in this architecture could be readily addressed by increasing the voltage of the intermediate DC bus. However, until the commercial launch of WBG devices, the only viable alternative to Silicon MOSFETs was Silicon IGBTs. Implementing this architecture based on Silicon IGBTs would limit the achievable switching frequency and drive towards a mechanically larger solution.
The proposed architecture [26] shown in Figure 4-1(b) addresses all of these challenges simultaneously through the adoption of 1.2 kV SiC MOSFETs in the PSU design. The blocking voltage supported by these devices enables the elevation of the intermediate bus voltage to 750 VDC with sufficient derating to ensure long-term reliability. This change addresses the first challenge by enabling input voltages up to 480 VAC or 700 VDC, while enabling the front-end PFC converter to operate in boost mode, and thereby retaining the size advantage associated with the design of the EMI filter for a continuous conduction operation topology. This makes it possible to support universal worldwide input voltages, including high voltage DC (HVDC) in Europe and Canada, as well as 480 V, 3-phase, high voltage AC (HVAC) in the United States. Universal input can also reduce the need for upstream transformers, which incur further loss. The proposed architecture addresses the second challenge by elevating the distribution voltage used within the rack from 12 VDC to 350 VDC. This will yield a significant reduction in conduction losses within the rack, at the expense of a modest increase in the POL converter loss, which will likely need to be a 2-stage converter in this architecture. The proposed architecture also addresses the third challenge because WBG devices, such as 1.2 kV SiC MOSFETs, natively support extremely high-frequency operation, while retaining very low losses compared to alternative devices such as Silicon IGBTs at these voltage levels. This provides the ability to significantly reduce the volume of the magnetic and filtering components compared to lower-frequency alternative designs. Lastly, Li-ion batteries are employed in this architecture in place of an external UPS. This design provides increased energy density that can be located closer to the server and can operate off the intermediate bus voltage. The ability to eliminate the external UPS is one of the major advantages of the proposed architecture for packaging, density, efficiency, and cost reasons [78]. Nevertheless, it should be mentioned that present isolated DC-
DC converters of this stage, operating at $50 - 100 \text{ kHz}$, typically have a power density of less that $50 \text{ W/in}^3$ [79].

4.2.2. The Prototype PSFB Converter

Figure 4-2 presents a picture of the prototype PSFB converter implemented in support of this study. This prototype converter utilizes SiC power semiconductors (i.e. MOSFET and diodes) and is designed to provide a continuous output power of 10 kW at 350 VDC from an input bus of 750 VDC. These voltage specifications were derived from the requirements of the new datacenter power distribution architecture presented in Figure 4-1(b) and discussed in subsection 4.2.1. The detailed specifications of this converter are presented in Table 1. In this converter, the primary-side switches (i.e. switches $Q_1$, $Q_2$, $Q_3$, and $Q_4$ of the schematic of Figure 2-1) are implemented using 20 A, 1.2 kV, 80 mΩ SiC MOSFETs, part number
On the secondary side, each SiC diode position (i.e. $D_1$, $D_2$, $D_3$, and $D_4$) in the schematic of Figure 2-1) consists of two paralleled 20A, 1.2 kV SiC Schottky diodes, part number LSIC2SD120A20 from Littelfuse [81]. This prototype converter employs a 4-layer mainboard, with the top and bottom layers used for power routing and the internal layers used for controller feedback and gate-drive signal routing. The control stage is mounted on a separate daughterboard and is based on the UCC28950 dedicated phase-shift-modulation controller IC from Texas Instruments [82]. This controller implements two-loop feedback control with an outer voltage loop and an inner current loop. The inner loop implements peak-current-mode control (PCMC), which is particularly appealing to industrial applications due to its superior dynamic response and inherent over-current protection.
This design also incorporates custom-designed isolated gate-drive modules to drive the primary side SiC MOSFETs. The implementation of this gate drive module is shown in Figure 4-3.

One additional notable feature of this converter, which is shown in Figure 4-2, is its unique thermal management structure. To improve the performance of the forced air system required for thermal stability, a common heatsink is utilized for all primary and secondary power semiconductors. This “heatsink rail”, which is shown in Figure 4-4, is an extruded aluminum structure that features internal fins to reduce the thermal resistance from the heatsink to ambient. A centrifugal blower, as also shown in Figure 4-4, is used to inject a high volume of air into this rail for cooling. This unique structure not only helps to reduce the overall size of the system but also leads to more efficient thermal management, compared to the use of separate heatsinks for each semiconductor in the system. This design also improves the thermal balance between
semiconductor devices operating with the same role, thereby marginally reducing the risk of thermally-induced semiconductor failure. Moreover, this heatsink rail can be easily converted into a liquid-based heat exchanger by sealing the ends and using a circulating chiller to pump cooling liquid through the tube.

4.3. Empirical Evaluation Procedure

As part of this research, the prototype converter described in section 4.2.2 was subjected to extensive empirical evaluation. This evaluation procedure was segmented into two major phases.

During the first phase of the empirical evaluation procedure, the prototype converter was leveraged to validate the theoretical deadtime boundaries ($T_d(\text{min})$ and $T_d(\text{max})$) that were

Figure 4-5: An example showing $V_{DS}$ waveform of a lagging switch in order to capture corresponding $T_d(\text{min})$ and $T_d(\text{max})$. The corresponding deadtime was set large enough to be able to capture $T_d(\text{min})$ and $T_d(\text{max})$. 

$L_r=10 \ \mu\text{H}$

$P_{\text{out}}=3.2 \ \text{kW}$
derived in section 3.3 and the ZVS trends that were discussed in section 3.4. These validation experiments were performed across a test matrix that encompasses variation in parameter values for critical system components including $L_r$ and $C_{Q,eq}$ as well as variation in the operating conditions for the converter. It should be noted that the value of $L_r$ was varied by winding physically different inductor values, which were subsequently characterized with an LCR meter. The value of $C_{Q,eq}$ was “varied” by placing a set of surface-mount ceramic capacitors across the drain and source terminals of the SiC MOSFET to emulate variation in the intrinsic output capacitance of the device. The converter operating load was adjusted by changing the impedance of a resistive load bank attached to the converter output terminals. All experiments were conducted with the input and output voltage levels given in Table 1, and the converter was operated under closed-loop control at all times. The resulting test matrix was executed twice – once for the lagging leg deadtime evaluation, and once for the leading leg deadtime evaluation. For all configurations considered, the controller was configured to provide a very long deadtime during operation (approximately 600 ns). This deadtime value is not intended to demonstrate the optimal performance of the converter. Instead, this deadtime value is selected to intentionally delay the switching event until after the end of the ZVS opportunity window. This permits both the fall and subsequent rise of the switch $V_{DS}$ waveform to be clearly observed. The result of this procedure is shown by experimental example for the lagging leg in Figure 4-5. This example was captured at an output power level of 3.2 kW, and with a resonant inductor value of 10 $\mu$H. In this configuration, the value of $T_d(min)$ is shown to be approximately 35 ns from the start of the $V_{DS}$ waveform drop, as evidenced by the cursors in Figure 4-5. In a similar fashion, the value of $T_d(max)$ is shown to be 151 ns for this configuration. This is the time that $V_{DS}$ rises above a user-specified threshold voltage (here considered to be 1 V). This empirical procedure was
performed once for each considered configuration in the test matrix, and the observed values for $T_d(min)$ and $T_d(max)$ were recorded for all cases. A comparison between the results of this procedure and the predictions of the theoretical model will be presented in section 4.4.1 for the lagging leg and in section 4.4.2 for the leading leg.

During the second phase of the empirical procedure, the efficiency of the converter was evaluated across a wide set of conditions. In light of the demonstrated sensitivity of the PSFB topology to deadtime values, the test matrix created for this phase of the evaluation incorporates variation in the deadtime values enforced by the controller during operation. It should be noted that the same deadtime value is utilized for the lagging leg and the leading leg for each experiment included in this phase. In addition to sweeping the deadtime values enforced by the controller, this test matrix also incorporates the same variations in parameter values for critical system components and in the operating conditions that were described for the first phase of this evaluation. During the second phase of this evaluation, the system efficiency of the converter was captured using a Tektronix PA4000 power quality analyzer (PQA), which is shown in Figure 4-6. All efficiency measurements include the contribution of the power consumed by the heatsink rail blower as well as the gate-drive auxiliary power supply. Considerations were also made to account for the temperature dependence of certain loss mechanisms within this
converter. For example, before the efficiency was captured at each operating point, the converter was allowed to operate for approximately 10 minutes in order for the system to reach thermal stability. After confirming thermal stability using an infrared camera, the efficiency value reported by the PQA instrument was averaged for a few minutes of continuous operation to obtain a final efficiency estimate. This procedure was repeated for each considered testing configuration. The results of this empirical analysis are presented in section 4.5.

4.4. ZVS Model Validation

This section provides empirical validation of the theoretical ZVS models derived in chapter 3 of this dissertation. This validation utilizes experimental results obtained during the operation of the prototype PSFB converter described in section 4.2.2. This section is organized according to the arrangement of the empirical procedures outlined previously. sections 4.4.1 and 4.4.2 provide empirical validation for the ZVS model predictions associated with the lagging leg switches and the leading leg switches, respectively.

4.4.1. ZVS Model Validation for Lagging Switches

Utilizing the procedure outlined in section 4.3, the start and end of the ZVS opportunity window can be measured empirically. These measured results provide a clear means to evaluate the accuracy of the timing predictions offered by Equations (3-4) and (3-7) for the lagging switches. This procedure can also be used to verify the analytical ZVS trends presented in Figure 3-5 and Figure 3-6 for the lagging switches. In Figure 4-7, the ZVS trends previously shown in Figure 3-5 are compared to experimental results. In this figure, the empirical measurements for the start and end of the ZVS opportunity window are indicated by the locations of the asterisks. As shown in this figure, the experimental results are in good agreement with the predictions of the analytical model in nearly all cases. However, for each $L_r$ case in this figure, at low powers
where the ZVS opportunity window becomes narrower, a slight difference is observed between the theoretical predictions and the experimental results. In other words, as the output power decreases, the ZVS opportunity window becomes smaller and $T_{d}(\text{min})$ ends sooner than what the model predicts. This shows that in reality, the value of stored energy predicted by the model for full discharging of the switch capacitances is not sufficient at low power levels.

This discrepancy can likely be attributed to the presence of subtle loss factors that are often neglected when calculating the required minimum energy for full discharging of the switch capacitances. One obvious loss factor is the resistance of the discharge path. This discharge path for the lagging switch $Q_3$ is shown in Figure 2-7. In this figure, the resistance of the elements involved in the path $V_{in}-C_{DS3}-L_r-D_{P1}$ dissipates some of the stored energy in $L_r$. At lower output
powers, the amount of stored energy becomes smaller and the energy dissipation becomes comparable to this stored energy. Therefore, this dissipation contributes to losing ZVS at power levels slightly higher than what is predicted by the model. A less obvious factor is the charging/discharging loss (also known as the hysteresis loss) of the $C_{Q_{equ}}$ capacitance itself. In fact, it has been shown that charging and discharging a MOSFET $C_{oss}$ is not a lossless process [63][64]. This important effect has recently been made known and its implications are not still clearly understood by many designers. More information about this phenomenon is presented within section 4.6.3.

Figure 4-8: Experimental ZVS trends of lagging switches with different charge-equivalent output capacitance values and across a range of different deadtimes and output powers. Asterisks correspond to experiments.
Similarly, in Figure 4-8, the ZVS trends previously shown in Figure 3-6 are compared to experimental results. In this figure, the empirical measurements for the start and end of the ZVS opportunity window are indicated by the locations of the asterisks. As in the previous case, the empirical results demonstrate good agreement with the predictions of the theoretical model. There is a modest discrepancy observed for the maximum deadtime boundary in all three cases considered, but the theoretical trend is clearly corroborated by the experimental results in all cases.

![Figure 4-9: Experimental ZVS trends of leading switches across a range of different deadtimes and output powers. Asterisks correspond to experiments.](image)
4.4.2. ZVS Model Validation for Leading Switches

The procedure described previously for the empirical observation of the ZVS opportunity window can also be applied for validation of the ZVS model associated with the leading leg. A comparison between the measured results for the leading leg and the timing predictions offered by Equation (3-8) and previously shown in Figure 3-7 is presented in Figure 4-9. In this figure, the empirical measurements for the start of the ZVS opportunity window are indicated by the locations of the asterisks. Across the entire load range of the converter, the experimental results demonstrate good agreement with the theoretical predictions from Equation (3-8).

Figure 4-10: Experimental ZVS trends of leading switches with different charge-equivalent output capacitance values and across a range of different deadtimes and output powers. Asterisks correspond to experiments.
Similarly, Figure 4-10 presents the experimental validation of the trends previously shown in Figure 3-8 for the leading leg switches with different charge-equivalent output capacitance values. As before, the empirical measurements for the start of the ZVS opportunity window are indicated by the locations of the asterisks in this figure. As in the previous case, the empirical results demonstrate good agreement with the predictions of the theoretical model presented in section 3.3.2 across all considered configurations of the converter.

4.5. Efficiency Trends and Observations

In this section, the collective influence of deadtimes, resonant inductor value, and output power level on the performance of the PSFB converter is investigated. In this analysis, contour plots are employed to present the efficiency of the converter as a function of multiple parameters. These contour plots provide a convenient means for visualizing and identifying quantitative trends and relationships between independent variables that may be difficult to observe in 2D and 3D efficiency plots. Such plots, as will be presented shortly, contain a lot of useful information that can be deciphered and leveraged to increase the efficiency of the system. Furthermore, the sensitivity of system efficiency to various system parameters can be easily visualized and analyzed using these plots. The results presented in this section are the outcome of the second phase of the empirical evaluation procedure described in section 4.3. For this analysis, the converter performance is evaluated in terms of its input-to-output efficiency as the primary figure of merit. One important contribution of this analysis is the identification of the impact of ZVS achievement on the realized efficiency of the converter. As will be shown, the maximum efficiency of the converter is observed under the conditions for which both switching legs are predicted to achieve ZVS.
Figure 4-11: Efficiency contour plots for $L_r=5\mu H$, sweeping output power and deadtime (assumed the same for all leading and lagging switches).

Figure 4-12: Efficiency contour plots for $L_r=10\mu H$, sweeping output power and deadtime (assumed the same for all leading and lagging switches).
Figure 4-13: Efficiency contour plots for $L_r=15\mu H$, sweeping output power and deadtime (assumed the same for all leading and lagging switches).

Figure 4-14: Efficiency contour plots for $L_r=20\mu H$, sweeping output power and deadtime (assumed the same for all leading and lagging switches).
Figure 4-11 to Figure 4-14 present a set of efficiency contour plots obtained for a set of experiments utilizing different resonant inductor values (i.e. \( L_r = 5\mu H \), \( L_r = 10\mu H \), \( L_r = 15\mu H \), \( L_r = 20\mu H \)). In each of these plots, the y-axis represents the range of deadtime values swept in the experiment; while the x-axis represents the range of output power level values swept in the experiment. The z-axis value, which is also indicated by the color map, represents the efficiency of each considered configuration. The theoretical deadtime boundaries, which were previously derived for both leading and lagging switches, are also overlaid on each contour plot to aid with visualization of the operating regions that are expected to achieve ZVS. With careful selection of deadtime values for the primary side switches, efficiency values approaching 97% are achievable for this prototype converter. Overall, by following the plots of Figure 4-11 to Figure 4-14, it is observed that increasing the resonant inductor value expands the peak efficiency region, and in general, provides better efficiency across a wider operating envelope. This observation can be made from the experimental results alone. However, the predictions of the ZVS model from section 3.3 provides otherwise unavailable insight into the reason that this trend exists. The observed expansion of the high-efficiency region is explained by the expansion of the overlap between the leading leg and lagging leg ZVS regions, as shown in the plots of Figure 4-11 to Figure 4-14. In other words, the measured efficiency of the converter is reduced in regions for which the ZVS model predicts that one of the switch sets will not achieve ZVS. However, this impact is incurred gradually as the operating point leaves the ZVS region, due to partial soft-switching and the resulting partial mitigation of turn-on switching losses. The insight gained by the identification of the ZVS boundaries is most pronounced in Figure 4-11 and Figure 4-14. In Figure 4-11, the ZVS region for the lagging switches is very small and shares little overlap with the ZVS region for the leading switches. This leads to the presence of a very small peak...
efficiency region at deadtime values around 100 ns. In Figure 4-14, the ZVS region for the lagging switches is quite large and shares a significant overlap with the ZVS region for the leading switches. This leads to a large peak efficiency region, which can be accessed from the triangle-shaped region of the operating envelope between deadtime values of 75 ns and 350 ns. One further observation can be made by following the regions that fall within both ZVS boundaries in Figure 4-11 to Figure 4-14. Following these regions from the smallest to the largest $L_r$ plots demonstrates no efficiency penalty at high power levels for large values of $L_r$, in contrast to some predictions [44][50][84]. These studies claim that the disadvantage of using large resonant inductor values is an increase in circulating current during the freewheeling intervals, which can increase conduction losses. However, within the ZVS boundaries in Figure 4-11 to Figure 4-14, this trend cannot be observed. For example, Figure 4-14, which corresponds to the largest considered $L_r$ value, shows increased efficiency within the ZVS boundaries at 10 kW output power compared to the same conditions in Figure 4-11 to Figure 4-13.

Furthermore, one additional parametric sweep was performed to further solidify the relationship between the ZVS boundary regions for each leg and the efficiency profile of the PSFB converter. For this analysis, the controller was configured to maintain a fixed 200 ns deadtime for one leg; and the deadtime for the other leg was swept from 75 ns to 350 ns. This evaluation makes it possible to independently evaluate the sensitivity of the system efficiency to the operation of each leg. The results of this analysis are presented in Figure 4-15 for the sweep of the leading leg deadtime, and in Figure 4-16 for the sweep of the lagging leg deadtime. It can clearly be seen in each case that deadtime selection has a pronounced effect on efficiency. To be more specific, efficiency at low power levels is especially sensitive to the selection of the deadtime.
Figure 4-15: Efficiency contour plots, sweeping output power and deadtime of leading switches ($T_{d,lag}$ fixed at 200ns).

Figure 4-16: Efficiency contour plots, sweeping output power and deadtime of lagging switches ($T_{d,lead}$ fixed at 200ns).
Figure 4-15 demonstrates that efficiency at low power suffers when the deadtime for the leading switches is not long enough. As discussed previously, the leading leg switches require comparatively longer deadtimes to achieve ZVS and are expected to lose ZVS if the selected deadtime is too short. To verify that the efficiency drop observed in this regime is the result of ZVS loss for the leading leg, it is helpful to inspect the experimental waveforms for this condition. Accordingly, Figure 4-17 presents drain-source voltage and gate-source voltage waveforms for a leading-leg switch, operating at the very bottom left corner of Figure 4-15 ($P_{out} = 1.1kW$ and $T_{d,lead} = 75ns$). As shown in this figure, the drain-source voltage is approximately 500 V when the gate is turned on. Therefore, this switch is clearly not switching under ZVS conditions, and should be expected to incur substantial switching loss.

On the other hand, Figure 4-16 shows that efficiency at low power suffers when the deadtime for the lagging switches is too long. For the lagging switches, the time window for

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**Figure 4-17:** An example of non-ZVS switching waveform at $P_{out} = 1.1kW$ and $T_{d,lead} = 75 ns$ of plot in Figure 4-15 for a leading switch.
achieving ZVS is rather limited and may end prior to completion of the switching event if the selected deadtime is too long. To verify that the efficiency drop observed in this regime is the result of ZVS loss for the lagging leg, it is helpful to inspect the experimental waveforms for this condition. Accordingly, Figure 4-18 presents drain-source voltage and gate-source voltage waveforms for a lagging switch, operating at the very top left corner of Figure 4-16 ($P_{out} = 1.1kW$ and $T_{d,lead} = 350ns$). As shown in this figure, the drain-source voltage of this switch initially rings down to zero volts. However, since the deadtime is large, the drain-source voltage starts rising back towards the input bus voltage at approximately 200 ns. By the time that the switch gate is turned on at 350 ns, almost the full input bus voltage is present across the device. Therefore, this switch is subject to hard-switching in this scenario and should be expected to incur substantial switching loss.

Figure 4-18: An example of non-ZVS switching waveform at $P_{out} = 1.1kW$ and $T_{d,lead} = 75$ ns of plot in Figure 4-16 for a leading switch.
4.6. Application Discussions

The previous sections of this dissertation have provided an empirically validated theoretical analysis of the ZVS mechanisms for the PSFB converter topology. These mechanisms were also demonstrated to strongly influence the overall performance of the PSFB converter under realistic operating conditions. However, some additional information is needed to translate these general observations into specific recommendations that can be put into practice. This section provides specific recommendations for capitalizing on the trends that have been identified in order to optimize the performance of a practical PSFB converter design.

4.6.1. Dynamic Deadtime Optimization

Any deadtime value within the shaded regions of Figure 4-7 through Figure 4-10 is equally effective in achieving ZVS for the affected switch set. However, from an efficiency standpoint, all of these values are not equally desirable. Indeed, it is beneficial to keep the deadtime as small as possible in most cases. This is due to the fact that longer deadtimes increase the conduction time of the primary-side switch body diode, which is more dissipative than the channel of the device [68]-[70]. Therefore, one viable optimization method is to implement a scheme that varies the deadtime as a function of output power. Some commercial controller implementations implement load-power dependent deadtime enforcement in order to better manage the required deadtime values within these constraints [82]. However, these schemes could be further improved by employing the theoretical treatment in this manuscript. For example, Equation (3-4) could be used to determine the optimal deadtime value for the lagging switches as a function of output power. This would result in the “dynamic deadtime trajectory” annotated in Figure 4-7. Similarly, Equation (3-8) could be used to determine the optimal
deadtime value for the leading switches as a function of output power. This would result in the “dynamic deadtime trajectory” annotated in Figure 4-9.

However, designers should bear in mind that the lower deadtime boundaries defined by Equation (3-4) and Equation (3-8) represent theoretical limits. Use of these minimum values includes an implicit assumption that the switch can be activated instantaneously whenever desired by the controller. However, practical gate-drive designs incur non-negligible latency. This needs to be taken into account when leveraging this or any other theoretical treatment for optimizing deadtime values. Some reasonable margin should be added to these minimum values predicted by the theoretical model to account for gate-drive latency and other non-idealities. It is noted that the impact of gate-drive circuit latency on the required minimum deadtime values for achieving ZVS is often neglected in the literature. It is further noted that, depending on the operating point, the loss penalty for underestimating the required minimum deadtime might be less or more than overestimating it. To be more specific, at low power levels, where switching losses generally dominate over conduction losses, underestimating the required minimum deadtime may have a more severe effect on efficiency. On the other hand, at high power levels, where conduction losses generally dominate over switching losses, overestimating the minimum deadtime may have a more severe effect on efficiency due to the longer conduction time of the body diode. Nevertheless, in all cases, the designer should be aware of the latency present in the gate-drive circuitry and include a modest level of engineering margin in the estimation of the minimum required deadtime to account for this factor.

4.6.2. Static Deadtime Optimization

One natural alternative to the dynamic deadtime strategy is employing a fixed deadtime at all operating points. Indeed, this may be the preferred approach in many implementations due
to the simplicity of the implementation. In this approach, a single deadtime value (for each switch leg) must be selected for a given configuration of circuit parameters. The theoretical treatment provided in this manuscript can also be used for this scenario. For both switching legs, the optimum fixed deadtime is the value that provides ZVS across the widest possible range of output power levels. This value is annotated as the “optimal fixed deadtime” in Figure 4-7 for the lagging leg and in Figure 4-9 for the leading leg. For the lagging leg, this value also corresponds to one-quarter of the resonant period of the equivalent circuit shown in Figure 3-3. This value can be derived as follows:

\[
T_{d,\text{lag}}(\text{opt}) = \frac{\pi}{2} \times \sqrt{\frac{2 \times C_{Q,\text{equ}} \times L_r}{}}
\]  

(4-1)

One-quarter of the resonant tank period is also traditionally referenced in the literature as the optimal fixed deadtime value for the lagging switches [29][48][72].

As long as sufficient energy is stored in the resonant tank of Figure 3-3, the fixed deadtime value calculated by Equation (4-1) guarantees ZVS for the lagging switches. However, as noted previously, ZVS will give way to valley-switching at light load. In this condition, it is important to configure the deadtime such that the device is turned on when the drain-source voltage is at the valley point (i.e. the lowest value) during the resonant action. Fortunately, this valley point occurs at exactly one-quarter of the resonant period. Therefore, in addition to providing ZVS at the broadest possible output power range, the optimum fixed deadtime computed by Equation (4-1) also provides the best valley-switching performance for lagging switches at low power levels where ZVS cannot be achieved.
4.6.3. Resonant Inductor Value

In Figure 4-7, it is observed that the experimental values deviate from the predicated lower deadtime boundaries at low output power levels. This indicates that, as output power decreases, the ZVS opportunity window ends sooner than what is predicted by theory. This is an important fact that is often neglected in the literature describing the selection of the resonant inductor value. Many papers provide a method to calculate the minimum value of the resonant inductor based on either the amount of charge or energy stored in the MOSFET output capacitance [42][47][51][67]. For example, it is commonly claimed that the resonant inductor should be selected to satisfy the following condition [42][47][51][67]:

$$\frac{1}{2} L_r I_0^2 > Q_{oss} (V_{DC})V_{DC}$$  \hspace{1cm} (4-2)

where $I_0$ is the initial current of resonant inductor $L_r$ and $Q_{oss}$ is the total stored charge of the MOSFET in question at input bus voltage $V_{in}$. However, this condition disregards the fact that charging and discharging of the MOSFET output capacitance is not a lossless process. For SiC MOSFETs, it has been shown that losses up to 10% of the energy stored in the output capacitance can occur during the charging and discharging process [67]; for SuperJunction MOSFETs, this loss may be as high as 50% of the energy stored in the output capacitance [63][64]. By not considering the $C_{oss}$ hysteresis losses, Equation (4-2) gives an optimistic prediction of the power level at which ZVS can occur for the lagging switches. Alternatively, this error can also lead to the calculation of a resonant inductor value that is too small for achieving ZVS at the desired output level. Furthermore, Equation (4-2) disregards the fact that not all of the stored energy in the resonant inductor can be used for discharging the MOSFET output capacitance. Some of this energy is dissipated by the resistive elements of the circuit before being used for discharging the MOSFET output capacitance. Therefore, to address this underestimation, a modest margin should
also be included in the estimation of the minimum resonant inductor value needed to achieve ZVS for a certain output power level.

In light of the previous discussion, designers may consider using a much larger resonant inductor than needed, in order to ensure ZVS at light loads. However, there is a disadvantage to the use of a large resonant inductor. A large resonant tank leads to excessive “duty cycle loss” for the PSFB converter, as discussed in section 2.4. Duty cycle loss occurs during the current commutation interval of the resonant inductor, as illustrated during the \([t_6, t_8]\) time interval of Figure 2-2. During this current commutation interval, although the input voltage is applied to the transformer primary winding, power is not transferred to the secondary side of the converter. This reduces the total portion of the switching period that can be used to deliver power to the load. Selecting a very large value of the resonant inductor magnifies this problem. In some cases, this can lead to inability to regulate the output voltage at the desired setpoint due to the lack of available duty cycle. There are several possible solutions to this problem, such as reducing the transformer primary-to-secondary turns ratio. However, a better solution is often limiting the size of the resonant inductor to the value needed to ensure ZVS at a reasonable output power level, including some design margin. For example, one typical guideline is to select the resonant inductor value to achieve ZVS for the lagging switches at 30\% to 50\% of the rated load current [72][85]-[87].

In this chapter, the predictions of the ZVS and the associated ZVS behavior trends, presented in CHAPTER 3, were empirically validated and discussed in the context of practical converter design. Moreover, empirical efficiency trends with regard to changes in various system parameters were presented and discussed. Furthermore, some application discussions were presented that can help designers to better tune this converter. In the next chapter, a multi-
objective optimization framework will be introduced that can be leveraged to optimize efficiency and power density of PSFB converter. Then, employing this framework, the design of an optimized PSFB converter will be presented.
CHAPTER 5
MULTI-OBJECTIVE OPTIMIZATION OF THE PSFB CONVERTER

5.1. Introduction

This chapter is dedicated to the design of an optimized PSFB converter for datacenter applications by pursuing improvements in both the efficiency and power density of the original prototype PSFB converter presented in CHAPTER 4. The basic idea of this design is to leverage analytical models of the components that contribute to losses within this topology in conjunction with simple volume projections for the main converter elements in order to optimize the system. As discussed previously, an inherent trade-off between efficiency and power density pertains to most power electronic systems. Thus, the optimization discussed in this chapter seeks to quantify this trade-off and seek solutions that are optimal in a Pareto sense [88]. Essential to this optimization process is the analytical treatment for achieving ZVS, which was presented in CHAPTER 3. This analytical treatment makes it possible to estimate switching loss, which is a major constituent of the loss budget of the converter, while varying different system parameters, such as deadtime, resonant inductor value, switch output capacitance, output power, etc. Two other system-level enhancements are applied to the design of the improved PSFB converter described in this chapter. The improved PSFB converter design features synchronous rectification on the secondary side and liquid cooling for thermal management of the power semiconductors. Moreover, similar to the original prototype PSFB converter introduced in CHAPTER 4, all power semiconductors are based on SiC technology. The initial aim for this optimized design is to achieve at a peak efficiency close to 98% while increasing the system
power density to 2-2.5 times higher than that of the previous version. As previously mentioned in section 4.2.1, current isolated DC-DC converters of the PSU unit of datacenters, operating at 50 – 100 kHz, typically have a power density of less than 50 W/in³ [79]. Therefore, the targeted power density should realize a denser implementation than the typical datacenter implementations.

5.2. Multi-Objective Optimization

Multi-objective optimization is an area of mathematics that is concerned with problems having at least two objective functions, which need to be optimized simultaneously. In other words, a multi-objective optimization problem is defined as the problem of simultaneously minimizing $n$ number of objective functions $\phi_i(p)$, $i = 1, ..., n$, with a variable vector $p$ defined in the universe $U$, that is [89]:

$$\min_{p \in U} \{\phi_1(p), \phi_2(p), ..., \phi_n(p)\}$$

(5-1)

In general, a multi-objective function has no single solution that can optimize all solutions simultaneously. This means that reduction of one objective function usually leads to an increase in another and vice versa. But a set of equally sufficient, or non-inferior, solutions exists that provides the best possible compromise between the competing objective functions. These solutions are referred to as “Pareto optimal solutions” [88][89]. In mathematical terms, a solution $p^*$ is considered Pareto optimal if there is no other solution that satisfies both of the following conditions [89]:

a. $\phi_i(p) \leq \phi_i(p^*)$ for all $i = 1, 2, ..., n$ and

b. $\phi_j(p) < \phi_j(p^*)$ for at least one $j$.
Accordingly, the Pareto optimal front is the set of all Pareto solutions for a multi-objective optimization problem. Therefore, a solution to a multi-objective function must lie on the Pareto optimal front.

In this dissertation, simultaneous optimization of efficiency and power density is pursued for the system under design. Therefore, it is desired to minimize the system net volume, $V_{\text{net}}$, and the total efficiency penalty, $TP$ (which will be defined shortly). Accordingly, Figure 5-1 shows a notional diagram of a solution set that could be encountered in this problem. In this diagram, all the feasible solutions are denoted by circles and stars. As shown, moving along the x-axis towards the origin leads to higher power density while moving along the y-axis towards the origin leads to higher efficiency. Ideally, the best solution is the one that would lie on the origin. Obviously, this solution does not exist because all practical converters have some losses and require some volume allocation. Therefore, the Pareto optimal solutions (as depicted by Figure 5-1: Notional diagram of the Pareto Optimal fronts and solutions in multi-objective optimization of efficiency and power density for a converter.)
stars) that lie on the Pareto optimal front (as depicted by the green line) are the most desirable solutions in this multi-objective optimization problem. In the following sections, multi-objective optimization of the PSFB converter for optimizing the efficiency and power density is pursued by employing the concept of Preto optimality, presented in this section.

5.3. Optimization Design Procedure for PSFB Converter

The category of high-efficiency, high-power-density DC-DC power supplies is somewhat limited to power converters that employ soft-switching along with synchronous rectification in order to reduce both switching and conduction losses. When considering other often-required demands such as high power transfer, low complexity, and galvanic isolation, the design space becomes even more restricted. As mentioned in CHAPTER 1, the PSFB converter is among a few standard topologies that can fulfill these requirements and is widely employed in the industry for high power density applications.

The PSFB converter variant with passive rectification was discussed in CHAPTER 2 and the corresponding schematic was presented in Figure 2-1. In order to reduce the conduction loss associated with the secondary side diodes, synchronous rectification is often employed. Synchronous rectification (also known as active rectification) is a technique for improving the

![Figure 5-2: The synchronous-rectified PSFB converter circuit topology.](image)

---

85
efficiency of a converter by replacing diodes with actively controlled switches such as power MOSFETs [90]. This technique reduces the conduction loss that otherwise occurs due to the relatively high forward voltage drop of the diodes during conduction. Consequently, a PSFB converter equipped with synchronous rectification is expected to have a noticeable advantage, in terms of efficiency, over a similar PSFB converter with passive rectification. Figure 5-2 shows the synchronous-rectified PSFB converter schematic. The only difference between this variant and the passive-rectified PSFB converter of Figure 2-1 is that MOSFETs (denoted by $SR_1$, $SR_2$, $SR_3$, and $SR_4$ ) are employed instead of diodes for rectification on the secondary side. The operational description of the synchronous-rectified PSFB converter is the same as that presented in CHAPTER 2 for the passive-rectified PSFB converter. The only difference is that in this design, the secondary-side MOSFETs actively switch on and off to mimic the operation of the replaced diodes.

In order to design an optimized converter, specific design parameters need to be identified, categorized, and tuned. The PSFB converter has a relatively large number of design

![Design parameters of the synchronous-rectified PSFB converter considered in this study.](image)

Figure 5-3: Design parameters of the synchronous-rectified PSFB converter considered in this study.
parameters and requires a comprehensive tuning process. The design parameters considered in this study are illustrated in Figure 5-3. It should be mentioned that some of these design parameters considered (e.g. core selection, number of turns, output inductor and capacitor values, etc.) are by-products of the main design parameters considered in the optimization procedure of this converter. All these design parameters collectively influence the system efficiency and power density. Therefore, a methodical design procedure is required to tune the design parameters for optimizing the system efficiency and power density. Due to the inherent trade-off between system efficiency and power density, it is difficult to achieve a converter design that has good performance in both categories. However, by applying an appropriate set of modeling tools, this trade-off can be quantified, and intelligently managed. The starting point for this process is to recognize that the majority of losses within a converter are either conduction-related losses or frequency-dependent losses.

One major component of system conduction losses is related to the behavior of power semiconductors when turned on. It is noted that the conduction behavior of unipolar devices such as MOSFETs and bipolar devices such as IGBTs is fundamentally different. However, for the purposes of this study, the focus is on unipolar devices. To reduced conduction losses for unipolar devices such as SiC MOSFETs, paralleling devices is a very effective approach and is commonly employed by designers. However, this approach increases the system size due to the additional space allocation for the devices themselves as well as the associated heat exchanger volume. Similarly, increasing the system switching frequency is a well-known method for achieving higher power density. However, frequency-dependent converter losses, such as switching losses, core losses, skin effect losses, and proximity effect losses, become more
prominent at higher frequencies. It should be mentioned that although soft-switching schemes greatly reduce the switching losses in power semiconductors, $C_{oss}$ hysteresis losses are not eliminated by such schemes [44][66]. Therefore, when soft-switching is employed, these residual soft-switching losses are increased with frequency, although they are much smaller than hard-switching losses. Similarly, increasing the system switching frequency increases the AC resistance of conduction paths due to skin effect and proximity effects, especially in transformers and inductor windings. Furthermore, most magnetic core materials suffer increased core losses with increased frequency as well. Consequently, although increasing the system switching frequency tends to increase the system power density, generally the related losses also increase, leading to lower efficiency.

All this means that the trade-off between system efficiency and system power density must be carefully considered during converter performance optimization. Since these two performance objectives stand in opposition, multi-objective optimization is required. The ultimate result of this optimization is presented in terms of the “Pareto Optimal Front”, as discussed in section 5.2. Consequently, multiple sets of optimized solutions are obtained from Pareto optimization. Due to the interdependence of the underlying parameters, a sequential determination of these parameters very likely will not result in an optimum solution. Instead, an automated design optimization procedure needs to be employed. The overall optimization procedure outline that was designed to optimize the efficiency and power density of the PSFB converter as part of this research is shown in Figure 5-4. The details of this optimization procedure are explained in the following paragraphs and the underlying analytical models of the constituent components are presented in sections 5.4 and 0. It should be mentioned that in this study MATLAB is used for implementing this optimization procedure. However, another
The design procedure shown in Figure 5-4 starts with step 1, in which the converter fixed parameters (including electrical, magnetic, and volumetric information) are fed to the framework. The main fixed parameters of the system that are used in this optimization procedure are listed in Table 2.
In step 2, the design parameter values are set by the optimization solver engine (in here, Genetic Algorithm). These values are used in the following steps to calculate the corresponding system operating point values as well as the system net volume. The main design parameters that are tuned in the optimization loop are presented in Table 3. During optimization, each design parameter is bounded between user-specified values in order to manage the total computation time of the optimization process. Accordingly, only integer values are considered for the number of paralleled switches on the primary and secondary sides. Information on the candidates for switch and magnetic core selections is stored in a database and an index number is assigned to each candidate. During each iteration, the optimization solver references the appropriate index to access the information for each switch or magnetic core candidate. It should be mentioned some of the system design values, such as the filter inductor value, the filter capacitor value, the number of turns for each inductor, and the number of cores for each inductor are byproducts of the main design parameters. These parameter values are calculated based upon the main design parameter values, which occurs outside the optimization loop. Also, it should be noted that some application requirements, such as dynamic response specifications, may impose additional

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter</th>
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</thead>
<tbody>
<tr>
<td>Nominal output power ($P_o$)</td>
<td>Output voltage ($V_o$)</td>
</tr>
<tr>
<td>Input voltage ($V_{in}$)</td>
<td>Transformer turns ratio ($n = \frac{n_p}{n_s}$)</td>
</tr>
<tr>
<td>Transformer leakage inductance ($L_{lk}$)</td>
<td>Transformer magnetizing inductance ($L_m$)</td>
</tr>
<tr>
<td>Transformer interwinding capacitance ($C_T$)</td>
<td>Maximum output ripple voltage ($\Delta V_o$)</td>
</tr>
<tr>
<td>Maximum filter inductor ripple current ($\Delta I_{L_o}$)</td>
<td>Gate-driver board volume ($V_{gd}$)</td>
</tr>
<tr>
<td>Transformer volume ($V_T$)</td>
<td>Input capacitor volume ($V_{cin}$)</td>
</tr>
</tbody>
</table>
constraints on some of the system design values. For example, the application requirements for output voltage overshoot or undershoot during a load step change can limit the range of acceptable values for output filter capacitor and inductor. Accordingly, if needed, such constraints for design values should be properly formulated in the optimization algorithm in order to eliminate the unacceptable values.

In step 3 through step 6, the relevant operating information for four different operating points is calculated. This includes calculating specific voltage and current values within the converter at each operating point. These current and voltage values are used to compute loss estimations for critical system components in the following steps. The four operating points are selected according to the Energy Star® requirements for server applications [5]. Specifically, operating points of 10%, 20%, 50%, and 100% of the rated output power are considered in the

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of paralleled primary switches</td>
<td>$n_{\text{prim}}$</td>
</tr>
<tr>
<td>Number of paralleled secondary switches</td>
<td>$n_{\text{sec}}$</td>
</tr>
<tr>
<td>Resonant inductor value</td>
<td>$L_r$</td>
</tr>
<tr>
<td>Lagging switches deadtime</td>
<td>$T_{d,\text{lag}}$</td>
</tr>
<tr>
<td>Leading switches deadtime</td>
<td>$T_{d,\text{lead}}$</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{\text{sw}}$</td>
</tr>
<tr>
<td>Primary switch candidates</td>
<td>-</td>
</tr>
<tr>
<td>Secondary switch candidates</td>
<td>-</td>
</tr>
<tr>
<td>Resonant inductor ($L_r$) core candidates</td>
<td>-</td>
</tr>
<tr>
<td>Output inductor ($L_o$) core candidates</td>
<td>-</td>
</tr>
</tbody>
</table>
optimization procedure. It should be mentioned that the performance evaluation at each of these operating points is equally weighted in the framework. However, if desired, the designer can consider assigning different weights.

In step 7 through step 10, the main system losses are estimated for each corresponding operating point. The main contributors to the total system loss are categorized under one of the following categories: 1) the primary-side switches, 2) the secondary-side switches, 3) the power inductors, and 4) the transformer. Each of these categories includes multiple loss constituents that will be analytically modeled in the following sections of this chapter. It should be mentioned that the ability to predict the ZVS realization of the primary switches with respect to numerous system parameters is one of the main pillars of this optimization framework. If the primary switches fail to achieve ZVS and operate under hard-switching conditions, substantial losses occur. Therefore, it is crucial to accurately predict the ZVS realization for all primary switches as

![Figure 5-5: EnergyStar® [5] and the reference efficiency used in the optimization procedure.](image-url)
other design parameters are adjusted within the optimization loop. Due to the analytical ZVS models developed in section 3.3 of this dissertation, this determination can be accurately made.

In step 11, the total loss and efficiency at each operating point are calculated. At this point, an efficiency cost function is needed to determine how the overall efficiency profile (comprised at four operating points) compares to the reference efficiency profile. The efficiency profile specified in the Energy Star® requirement for computer servers [5] is selected as the baseline and shifted up 4% to obtain the reference efficiency profile $\eta_{ref}$ illustrated in Figure 5-5. The efficiency cost function used in this work, which is hereafter called the “efficiency penalty”, is adopted from [27]. This cost function compares the predicted or actual efficiency points, $\eta_{act \nu}$ ($\nu \in \{10\%, 20\%, 50\%, 100\%\}$), to the reference efficiency points, $\eta_{ref \nu}$ ($\nu \in \{10\%, 20\%, 50\%, 100\%\}$). Accordingly, the efficiency deviation is defined as:

$$\Delta \eta_{\nu} = \eta_{ref \nu} - \eta_{act \nu} \quad \nu \in \{10\%, 20\%, 50\%, 100\%\}$$  \hspace{1cm} (5-2)

The efficiency penalty $p(\Delta \eta_{\nu})$ is defined as a function of the efficiency deviation $\Delta \eta_{\nu}$ as:

$$p(\Delta \eta_{\nu}) = \begin{cases} 
\frac{1}{1 - \eta_{ref \nu}} \times (1 - \eta_{act \nu}), & \text{for } \Delta \eta < 0 \\
1, & \text{for } \Delta \eta = 0 \\
(1 - \eta_{ref \nu} + \eta_{act \nu})^{20}, & \text{for } \Delta \eta > 0 
\end{cases} \nu \in \{10\%, 20\%, 50\%, 100\%\}$$  \hspace{1cm} (5-3)

The efficiency penalty cost function is depicted as a function of the efficiency deviation $\Delta \eta_{\nu}$ in Figure 5-6. As shown in this figure, the efficiency penalty linearly decreases for $\Delta \eta_{\nu}$ smaller than zero and monotonically increases for $\Delta \eta_{\nu}$ larger than zero. The efficiency penalty is 1 when the actual and the reference efficiency values are equal (i.e. when $\Delta \eta_{\nu} = 0$). Subsequent to the efficiency penalty calculation for each targeted operating point, these values are summed up to form the total efficiency penalty, $TP$, as:
$$TP = \sum_v p(\Delta \eta_v) \quad v \in \{10\%, 20\%, 50\%, 100\%\}$$

(5-4)

$TP$ is the metric used by the global optimization solver in order to compute the cost for a given solution set in terms of efficiency.

In parallel to steps 3 to 11, the volume of the main system components is calculated from the current value of the design parameters in step 12. As a result of tuning the design parameters, the volume of system components such as the resonant inductor, the output filter inductor, the output filter capacitor, the power semiconductors, and the coldplate change in each iteration. On the other hand, the volume of some system components remains fixed regardless of the value of the varying system parameters. The fixed-volume components include the transformer, the gate driver board, and the input capacitor. The system net volume, $V_{net}$, which is directly used by the global optimization solver, is estimated by summing the volume of all main components:

$$V_{net} = \sum V_x$$

(5-5)

where $V_x$ is the volume of each system component specified in Table 4. A more detailed description of the computation of these component volumes will be presented in section 5.5.
By leveraging the total efficiency penalty cost function $\mathcal{T}_P$ and the system net volume cost function $V_{\text{net}}$, the global optimization solver changes the design parameters systematically in step 13 in an attempt to solve the multi-objective function of:

$$\text{Minimize } \{\mathcal{T}_P, V_{\text{net}}\} \quad x \in S$$  \hspace{1cm} (5-6)

where $x$ is the set of design parameters, as presented in Table 3, and $S$ is the set of ranges for design parameters. Steps 2 through 13 are repeated until the Pareto optimal front, which represents the best possible compromise between minimizing $\mathcal{T}_P$ and minimizing $V_{\text{net}}$, is achieved. The principal output of the optimization process is the set of Pareto-optimal solutions. Each solution consists of a set of candidate design parameters that can be employed to implement the optimized PSFB converter. It should be mentioned that the Genetic Algorithm (GA) is employed as the global optimization solver in this dissertation. The Genetic Algorithm is an adaptive search algorithm for solving constrained and unconstrained optimization problems that uses the “theory of evolution” to find optimal solution(s) among a population of candidates [91]. The GA is a powerful solver than can avoid local minima (or maxima) of a feasible space and converge to a global minimum (or maximum) solution. Robust and efficient GA implementations are available through the MATLAB Global Optimization Toolbox [92] as well.
as through open-source MATLAB toolboxes such as GOSET[93]. This study employs the GA implementation provided by the GOSET toolbox.

5.4. Component Loss Models

The component analytical loss models shown in the optimization procedure of Figure 5-4 are presented in this section. These models are presented in the following order. First, a mechanism for estimating the losses of the power semiconductors is presented in section 5.4.1. Next, a mechanism for estimating the losses in the magnetic components is formulated in section 5.4.2. Finally, the residual losses in the remaining components are briefly discussed in section 5.4.3.

5.4.1. Semiconductor Loss Models

Losses in the power semiconductors (specifically in MOSFETs and diodes) are mainly caused by conduction loss and switching loss. To a lesser degree, the gate drive circuit loss and $C_{oss}$ hysteresis loss [63][64] also contribute to the total power loss associated with the switching devices. Paralleling switching devices at each switch position has a major influence on the corresponding conduction and switching losses. The following subsections provide the underlying models for loss estimation of the primary side and secondary side switches.

5.4.1.1. Channel Conduction Loss Model

The conduction loss for a set of paralleled MOSFETs is a function of the switch position current, the individual device on-resistance, and the number of paralleled devices. Therefore, the conduction loss of the primary and secondary switch positions is expressed as:

$$P_{cond,prim} = \frac{R_{DS,prim}}{n_{prim}} \times I_{sw,prim}^2$$

(5-7)
\[ P_{\text{cond,sec}} = \frac{R_{SD,sec}}{n_{sec}} \times I_{sw,sec}^2 \]  

(5-8)

where \( P_{\text{cond,prim}} \) and \( P_{\text{cond,sec}} \) are the conduction losses of the primary side and the secondary side switch positions, respectively; \( n_{\text{prim}} \) and \( n_{\text{sec}} \) are the number of paralleled switches per primary and secondary switch position, respectively; \( R_{DS,prim} \) is drain-source on-resistance of the primary side switches; and \( R_{SD,sec} \) is the source-drain channel resistance of the secondary side switches; and \( I_{sw,prim} \) and \( I_{sw,sec} \) are the RMS current values of the primary-side and secondary-side switch positions, respectively. \( I_{sw,prim} \) and \( I_{sw,sec} \) are defined by equations (2-12) and (2-13), respectively. It should be mentioned that, due to synchronous rectification, the secondary switches conduct current from source to drain. Therefore, the source-to-drain channel resistance, rather than the drain-to-source channel resistance, is relevant in this case. Accordingly, this channel resistance value must be extracted from the third quadrant characteristics presented in the device datasheet.

5.4.1.2. Body Diode Conduction Loss Model for Primary Switches

Apart from the channel resistance, another element that contributes to semiconductor conduction losses in the PSFB converter is the body diode of the active switches. Since the

![Figure 5-7: Primary switch Body diode current shape during the conduction times.](image)
primary switch deadtimes are design parameters, it is particularly important to model this behavior in order to calculate the loss penalty incurred as the result of utilizing longer than needed deadtime values. Figure 5-7 shows the current profile of the primary switch body diode current during the conduction times (i.e. [t2 t3] and [t4 t5] for the leading and lagging switches, respectively, in Figure 2-2). As discussed previously, a minimum deadtime value of $T_{d,min}$ is needed for the switch $C_{DSS}$ to be discharged (i.e. for the switch $V_{DS}$ to become zero) before the switch body diode starts conducting. Therefore, if $T_d$ is less than $T_{d,min}$ for the switch type in question (i.e. leading or lagging), the associated body diode will not conduct. However, longer deadtime values lead to conduction of the switch body diode. The conduction time of the body diode for each switch type is calculated as follows:

- If $T_d \leq T_{d,min}$:
  \[ t_{bd} = 0 \]  \hspace{1cm} (5-9)

- If $T_{d,min} < T_d < T_{d,max}$ and $0 < I_{bd}(1)$:
  \[ t_{bd} = T_d - T_{d,min} \]  \hspace{1cm} (5-10)

- If $T_{d,min} < T_d < T_{d,max}$ and $I_{bd}(1) = 0$:
  \[ t_{bd} = T_d - t_{1|I_{bd}(1)=0} \]  \hspace{1cm} (5-11)

- If $T_{d,max} < T_d$:
  \[ t_{bd} = T_{d,max} - T_{d,min} \]  \hspace{1cm} (5-12)

where $T_{d,min}$ and $T_{d,max}$ are the minimum and maximum allowable deadtime values to achieve ZVS for the switch type in question, respectively. At light loads, it is possible for the body diode current to become zero before the deadtime ends. This marks the end of the body diode conduction interval as well. In this case, the body diode conduction time is defined by (5-11), in which $t_{1|I_{bd}(1)=0}$ is the time at which $I_{bd}$ becomes zero.
For either type of primary switch, the body diode current decreases in an approximately linear fashion after the current starts flowing in the body diode. This current decline is due to the start of the freewheeling period for the leading switches or changing the direction of the primary-side current for the lagging switches. The rate of change for the current in the body diode for each type of primary switch can be computed as:

$$\frac{di_{bd,lead}}{dt} \approx \frac{V_{cb}}{L_{lk}}$$ \hspace{1cm} (5-13)

$$\frac{di_{bd,lag}}{dt} \approx \frac{V_{in}}{L_{r}}$$ \hspace{1cm} (5-14)

where \(\frac{di_{bd,lead}}{dt}\) and \(\frac{di_{bd,lag}}{dt}\) are the rate of change of the body diode current for the leading and lagging switches, respectively; \(V_{cb}\) is the maximum voltage across the blocking capacitor \(C_b\); \(L_{lk}\) is the transformer leakage inductance value; \(V_{in}\) is the input voltage; and \(L_{r}\) is the resonant inductor value.

The body diode initial current, \(I_{bd}(0)\), for both primary switch types can be approximated by:

$$I_{bd}(0) \approx I_o \cdot \frac{1}{n} + \left(1 - D_{eff}\right) \times \frac{V_o}{4 \times n \times L_o \times f_{sw}} + I_{m,max}$$ \hspace{1cm} (5-15)

where \(I_o\) is the output current; \(n\) is the transformer primary to secondary turns ratio; \(D_{eff}\) is the effective duty cycle; \(V_o\) is the output voltage; \(L_o\) is the output filter inductor value; \(f_{sw}\) is the switching frequency, and \(I_{m,max}\) is the transformer maximum magnetizing current as defined by equation (2-6). Utilizing equation (5-15) in conjunction with equation (5-13) and equation (5-14), the value of \(t_{1|I_{bd}(t)=0}\) is derived for the leading and lagging switches as:

For leading switches: \(t_{1|I_{bd}(t)=0 (lead)} = I_{bd}(0) \times \frac{L_{lk}}{V_{cb}}\) \hspace{1cm} (5-16)
For lagging switches: \( t_{1|bd(t)=0}^{(\text{lag})} = I_{bd}(0) \times \frac{L_{r}}{V_{in}} \) \hspace{1cm} (5-17)

Finally, the total body diode conduction loss for both types of primary switches in the PSFB converter is estimated as:

\[
P_{bd} \approx A_{bd} \times t_{bd}^2 + B_{bd} \times t_{bd} + C_{bd}
\]

\[
A_{bd} = \frac{1}{3} \times R_{bd} \times \left( \frac{dI_{bd}}{dt} \right)^3
\]

\[
B_{bd} = R_{bd} \times I_{bd}(0) \times \frac{dI_{bd}}{dt} - \frac{1}{2} \times V_{th} \times \frac{dI_{bd}}{dt}
\]

\[
C_{bd} = R_{bd} \times I_{bd}^2(0) - V_{th} \times I_{bd}(0)
\]

where \( V_{th} \) is the threshold voltage of the MOSFET and \( R_{bd} \) is the equivalent resistance of the body diode for the MOSFET. Both of these parameters can be extracted from the datasheet of the MOSFET in question. It is noted that, depending on the switch type (leading or lagging), \( t_{bd} \) is calculated based on equations (5-9) to (5-12) and \( \frac{dI_{bd}}{dt} \) is calculated from equation (5-13) or equation (5-14).

5.4.1.3. Switching Loss Model

The primary side switches are expected to operate under ZVS conditions if proper deadtime values are employed and sufficient inductive energy is available. The turn-on switching loss under ZVS conditions is expected to be very near zero. However, if the MOSFET output capacitance is not fully discharged before turning-on, either due to insufficient stored inductive energy or an inappropriate deadtime value, hard switching occurs during turn-on. On the other hand, the primary side switches of the PSFB topology do not generally operate under ZVS conditions during turn-off transitions. Therefore, turn-off switching losses are expected for the primary side MOSFETs.
The theoretical model presented in section 3.3 predicts the realization of ZVS according to various system parameters. This model is central to assessing ZVS operation for the primary switches in accordance with numerous system parameter variations in the optimization loop. Accordingly, if ZVS operation is predicted for either set of primary switches, the corresponding turn-on switching loss can be assumed to be zero for that design parameter set, i.e.:

\[ f_{\text{on,lead}} < T_{d,\text{lead}}(\text{min}) : P_{\text{on,lead}} = 0 \] \hspace{1cm} (5-22)

\[ f_{\text{on,lag}} < T_{d,lag} < T_{d,lag}(\text{max}) : P_{\text{on,lag}} = 0 \] \hspace{1cm} (5-23)

where \( P_{\text{on,lead}} \) and \( P_{\text{on,lag}} \) are the turn-on switching losses for the leading and lagging switches, respectively.

On the other hand, the absence of ZVS operation can lead to (full or partial) hard-switching for the primary switches. In other words, ZVS operation is not expected for leading switches under the following conditions:

\[ T_{d,\text{lead}} < T_{d,\text{lead}}(\text{min}) \] \hspace{1cm} (5-24)

Similarly, ZVS operation is not expected for the laggings witches under the following conditions:

\[ T_{d,lag} < T_{d,lag}(\text{min}) \text{ or } T_{d,lag}(\text{max}) < T_{d,lag} \] \hspace{1cm} (5-25)

In these cases, either full or partial hard switching is expected for the corresponding switch. In such cases, a residual voltage (up to the full DC input voltage, \( V_{\text{in}} \)) is present across drain-source terminals of the MOSFET when the device is turned on. Consequently, some turn-on switching loss, which is proportional to the residual voltage across the switch, is incurred. To determine this residual voltage, the equivalent circuits of Figure 3-3 and Figure 3-4 can be employed once again. Solving the equivalent circuit of Figure 3-3 for the voltage \( V_{\text{sw}} \) at time \( t = T_{d,lag} \) (subject to the conditions of (5-25)) yields the residual voltage, \( V_{\text{DS,lag (res)}} \), which is present across the
drain-source terminals of the lagging switch immediately before turn on. Similarly, solving the equivalent circuit of Figure 3-4 for the voltage $V_{sw}$ at time $t = T_{d,lead}$ (subject to the conditions of (5-24)) yields the residual voltage, $V_{DS,lead}(res)$, which is present across drain-source terminals of the leading switch immediately before turn on.

Therefore, when ZVS is not achieved at turn on for either type of primary switch, the corresponding residual voltages (i.e. $V_{DS,lead}(res)$ or $V_{DS,lag}(res)$) can be estimated according to the description above. Consequently, an analytical switching loss model is needed to calculate the switching loss incurred during non-ZVS turn-on switch transitions as well during turn-off switch transitions that do not generally experience ZVS. Analytical modeling of switching loss in power MOSFETs has been the subject of numerous studies [95]-[103]. However, many of these models rely on specific device parameters that need to be measured or are not readily available at design time. However, D. Christen and J. Biela recently proposed an analytical switching loss model that overcomes this challenge and is entirely based on available datasheet parameters [103]. The proposed model, which is based on the charge equivalent representation of MOSFET intrinsic capacitances, can individually estimate the device turn-on and turn-off switching losses. This model also takes into account the MOSFET body diode reverse recovery, the parasitic source inductance of the MOSFET package, and the current dependence of the device transconductance for determining the Miller plateau. Since this model does not require empirical waveforms to compute switching losses, it is a very good candidate for use in an optimization procedure of the type under consideration here. Therefore, the analytical switching loss model of [103] is adopted in this study to estimate the (full or partial) hard-switching losses that can occur for the primary switches. For the sake of brevity, the loss model is not described here in detail.
but is instead incorporated by reference [103]. However, Figure A-1 of Appendix A.1, which is adapted from [103], provides an overview of the procedures utilized in this switching loss model.

On the secondary side of the PSFB converter, no significant switching loss is expected because the MOSFETs in this position operate under synchronous rectification conditions [94]. Therefore,

\[ P_{sw,sec} \approx 0 \]  

(5-26)

where \( P_{sw,sec} \) is the total switching loss (i.e. the sum of turn-on and turn-off switching losses) for the secondary side MOSFETs.

5.4.1.4. \( C_{oss} \) Hysteresis Loss Model

As mentioned previously, charging and discharging the MOSFET \( C_{oss} \) is not a loss-free process. In fact, it has been shown that the output capacitance profile of some MOSFETs shows significant hysteresis during charging and discharging, which leads to unrecoverable power loss [63][64]. This hysteresis power loss is prominent in Superjunction MOSFETs. For example, the hysteresis power loss is estimated to be as high as 50% of the energy stored in the device output capacitance for some devices of this type [63][64]. On the other hand, it is estimated that SiC MOSFETs, GaN HEMTs, and low-voltage Si MOSFETs also dissipate up to 10% of the stored energy in the output capacitance due to the \( C_{oss} \) hysteresis effect [67]. \( C_{oss} \) hysteresis loss has recently become a topic of interest, and many application designers do not fully understand the implications of this phenomenon. As a result, analytical modeling of this phenomenon is not yet mature. To the best of the author’s knowledge, two main approaches have been proposed for characterizing this loss. The first method, proposed by J.B. Fedison and M.J. Harrison [64], employs a Sawyer-Tower circuit to empirically characterize the hysteresis phenomenon of the MOSFET output capacitance and estimate the related loss. The original Steinmetz equation [104]
is then fit to the estimated power loss in order to obtain a closed-form relationship to describe
this loss. The second method is based on calorimetric measurements. In this approach, the $C_{oss}$
hysteresis losses are characterized by measuring the temperature change of the device in a half-
bridge or full-bridge test circuit within a strictly controlled thermal environment [105][106].
Both of these methods require precise measurements under strictly controlled conditions in order
to obtain accurate results. Therefore, these approaches are not suitable for estimating the $C_{oss}$
hysteresis losses in the context of an iterative optimization process. On the other hand, the
analytical modeling of this loss mechanism has not been investigated in the literature. Therefore, a
simplified approach is taken for estimating the $C_{oss}$ hysteresis losses in this study. For the
purpose of optimization, the $C_{oss}$ hysteresis energy loss, $E_{oss}$, is approximated as 10% of the
total energy stored in the MOSFET output capacitance, $E_{oss}$, at each specific operating point,
i.e.:

$$E_{hyst}(V_{DS}) = 0.1 \times E_{oss}(V_{DS}) = 0.1 \times \int_0^{V_{DS}} v \times c_{oss}(v) dv$$

(5-27)

Consequently, the $C_{oss}$ hysteresis power loss for each primary switch position is estimated as:

$$P_{hyst, prim} = n_{prim} \times E_{hyst}(V_{DS}) \times f_{sw}$$

(5-28)

where $n_{prim}$ is the number of paralleled switches per primary switch position and $f_{sw}$ is the
switching frequency.

5.4.2. Magnetic Component Loss Models

The PSFB converter of Figure 5-2 has three main magnetic components, namely the
transformer $T_r$, the resonant inductor $L_r$, and the output filter inductor $L_o$. Magnetic components
are another major source of losses in a power converter. These losses can be generally broken
down into copper losses and core losses. Each of these loss mechanisms is modeled and described in detail in the following subsections.

5.4.2.1. Core Loss Model

An important limiting factor in high-frequency magnetic components is core loss. For low-frequency (i.e. 50 Hz and 60 Hz) applications, magnetic component design is generally limited by the core material saturation flux density. However, in high-frequency applications, magnetic component design is generally limited by core losses [107]. Therefore, when employing high switching frequencies, core losses become significant and need to be considered in the converter design process. Three main mechanisms collectively establish the total core loss for a given magnetic component:

1. Hysteresis losses
2. Eddy current losses
3. Residual or relaxation losses

The details of these core loss mechanisms can be found in the literature [108]-[110]. To optimize the efficiency and power density of the converter under study, the total core loss of each magnetic component in the design must be estimated. Unfortunately, due to the nonlinear properties and complex nature of magnetic materials, precise estimation of core losses is often a tedious task. However, a common approach to approximate the total core loss in magnetic components is to utilize the so-called “Steinmetz equation”. The Steinmetz equation is an empirically-based derivation. According to this equation, the core power loss per unit volume, $P_{cv}$, is expressed as:

$$P_{cv} = a \times B_{pk}^b \times f^c$$  (5-29)
where $a$, $b$, and $c$ are the Steinmetz parameters; $f$ is the operating frequency, and $B_{pk}$ is half of the AC flux swing in the core:

$$B_{pk} = \frac{\Delta B}{2} = \frac{B_{ac,max} - B_{ac,min}}{2}$$  \hspace{1cm} (5-30)

The Steinmetz parameters $a$, $b$, and $c$ depend on the core material and are found by curve fitting. Core manufacturers often provide either the Steinmetz parameters or the plots of $P_{cv}$ vs. $B_{pk}$ for different $f$ values. The total core loss is calculated as:

$$P_c = P_{cv} \times V_c$$  \hspace{1cm} (5-31)

where $V_c$ is the core volume.

The Steinmetz core loss expression is formulated for pure sinusoidal excitation with frequency $f$. However, the magnetic cores in modern power converters rarely (if ever) experience sinusoidal excitation. In fact, magnetic cores in power electronics converters are subject to waveforms composed of a broad range of frequencies. Often, the switching frequency is dominant and the switching frequency harmonics also play a role in determining the overall core losses. Therefore, it is expected that the original Steinmetz equation of (5-29) will be inaccurate under non-sinusoidal core excitation [111][112]. Unfortunately, quantifying the influence of excitation harmonics into the core loss equation is a complex task. Numerous investigations have been reported to address this problem [113]-[118]. However, most of these studies have led to more complicated formulations that depend on parameters that are not supplied by core manufacturers and must be independently measured. Consequently, the practical usage of these models is limited. However, an extension of the Steinmetz equation, called the “Improved Generalized Steinmetz Equation” (IGSE) [112], is proposed by K. Venkatachalam et al. The IGSE improves core loss estimations for non-sinusoidal excitation.
waveforms using only the Steinmetz parameters supplied by manufacturers. The general form of this core loss formulation is expressed as [109]:

\[ P_{cv\mid IGSE} = \frac{k_i}{T} \int_0^T \left| \frac{dB}{dt} \right|^c |\Delta B|^{b-c} dt \]  

(5-32)

\[ k_i = \frac{a}{2^{b-c}(2\pi)^{c-1}} \int_0^{2\pi} |\cos \theta|^c d\theta \]  

(5-33)

where \( P_{cv\mid IGSE} \) is the core loss per unit volume estimated by the IGSE method; \( a, b, \) and \( c \) are the Steinmetz parameters; \( T \) is the fundamental period of core excitation; and \( \Delta B \) is the core magnetic flux density change, expressed as:

\[ \Delta B = B_{max} - B_{min} \]  

(5-34)

Fortunately, the core loss estimation of (5-32) can be further simplified. The magnetic components of modern power converters are usually subjected to one of two typical excitations. The first typical excitation is a rectangular waveform without a period of zero voltage, and the second typical excitation is a rectangular waveform with a period of zero voltage. The notional waveform of each of these excitations, as well as the resultant flux density, is shown in Figure 5-8. In the PSFB converter, the core of the output inductor, \( L_o \), experiences the excitation waveform of Figure 5-8(a), while the core of the transformer and the resonant inductor, \( L_r \), experience the excitation waveform of Figure 5-8(b). Consequently, the IGSE equation of (5-14) can be further simplified according to each of the excitation waveforms of Figure 5-8 [119][120]. The core loss per unit volume of a rectangular core excitation without a period of zero voltage is given by:

\[ P_{cv} = k_i \times f^c \times B_{pk}^b \times 2^b \left[ D_{core}^{1-c} + (1 - D_{core})^{1-c} \right] \]  

(5-35)

Similarly, the core loss per unit volume of a rectangular core excitation with a period of zero voltage is given by:

\[ P_{cv} = k_i \times f^c \times B_{pk}^b \times 2^{b+c} \times D_{core}^{1-c} \]  

(5-36)
In both of these formulations, $P_{\text{cv}}$ is the core loss per unit volume; $a$, $b$, and $c$ are the Steinmetz parameters; $f$ is the fundamental frequency of the core excitation (i.e. the switching frequency); $B_{pk}$ is the maximum flux density of the core; and $D_{\text{core}}$ is the duty cycle of core excitation.

In the optimization process considered here, equation (5-35) is used for core loss estimation of the output inductor, $L_o$, and equation (5-36) is used for core loss estimation of the transformer and the resonant inductor, $L_r$. The core excitation duty cycle (i.e. $D_{\text{core}}$) and the maximum core flux density (i.e. $B_{pk}$) for the output inductor, $L_o$ are computed as follows.

\[
D_{\text{core},L_o} = D_{\text{eff}}
\]

\[
B_{pk,L_o} = \mathcal{F}_1(H_{\text{max},L_o})
\]

\[
H_{\text{max},L_o} = \frac{T_{c,L_o} \times I_{L_o,\text{max}}}{I_{L_o}}
\]

The core excitation duty cycle (i.e. $D_{\text{core}}$) and the maximum core flux density (i.e. $B_{pk}$) for the resonant inductor, $L_r$ are computed as follows.
\[ D_{\text{core},Lr} = \frac{4 \times I_{p,\text{max}} \times L_r \times f_{sw}}{V_{in}} \]  \hspace{1cm} (5-40)

\[ B_{pk,Lr} = \mathcal{F}_2(H_{\text{max},Lr}) \]  \hspace{1cm} (5-41)

\[ H_{\text{max},Lr} = \frac{T_{c,Lr} \times I_{p,\text{max}}}{l_{Lr}} \]  \hspace{1cm} (5-42)

The core excitation duty cycle (i.e. \( D_{\text{core}} \)) and the maximum core flux density (i.e. \( B_{pk} \)) for the transformer, \( T_r \) are computed as follows.

\[ D_{\text{core},Tr} = D_{\text{eff}} \]  \hspace{1cm} (5-43)

\[ B_{pk,Tr} = \frac{D_{\text{eff}} \times V_{in}}{4 \times f_{sw} \times n_p \times A_{Tr}} \]  \hspace{1cm} (5-44)

In the above formulations, \( D_{\text{core},Lo}, D_{\text{core},Lr}, \) and \( D_{\text{core},Tr} \) are the core excitation duty cycles for the output filter inductor, the resonant inductor, and the transformer, respectively; \( B_{pk,Lo}, B_{pk,Lr}, \) and \( B_{pk,Tr} \) are the maximum core flux densities of the output filter inductor, the resonant inductor, and the transformer, respectively; \( H_{\text{max},Lo} \) and \( H_{\text{max},Lr} \) are the maximum magnetic field intensities for the output filter inductor and the resonant inductor, respectively; \( \mathcal{F}_1 \) and \( \mathcal{F}_2 \) are the B-H (i.e flux density vs. magnetic field intensity) functions for the output filter inductor core and the resonant inductor core, respectively; \( D_{\text{eff}} \) is the effective duty cycle of the converter as defined by equation (2-3); \( I_{p,\text{max}} \) is the maximum transformer primary current as defined by equation (2-5); \( I_{Lo,\text{max}} \) is the maximum output filter inductor current as defined by equation (2-9); \( T_{c,Lo} \) and \( T_{c,Lr} \) are the number of turns for the output filter inductor and the resonant inductor, respectively; \( l_{Lo} \) and \( l_{Lr} \) are the effective core lengths for the output filter inductor and the resonant inductor, respectively; \( A_{Tr} \) is the core cross section area of the transformer; \( n_p \) is the transformer primary number of turns; \( f_{sw} \) is the switching frequency; and \( V_{in} \) is the input voltage.
Therefore, equations (5-35) to (5-43) can be employed to estimate the core loss per unit volume of the output filter inductor, the resonant inductor, and the transformer of the PSFB converter. It is noted that equation (5-35) is relevant for core loss estimation of the output filter inductor while equation (5-36) is relevant for core loss estimation of the resonant inductor and the transformer. Subsequent to these calculations, the final core loss estimate for each component is determined by multiplying the calculated core loss per unit volume (i.e. $P_{cv}$) by the volume of the associated core (i.e. $V_c$), as expressed by equation (5-31).

5.4.2.2. Copper Loss Model

Another important loss mechanism in magnetic components is the associated “copper losses”, which are also called “winding losses”. Copper losses consist of a DC power loss part and an AC power loss part. The DC power loss is caused by the DC component of the current in a given conductor. In this design, round copper magnet wire with a wire gauge of 12 (i.e. AWG 12) [121] is employed for winding the inductors. The DC resistance of a round conductor, $R_{dc}$, can be calculated as:

$$R_{dc} = \rho \times \frac{l}{A}$$ \hspace{1cm} (5-44)

where $\rho$ is the resistivity of the material employed, $l$ is the total length of the conductor, and $A$ is the cross-section area of the conductor. Consequently, the DC power loss, $P_{w,dc}$, for a winding fashioned from a round conductor is computed by:

$$P_{w,dc} = R_{dc} \times I_{dc}^2$$ \hspace{1cm} (5-45)

where $I_{dc}$ is the dc component of the conductor current.

On the other hand, the AC power losses of a conductor relate to the increase in the conductor resistance due to induced eddy currents within the conductor. These eddy currents originate either from the alternating magnetic field of the conductor itself or from the alternating
magnetic fields generated by nearby conductors. The generated eddy currents, in return, cause a nonuniform current flow within the conductor, effectively increasing the conductor resistance. The increase of a given conductor’s resistance due to its own alternating current is called “skin effect”, while the increase of a given conductor’s resistance due to the alternating current of nearby conductors is called “proximity effect”. The influence of these induced eddy currents increases with frequency [107]. For this reason, it is expected that conductor resistance and the associated copper losses will increase with frequency as well.

One method of estimating the AC resistance due to the skin effect involves determining and solving a Bessel function. However, the solution of this Bessel function is complex and prone to error as the skin depth becomes less than about one-tenth of the conductor radius [122][123]. Alternative solutions have been proposed that estimate the AC resistance due to the skin effect based on an effective cross-section area at a specified stimulus frequency. For example, the AC resistance due to the skin effect, $R_{ac}$, is calculated as [122]:

$$R_{ac} = \rho \times \frac{l}{A_{eff}}$$  \hspace{1cm} (5-46)

where $\rho$ is the resistivity of the conductor material, $l$ is the total length of the conductor, and $A_{eff}$ is the cross-section area of the conductor, which is defined as:

$$A_{eff} = \pi \delta (1 - e^{-\frac{r}{\delta}}) (2r - \delta \left(1 - e^{-\frac{r}{\delta}}\right))$$  \hspace{1cm} (5-47)

where $r$ is the radius of the conductor and $\delta$ is skin depth, which is given as:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$  \hspace{1cm} (5-48)

where $f$ is the stimulus frequency; $\mu$ is the permeability of the conductor material; and $\delta$ is the conductivity of the conductor material. Consequently, the AC copper loss (due to the skin effect) is calculated as:
\[ P_{w,ac} = R_{ac} \times I_{ac}^2 \] (5-49)

where \( I_{ac} \) is the AC component of the winding current at frequency \( f \).

Unfortunately, the formulation of the AC resistance increase due to the proximity effect is not as straightforward as that associated with the skin effect. In the case of proximity effect, the AC resistance of the conductor changes due to the effect of external magnetic fields, which are generated by other nearby conductors. Therefore, the AC resistance increase due to the proximity effect is strongly dependent on the spatial placement and the current of adjacent conductors (which form the resultant external magnetic field). Finite element analysis (FEA) utilizing specialized software is one common method employed to estimate the AC resistance increase due to the proximity effect. However, this requires the exact geometry of the windings, which may change at each iteration of the optimization process. The FEA process also requires extensive computational resources. Consequently, obtaining the proximity effect contribution to the AC resistance of a conductor winding through FEA is not practical in the type of optimization procedure considered here. Therefore, the proximity effect contribution to the copper loss of magnetic components is not considered in this study.

5.4.3. Output Capacitor Dielectric Loss Model

The equivalent series resistance (ESR) in the output filter capacitor, \( C_o \), generates some losses in this component. To estimate this loss component, it is assumed the output current, \( I_o \), is a pure DC quantity and that the entirety of the output inductor ripple current passes through the output capacitor. Under this assumption, the output capacitor loss is expressed as:

\[ P_{co} = ESR_{co} \times I_r^2 \] (5-50)
where $ESR_{co}$ is the ESR of the output filter capacitor and $I_r$ is the RMS value of the output capacitor ripple current. The output capacitor ripple current is equal to the output inductor current ripple, $\Delta I_{Lo}$, as defined by equation (2-8). Therefore, $I_r$ is calculated as:

$$I_r = \frac{(1-D_{eff}) \times V_o}{4\sqrt{3} \times L_o \times f_{sw}} \quad (5-51)$$

where $D_{eff}$ is the effective duty cycle as defined by equation (2-1); $V_o$ is the output voltage; $L_o$ is the output inductor value; and $f_{sw}$ is the switching frequency.

5.5. Component Volume Models

Estimation of the volume of the main system components is also required for optimizing the PSFB converter power density. The estimated component volumes are computed by the global optimization algorithm, which systematically changes the design parameters to optimize the system power density. The main system components that influence the net volume of the converter include the primary switches, the secondary switches, the resonant inductor, the output filter inductor, the output filter capacitor, the input capacitor, the transformer, the gate drive circuit, and the cold plate. For some of these components, the volume changes at each iteration of the optimization loop, while the volume of the other components is fixed. The models utilized to estimate the volume of each of these components are presented in the following subsections.

5.5.1. Semiconductor Volume Model

The primary and secondary switches utilized in this design are packaged in the standard TO-247 through-hole package [124]. Hence, the total volume of the primary and secondary semiconductors is calculated as:

$$V_{sw,p} = 4 \times n_{prim} \times V_{to247} \quad (5-52)$$
\[ V_{sw,s} = 4 \times n_{sec} \times V_{to247} \] (5-53)

where \( V_{sw,p} \) and \( V_{sw,s} \) are the total primary and secondary semiconductor volumes, respectively; \( n_{prim} \) and \( n_{sec} \) are the number of parallel switches per position for the primary and secondary sides, respectively; and \( V_{to247} \) is the volume of a single TO-247 semiconductor package. \( V_{to247} \) is approximated as:

\[ V_{to247} \approx 1.6e - 6 \text{ m}^3 \] (5-54)

5.5.2. Inductor Volume Model

The resonant and output inductor volumes depend on the core candidate specifications and the value of required inductance. The value of each inductor may change at each iteration of the optimization process. The optimization procedure employs the analytical model presented in section 3.3 to tune the value of the resonant inductor \( L_r \) so that ZVS is realized across the widest possible range of operating conditions. The value of the output filter inductor \( L_o \) is obtained according to the other design parameters and the specification for the maximum allowable inductor ripple current:

\[ L_o = 1.2 \frac{(1 - D_{eff}) \times V_o}{2 \times \Delta I_{lo,\text{max}} \times f_{\text{sw}}} \] (5-55)

where \( D_{eff} \) is the effective duty cycle as defined by equation (2-1); \( V_o \) is the output voltage; \( \Delta I_{lo,\text{max}} \) is the maximum allowable ripple current of the output inductor; \( f_{\text{sw}} \) is the switching frequency; and 1.2 is a scaling factor that is used to add a small amount of design margin to the value of this inductor. Commonly, the maximum allowable ripple current of the output inductor is set as 10\% to 40\% of the nominal output current [125]-[127]. For this study, the 20\% value is used. Accordingly, \( \Delta I_{lo,\text{max}} \) is expressed as:

\[ \Delta I_{lo,\text{max}} = 0.2 \times I_{o,\text{max}} \] (5-56)
where $I_{o,max}$ is the maximum expected output current, or the nominal output current of the converter at rated load.

The optimization framework also considers a range of options for the magnetic cores used to implement the resonant and filter inductors. These design alternatives are hereafter referred to as “core candidates”. For a given inductor design, the selected core candidate should be able to withstand the maximum expected current without experiencing saturation. If saturation is detected for a core candidate during the framework calculations, the current solution is to increase the number of cores that are employed in series to achieve the desired inductance value. In this scenario, a smaller number of turns is utilized for each series-connected core. In turn, each series-connected core is subject to reduced magnetic flux density, $B$. The maximum number of turns that can be wound on a given core candidate without the risk of saturation, $T_{c,sat}$, is calculated as:

$$T_{c,sat} = \left\lfloor \frac{H_{sat} \times l_e}{I_{max}} \right\rfloor$$  \hfill (5-57)

where $H_{sat}$ is the maximum magnetic field strength permissible for the specified core candidate without the risk of saturation; $l_e$ is the effective length of the specified core candidate; and $I_{max}$ is the maximum winding current. The brackets employed in equation (5-57) represent the “floor” operator, which returns the largest integer less than or equal to its argument. The maximum winding current $I_{max}$ for the resonant inductor, $L_r$, is calculated as:

$$I_{max}(L_r) = \frac{I_o}{n} + \frac{(1-D_{eff}) \times V_o}{4 \times n \times L_o \times f_{sw}} + I_{m,max}$$  \hfill (5-58)

where $I_o$ is the nominal output current; $n$ is the transformer primary to secondary turns ratio; $D_{eff}$ is the effective duty cycle as defined by equation (2-1); $V_o$ is the output voltage; $L_o$ is the output filter inductor value; $f_{sw}$ is the switching frequency; and $I_{m,max}$ is the transformer
maximum magnetizing current as defined by equation (2-6). Similarly, the maximum winding current $I_{\text{max}}$ for the output inductor, $L_o$, is calculated as:

$$I_{\text{max}}(L_o) = I_o + \frac{(1-D_{\text{eff}}) \times V_o}{4 \times L_o \times f_{\text{sw}}} \quad (5-59)$$

where $I_o$ is the nominal output current; $n$ is the transformer primary to secondary turns ratio; $D_{\text{eff}}$ is the effective duty cycle as defined by equation (2-1); $V_o$ is the output voltage; $L_o$ is the output filter inductor; and $f_{\text{sw}}$ is the switching frequency.

On the other hand, there exists a maximum number of turns for each core candidate due to geometry. This limitation depends on the available winding window area and the winding conductor diameter. Accordingly, the maximum number of turns that a core candidate can physically accommodate, $T_{c,w}$, is calculated as:

$$T_{c,w} = \left[ K_{\mu} \times \frac{W_a}{A_w} \right] \quad (5-60)$$

where $A_w$ is the winding conductor area; $W_a$ is the available winding window area; and $K_{\mu}$ is the so-called “core window utilization factor”. $K_{\mu}$ is the fraction of the core winding window that can realistically be filled with conductors. A typical value of $K_{\mu}$ is 0.4 for inductors [107]. The brackets in equation (5-60) represent the floor operator, which returns the largest integer less than or equal to its argument.

Equations (5-57) and (5-60) specify two different maximum turns limitations for a given inductor design. Since both the winding physical geometry limitation and the core saturation limitation must be respected, the maximum number of turns for a given core candidate, $T_{c,max}$, is the minimum of $T_{c,sat}$ and $T_{c,w}$:

$$T_{c,max} = \min (T_{c,sat}, T_{c,w}) \quad (5-61)$$
The next step in estimating the volume of a given inductor element is to determine the maximum inductance, \( L_{c,max} \), that a given core candidate can achieve. This parameter is calculated as:

\[
L_{c,max} = \mu_0 \times \mu_r \times \frac{A_e \times T_e^{2 \max}}{l_e}
\]  
(5-62)

where \( \mu_0 \) is the permeability of the free space (i.e. the vacuum); \( \mu_r \) is the relative permeability of the core material; \( A_e \) is the core cross-section area; and \( l_e \) is the effective length of the core.

Therefore, the total number of required series-connected cores, \( N_c \), to implement an inductor with a total inductance value of \( L \) is calculated as:

\[
N_c = \left\lceil \frac{L}{L_{c,max}} \right\rceil
\]  
(5-63)

The brackets in equation (5-63) represent the ceiling operator, which returns the smallest integer greater than or equal to its argument. Moreover, under the assumption that an equal number of turns is applied to each series-connected core, the selected number of turns, \( T_e \), is calculated as:

\[
T_e = \left\lceil \sqrt{\frac{L \times l_e}{\mu_0 \times \mu_r \times A_e}} \right\rceil
\]  
(5-64)

The brackets in equation (5-64) again represent the ceiling operator, which returns the smallest integer greater than or equal to its argument. Utilizing the preceding formulation, the total volume for a given inductor element, \( V_L \), is calculated as:

\[
V_L = 1.05 \times (N_c \times V_c)
\]  
(5-65)

where \( N_c \) is the total number of required cores; \( V_c \) is the volume of each core; and 1.05 is a scaling factor to account for the volume increase due to the presence of windings around the core geometry.
5.5.3. Capacitor Volume Model

The volume of the output capacitor, $C_o$, can be determined from its value and the volume per capacitance relationship of a chosen capacitor family. The value of $C_o$ is formulated as:

$$C_o = 4 \times \frac{\Delta I_{L,o,max}}{16 \times \Delta V_{o,max} \times f_{sw}} \tag{5-66}$$

where $\Delta I_{L,o,max}$ is the output inductor maximum ripple current as defined by equation (5-56); $\Delta V_{o,max}$ is maximum allowable output ripple voltage; $f_{sw}$ is the switching frequency; and 4 is an optional scaling factor that is used to add design margin to the value of this capacitor. This margin is needed to compensate for the ripple voltage caused by the capacitor ESR value. The maximum allowed ripple voltage, $\Delta V_{o,max}$, is set to 1V in this study.

In order to provide a generalized model for estimating the output capacitor volume within the optimization framework, a volume per capacitance ratio is needed. Such a ratio can be defined based on the geometric specifications provided in most commercial capacitor datasheets [128][129]. In this study, the 450V ECWFE capacitor series from Panasonic [130] is chosen as the 450V ECWFE series capacitors (450V rated voltage) from Panasonic [130].
the reference for the output filter capacitor. The general relation between the volume and the capacitance of this capacitor series is extracted by applying linear regression to the volume vs. capacitance points of all capacitors in this series. Figure 5-9 depicts the result of this fitting process. The resulting output capacitor volume model is formulated as:

\[ V_{co} = 1.128C_o + 6.14e^{-7} \]  \hspace{1cm} (5-67)

5.5.4. Cold Plate Volume Model

For the optimized PSFB converter design considered here, the semiconductor switches are the main components that are mounted on the cold plate. Therefore, the determination of the minimum cold plate volume, \( V_{cld,\text{min}} \), depends on the total number of switches as well as the unit surface area required for the placement of each switch. The thickness of the cold plate is assumed to be a constant value for the purposes of optimization. The system utilizes \( n_{prim} \) and \( n_{sec} \) active switches on the primary and secondary sides, respectively. In addition, as seen in Figure 5-2, the system also employs two damping diodes, \( D_{p1} \) and \( D_{p2} \). These diodes are housed in TO220 packaging [131], which is slightly smaller than the TO247 packaging that houses each active switch [124]. However, for the sake of simplicity, it is assumed that these diodes require the same unit surface area on the cold plate as the active switches. Correspondingly, the minimum required cold plate volume is estimated as:

\[ V_{cld,\text{min}} = S_u \times H_{cld} \times (n_{prim} + n_{sec} + 2) \]  \hspace{1cm} (5-68)

where \( S_u \) is the unit surface area required for mounting each semiconductor element in \( m^2 \) and \( H_{cld} \) is the cold plate height in m.
5.5.5. Fixed Volume Components

As mentioned previously, some of the system components selected for the optimized PSFB converter design have a fixed volume and therefore do not take part in the optimization process. These components are listed in Table 5. It should be mentioned that optimizing the transformer design is out of the scope for this study. While the transformer plays an important role in determining the overall performance of the PSFB converter, optimizing this one component would require significant effort. This would require an extensive trade study and substantial modeling to simultaneously optimize the design of the core as well as the transformer windings. In light of the influence of skin and proximity effects, this would necessitate an extensive finite element analysis (FEA) study. Since the current study is focused on multi-objective optimization of the PSFB converter topology rather than optimization of magnetics, the transformer design was excluded from the optimization process. Instead, a custom-made planar transformer, part number 59850 from Payton Planar [132], is used in this design. Consequently, the transformer volume is fixed.

Before utilizing the models presented in this chapter to optimize the converter design, it is important to first validate these models, especially the loss models presented in section 5.4. This validation has been performed and is presented in Appendix A.1.

<table>
<thead>
<tr>
<th>TABLE 5: THE MAIN FIXED VOLUMES IN OPTIMIZATION OF THE PSFB CONVERTER.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer volume ($V_T$)</td>
</tr>
<tr>
<td>Input capacitor volume ($V_{cin}$)</td>
</tr>
</tbody>
</table>
5.6. Optimization Results

This section details the results of applying multi-objective optimization to the design of an enhanced PSFB converter for datacenter applications. The goal of this process is to obtain improvements in both the efficiency and power density of the original prototype PSFB converter presented in CHAPTER 4 by applying the procedure outlined in Figure 5-4 along with the analytical models described in sections 5.4 and 0. As mentioned previously, the Genetic Algorithm (GA) is employed as the global optimization solver for implementation of this procedure. The main design parameters that the optimization algorithm alters during operation are presented in Table 3. The objective functions used in this process are the total efficiency penalty and the system net volume, which are defined by equation (5-4) and equation (5-5), respectively. The overall cost function, which the Genetic Algorithm seeks to minimize, is defined by equation (5-6). During operation, each design parameter shown in Table 3 is selected from a predefined range of values or selected from a predefined list of options. These predefined parameter ranges and component selection options are enumerated in Table 6.

As presented in Table 6, up to three paralleled devices per switch position are considered by the optimization process for both the primary and secondary sides of the converter. The resonant inductor, $L_r$, range is defined between 1$\mu$H and 25$\mu$H. Note that while larger $L_r$ values may extend the ZVS range to lower power levels, this also leads to increased duty cycle loss. The allowable deadtime range for the lagging switches is between $10\,ns$ and $900\,ns$. A wider range is available for the deadtime of the leading switches because these switches generally require longer deadtime to achieve ZVS. The system switching frequency is tuned between $50\,kHz$ and $200\,kHz$. 


It is well known that within a class of power MOSFETs (e.g. 1.2 kV SiC MOSFETs), die size generally determines both channel resistance and output capacitance. For example, large die generally have low channel resistance and large output capacitance, $C_{oss}$. Inversely, small die

<table>
<thead>
<tr>
<th>Design Parameter</th>
<th>Range/Component Candidate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of paralleled primary switches ($n_{prim}$)</td>
<td>$1 \leq n_{prim} \leq 3 ; n_{prim} \in \mathbb{N}$</td>
</tr>
<tr>
<td>Number of paralleled secondary switches ($n_{sec}$)</td>
<td>$1 \leq n_{sec} \leq 3 ; n_{sec} \in \mathbb{N}$</td>
</tr>
<tr>
<td>Resonant inductor value ($L_r$)</td>
<td>$1 \mu H \leq L_r \leq 25 \mu H$</td>
</tr>
<tr>
<td>Lagging switches deadtime ($T_{d,lag}$)</td>
<td>$10 ns \leq T_{d,lag} \leq 500 ns$</td>
</tr>
<tr>
<td>Leading switches deadtime ($T_{d,lead}$)</td>
<td>$10 ns \leq T_{d,lead} \leq 900 ns$</td>
</tr>
<tr>
<td>Switching frequency ($f_{sw}$)</td>
<td>$50 kHz \leq f_{sw} \leq 200 kHz$</td>
</tr>
</tbody>
</table>

| Primary side switch candidates          | Littelfuse LSIC1MO120E0080 [80] |
|                                        | Littelfuse LSIC1MO120E0025       |
|                                        | Littelfuse LSIC1MO120E0040       |

| Secondary side switch candidates        | Littelfuse LSIC1MO120E0080 [80] |
|                                        | Littelfuse LSIC1MO120E0025       |
|                                        | Littelfuse LSIC1MO120E0040       |

| Resonant inductor ($L_r$) core candidates | Magnetics 0055256A2 [133] |
|                                          | Magnetics C055083A2 [134]   |
|                                          | Magnetics C055248A2 [135]   |
|                                          | Magnetics C055249A2 [136]   |
|                                          | Magnetics C055250A2 [137]   |

| Output inductor ($L_o$) core candidates  | Magnetics 0055256A2 [133] |
|                                          | Magnetics C055083A2 [134] |
|                                          | Magnetics C055248A2 [135] |
|                                          | Magnetics C055249A2 [136] |
|                                          | Magnetics C055250A2 [137] |
generally have small output capacitance and high channel resistance [138][139]. Due to these characteristics, large die are often favored for applications in which conduction losses are dominant, and small die are often favored for applications in which switching losses are dominant.

For a complex topology such as the PSFB converter, it is not known beforehand whether switching losses or conduction losses will dominate when the entire load envelope is considered. Therefore, it is not known whether the optimal design should include switches with large die (to minimize conduction losses) or small die (to minimize residual switching losses). This decision has complex implications that are linked to a number of other design parameters (such as the switching frequency). This decision is therefore best left up to the optimization process.

Accordingly, three different SiC MOSFETs from the same class (i.e. 1.2kV) and manufacturer but with different $R_{DS(on)}$ values (and accordingly different $C_{oss}$ profiles) are selected for inclusion in the optimization process. Therefore, as noted in Table 6, three different MOSFETs from Littelfuse are selected as the primary and secondary switch candidates. In this list, part number LSIC1MO120E0080 is a small-die 80$m\Omega$ SiC MOSFET [80]; part number LSIC1MO120E0040 is a medium-die 40$m\Omega$ MOSFET; and part number LSIC1MO120E0025 is a large-die 25$m\Omega$ MOSFET. It should be mentioned that LSIC1MO120E0040 and LSIC1MO120E0025 are not commercially available and were obtained as engineering samples from Littelfuse. Table A-1 of the Appendix A.3 enumerates the most important characteristics for each of these three switch candidates.

For the design of the resonant inductor and the output inductor, five core candidates are selected for inclusion in the optimization process. All of the selected cores belong to the MPP category from Magnetics Inc. [140] but have different material properties. The five different core
materials represented in this set (MPP26, MPP60, MPP173, MPP300, and MPP550), show distinct core loss profiles from one another. In general, MPP cores exhibit low hysteresis and eddy current losses, excellent inductance stability under high DC bias conditions or after high DC magnetization, and minimal inductance shift up to magnetic flux density values of $0.2T$ under AC conditions [140]. Table A-2 of the Appendix A.4 enumerates the most important characteristics for each of these five core candidates. The corresponding B-H and B vs. $P_{cv}$ curves for each of these cores can be accessed in [140].

As mentioned previously, some system components do not take part in the optimization procedure and their volume is assumed to be fixed. The volumes of these components are presented in Table 7. Moreover, the list of fixed system parameter values employed in the optimization procedure is summarized in Table 8.

<table>
<thead>
<tr>
<th>TABLE 7: THE MAIN COMPONENTS WITH A FIXED VOLUME.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer ($T_r$)</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>Volume ($in^3$)</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
### Table 8: Fixed Parameters Used in the Optimization Process.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value /Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated output power ( P_0(\text{rated}) )</td>
<td>10 kW</td>
</tr>
<tr>
<td>Input DC voltage ( V_{in} )</td>
<td>750 V</td>
</tr>
<tr>
<td>Output DC voltage ( V_{in} )</td>
<td>350 V</td>
</tr>
<tr>
<td>Transformer turns ratio ( n = \frac{n_p}{n_s} )</td>
<td>( \frac{16}{10} )</td>
</tr>
<tr>
<td>Transformer leakage inductance ( L_{lk} )</td>
<td>0.76 ( \mu H )</td>
</tr>
<tr>
<td>Transformer magnetizing inductance ( L_m )</td>
<td>946 ( \mu H )</td>
</tr>
<tr>
<td>Transformer interwinding capacitance ( C_T )</td>
<td>650 ( pF )</td>
</tr>
<tr>
<td>Maximum ripple current of output inductor ( \Delta I_{Lo} )</td>
<td>( 0.2 \times I_o )</td>
</tr>
<tr>
<td>Maximum output ripple voltage ( \Delta V_o )</td>
<td>1 V</td>
</tr>
<tr>
<td>Input capacitor ( C_{in} )</td>
<td>12 ( uF )</td>
</tr>
<tr>
<td>Transformer volume ( V_T )</td>
<td>25.9 ( in^3 )</td>
</tr>
<tr>
<td>Gate-driver board volume ( V_{gdr} )</td>
<td>21.3 ( in^3 )</td>
</tr>
<tr>
<td>Input capacitor volume ( V_{cin} )</td>
<td>1.9 ( in^3 )</td>
</tr>
<tr>
<td>Damping diodes ( D_{p1} ) and ( D_{p2} )</td>
<td>Littelfuse LSIC2SD120A20 [81]</td>
</tr>
</tbody>
</table>
The outcome of the optimization process is shown as a Pareto optimal front in Figure 5-10. In general, a Pareto optimal front consists of all feasible solutions to the optimization problem that are not dominated by another solution. In this sense, solution $x_1$ is said to dominate solution $x_2$ if solution solution $x_1$ is no worse than solution $x_2$ in all objectives, and if solution $x_1$ is strictly better than solution $x_2$ in at least one objective [93]. Thus, the Pareto front shown in Figure 5-10 consists of those solutions that represent the best possible compromise between maximizing the system efficiency and minimizing the system net volume. These solutions are denoted by red circles in Figure 5-10. Note that the optimization procedure, which was administered by the Genetic Algorithm solver, found a total of 120 optimized solutions that are equally favorable in terms of simultaneously satisfying the efficiency and power density objectives. To make it more clear, these Pareto-optimal solutions are depicted in Figure 5-11 along with their corresponding solution indices on the z-axis. In this sense, moving along the
Pareto optimal front in one direction reduces the efficiency penalty (i.e. increases the system efficiency) at the expense of greater system volume. Moving along the Pareto optimal front in the other direction reduces the system net volume (i.e. increases the power density) at the expense of reduced efficiency. Accordingly, the designer may select among the Pareto-optimal solutions according to design preferences. Some applications may call for increased efficiency at the expense of power density; while other applications may call for increased power density at the expense of efficiency.
Figure 5-12: Optimal design parameters for each solution.
A set of unique design parameter values is associated with each optimal solution. For each design parameter, the optimal values are presented in Figure 5-12 according to the solution indices. According to these plots, the optimization procedure converged to one switch per position for the primary side for all optimal solutions. On the secondary side, most of the solutions converged to one switch per position, although a few converged to two switches per position. The optimal values selected for the resonant inductor, $L_r$, are spread between about 14 $\mu H$ and 24 $\mu H$. The optimal values selected for the lagging switch deadtime, $T_{d,lag}$, are spread between 114 $ns$ and 237 $ns$, with the majority of the solutions concentrated around 140 $ns$. On the other hand, the optimal values selected for the leading switch deadtime, $T_{d,lead}$,
are spread between $300\,\text{ns}$ and $760\,\text{ns}$, with the majority of the solutions concentrated in the vicinity of $310\,\text{ns}$. The optimal values selected for the switching frequency, $f_{sw}$, are scattered between $75\,\text{kHz}$ and $200\,\text{kHz}$. For the primary side switch, the optimization procedure selected the $25\,\text{m}\Omega$ SiC MOSFET (i.e. Littelfuse LSIC1MO120E0025) for two solutions and the $40\,\text{m}\Omega$ MOSFET (i.e. Littelfuse LSIC1MO20E040) for the rest of the solutions. No optimal solution converged to the $80\,\text{m}\Omega$ MOSFET (i.e. Littelfuse LSIC1MO20E0080 [80]) for the primary-side switch. This suggests that for a soft-switching topology such as the PSFB converter, the switch $R_{DS(\text{on})}$ may be a stronger influence than the switch output capacitance for selecting an optimal switch candidate. This may be due to the fact that switching losses are alleviated to a great extent by the soft-switching mechanism and, hence, the impact of the switch output capacitance is reduced. For the secondary side switch, all of the solutions converged to the $40\,\text{m}\Omega$ MOSFET (i.e. Littelfuse LSIC1MO20E040). This is an expected outcome because the secondary switches operate under synchronous rectification conditions. Therefore, no significant switching losses are expected for these devices [94] and the majority of the loss in these components is due to the third quadrant channel resistance, $R_{SD(\text{on})}$. Consequently, the MOSFET candidate with the lowest $R_{SD(\text{on})}$ value is expected to be the best choice for the secondary-side switch.

Accordingly, the $40\,\text{m}\Omega$ MOSFET (i.e. Littelfuse LSIC1MO20E040), which has the lowest $R_{SD(\text{on})}$ value presented in Table A-1 of the Appendix A.3, is picked by the optimization procedure for all optimal solutions. For the resonant inductor and the output filter inductor cores, the optimization procedure converged to the Magnetics Inc. 0055256A2 core [133] based on MPP26 material [140], for all optimal solutions.
Furthermore, Figure 5-13 presents the values of the non-design parameters for all optimal solutions. These are the parameters that are not directly tuned by the optimization algorithm but
rather are computed as by-products of the main design parameters. For example, the values computed for the output inductor, $L_o$, are spread from 46 $\mu$H to 125 $\mu$H. The values computed for the output capacitor, $C_o$, are spread from 6 $\mu$F to 16 $\mu$F. The algorithm also determined that only one series-connected core is required for implementing the $L_r$ and $L_o$ inductors for almost all solutions. The only exception is solution number 1, which requires two series-connected cores for the output filter inductor. This suggests that adding a second core imposes too high a penalty in terms of the system net volume to be considered as a viable option. According to the optimal values of $L_r$ and the selected core, the number of turns required for implementing this inductor ranges from 20 to 27 turns. Similarly, the number of turns required for implementing the output filter inductor, $L_o$, ranges from 37 to 52.

Figure 5-14: The chosen optimal solution on the Pareto optimal front.
As already mentioned, any of the solutions on the Pareto optimal front can be selected to implement the optimized converter, according to design preference. In this study, maximum efficiency is considered to be slightly more important than maximum system power density. Therefore, out of the 120 optimal solutions, solution number 2 is selected as the final solution for

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value/Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of paralleled primary switches ($n_{prim}$)</td>
<td>1</td>
</tr>
<tr>
<td>Number of paralleled secondary switches ($n_{sec}$)</td>
<td>2</td>
</tr>
<tr>
<td>Resonant inductor value ($L_r$)</td>
<td>$23 ; \mu H$</td>
</tr>
<tr>
<td>Lagging switches deadtime ($T_{d,lag}$)</td>
<td>$240 ; ns$</td>
</tr>
<tr>
<td>Leading switches deadtime ($T_{d,lead}$)</td>
<td>$433 ; ns$</td>
</tr>
<tr>
<td>Switching frequency ($f_{sw}$)</td>
<td>$98 ; kHz$</td>
</tr>
<tr>
<td>Primary switch</td>
<td>Littelfuse LSIC1MO120E0025</td>
</tr>
<tr>
<td>Secondary switch</td>
<td>Littelfuse LSIC1MO120E0040</td>
</tr>
<tr>
<td>Resonant inductor ($L_r$) core</td>
<td>Magnetics 0055256A2 [133]</td>
</tr>
<tr>
<td>Output inductor ($L_o$) core</td>
<td>Magnetics 0055256A2 [133]</td>
</tr>
<tr>
<td>Output inductor ($L_o$)</td>
<td>$95 ; \mu H$</td>
</tr>
<tr>
<td>Output capacitor ($C_o$)</td>
<td>$12 ; \mu F$</td>
</tr>
<tr>
<td>Number of $L_o$ cores</td>
<td>1</td>
</tr>
<tr>
<td>Number of $L_{res}$ cores</td>
<td>1</td>
</tr>
<tr>
<td>Number of turns for $L_o$</td>
<td>52</td>
</tr>
<tr>
<td>Number of turns for $L_{res}$</td>
<td>26</td>
</tr>
</tbody>
</table>
implementation. This solution is shown on the Pareto optimal front of Figure 5-14 in red. The
efficiency penalty and the net system volume are estimated for this solution as follows:

\[ TP = 2.77 \]  \hspace{1cm} (5-69)

\[ V_{net,t} = 71.9 \text{ in}^3 \]  \hspace{1cm} (5-70)

The system parameters needed to implement the PSFB converter based on solution
number 2 are presented in Table 9. These parameter values are also denoted by red asterisks in
the optimal parameter plots of Figure 5-12 and Figure 5-13. For the final design, each primary-
side switch position will be populated with one LSIC1MO120E0025 device, which is a 25 mΩ
SiC MOSFET. Each secondary-side switch position, on the other hand, will feature two parallel
LSIC1MO120E0040 devices, which are 40 mΩ SiC MOSFETs. Moreover, the deadtime for the
leading and lagging switches of the primary side will be fixed at 433 ns and 240 ns,
respectively. The switching frequency will be fixed at 98 KHz. The resonant inductor \( L_r \) will be
implemented with one Magnetics Inc. 0055256A2 core [133] and wound with 26 turns to realize
an inductance of 23 \( \mu \text{H} \). Similarly, the output inductor \( L_o \) will be implemented with one
Magnetics Inc. 0055256A2 core [133] and wound with 52 turns to realize an inductance of
95 \( \mu \text{H} \). Finally, a 12 \( \mu \text{F} \) capacitor will be utilized as the output capacitor.

The predicted system efficiency for the selected optimal solution is presented in Figure
5-15 along with the reference efficiency profile and the Energy Star \( \textregistered \) [5] efficiency criterion.
As shown in this figure, the projected system efficiency profile for the optimized system is
higher than the reference efficiency profile for most operating conditions. Only the calculated
efficiency at 5 kW is projected to be slightly lower than the corresponding reference efficiency.
However, this is not unexpected because the goal of the optimization procedure is not to
maximize the system efficiency at every point. Instead, the goal of the optimization process is to
find a balance between the system efficiency profile (over a wide range of operating conditions) and the system power density.

In this chapter, a methodical multi-objective optimization of the PSFB converter was followed by employing the loss and volumetric models of the system. To optimize the system efficiency and power density, an optimization framework was implemented to tune the system parameters systematically in order to find the Pareto optimal solutions. The design of an optimized PSFB converter was then followed by employing this optimization framework. In the next chapter, the implemented optimized PSFB converter will be introduced and the system improvements predicted by the optimization algorithm will be verified.
CHAPTER 6

OPTIMIZED PSFB CONVERTER IMPLEMENTATION AND EVALUATION

6.1. Introduction

This chapter presents the design, implementation, and evaluation of an improved prototype PSFB converter based on the optimal solution selected from the results of the multi-objective optimization procedure presented in CHAPTER 5. Accordingly, the design and implementation of the optimized converter are presented in section 6.2. In section 6.3, a baseline empirical evaluation of this system is presented. Finally, in section 6.3, the efficiency profile of the optimized converter is presented, along with the results of a final fine-tuning exercise performed with the realized prototype converter.

6.2. Implementation of the Optimized Converter

As part of this research, the selected optimal PSFB converter design described in section 5.6 was implemented according to the design parameter values presented in Table 9. As mentioned previously, the optimized prototype PSFB converter features synchronous rectification on the secondary side along with a liquid-based thermal management system. Figure 6-1 shows the PCB design and the CAD drawing of the implemented system. In this design, the mainboard is a four-layer PCB, featuring 6-oz copper for traces and pours. Counting from the top layer, internal layer number 3 is used for routing sensitive signal traces in order to provide good immunity from the electromagnetic emissions generated by the converter. Power flow within the
mainboard is concentrated in the top layer (i.e. layer number 1), the bottom layer (i.e. layer number 4), and internal layer number 2. The use of 6-oz copper in this design helps to reduce the ohmic losses associated with the power flow layers and also provides better heat conduction to improve the thermal performance of the mainboard. A custom coldplate from wakefield-vette [141] is employed as the main heat exchanger for the thermal management system. All power semiconductors are mounted to the cold plate with a thin thermal interface material employed for electrical isolation [142]. The semiconductors are sandwiched between the coldplate and the mainboard, which is secured to the coldplate with a wide bolt pattern to distribute equal mechanical pressure to all components. Furthermore, the case of the transformer is mounted to the cold plate, providing direct cooling for the transformer as well.

![Figure 6-1: The PCB and CAD drawing of the optimized prototype PSFB converter.](image)

**Table 10: Dimensions and Power Density of the Optimized Prototype PSFB Converter.**

<table>
<thead>
<tr>
<th>Length (in)</th>
<th>Width (in)</th>
<th>Height (in)</th>
<th>Power Density (W/in³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>6</td>
<td>2</td>
<td>75.7</td>
</tr>
</tbody>
</table>
Figure 6-2 presents annotated pictures of the top and front views of the realized converter. As presented in Table 10, the overall dimensions of this system include a length of 11\,\text{"}, a width of 6\,\text{"}, and a height of 2\,\text{"}. This volume envelope maps to an overall power density of 75.7\,\text{W}/\text{in}^3 when the converter is operated at 10\,\text{kW}. In this design, careful component selection was employed to ensure that no component would be taller than the installed transformer with the system fully assembled. Consequently, the power density achieved by this
design is approximately two times higher than the original prototype PSFB converter described in CHAPTER 3. The original prototype PSFB converter has a power density of $38 \, W/in^3$.

Therefore, the optimized prototype PSFB converter is demonstrated to achieve one of its main design objectives, which is realizing a power density at least two times higher than that of the original prototype PSFB converter.

6.3. Basic Empirical Evaluation

As part of this research, the prototype PSFB converter implementation presented in section 6.2 was empirically evaluated across a range of operating points. The converter coldplate was attached to an external recirculating chiller and the fluid temperature was regulated at $12 ^\circ C$.

It should be noted that the power semiconductors in this system are all mounted on a common, ground-referenced heat exchanger. It is well known that in this type of setup, common-mode

Figure 6-3: Main waveforms of the optimized prototype PSFB converter at $P_{\text{out}} = 10 \, kW$. Channel 1: $V_{\text{DS}}(Q_3)$. Channel 2: $V_{\text{DS}}(Q_4)$. Channel 3: Primary current ($i_p$). Channel 4: Primary voltage ($V_p$).
(CM) currents are likely to flow through galvanic isolation and pass into the system grounding structure [143]. Circulating CM currents may cause disruption of normal converter operation, and can also cause degradation of system insulation. Therefore, appropriately designed CM filters or chokes should be applied to the input and output of the converter in this type of setup. It may also be useful to apply CM chokes to the liquid cooling tubes attached to the chiller apparatus to suppress CM currents within the liquid.

Before evaluating the efficiency of the optimized prototype PSFB converter, a series of commissioning experiments was performed to confirm the nominal operation, dielectric strength, and thermal stability of the system. Accordingly, the system was evaluated in incremental steps up to the nominal operating voltage and rated output power level (i.e. \( V_{\text{in}} = 750 \, V \), \( V_o = 350 \, V \), and \( P_o = 10 \, kW \)). Figure 6-3 provides an oscilloscope capture of the main converter waveforms at this operating point, which verifies the expected electrical behavior of the system. On the other hand, Figure 6-4(a) presents a thermal image of the system from the top view at the rated output power level of 10 kW. As shown in this figure, most of the system components operate at

\[ (a) \quad \text{Spot: 26.5 °C, Box: 108 °C, Max: 25.6 °C, Avg: 91.8 °C} \]

\[ (b) \quad \text{Spot: 25.8 °C, Box: 32.0 °C, Max: 24.8 °C, Avg: 90.4 °C} \]

\[ \text{Figure 6-4: Thermal images of the optimized prototype PSFB converter at 10 kW: (a) Top view; (b) Front view, capturing the semiconductors.} \]
relatively low temperatures. The resonant inductor, $L_r$, is the hottest component in the system at this operating point, with a steady-state temperature of $108 \, ^\circ C$. Figure 6-4(b) presents a thermal image of the system from the front view at the rated output power level of $10 \, kW$. This image specifically captures the temperature of the power semiconductors mounted on the coldplate. As shown in this figure, the maximum recorded temperature for these devices is $32 \, ^\circ C$. This evaluation verifies that the power semiconductors in this converter are subject to very low thermal stress even at an output power as high as $10 \, kW$. The low thermal stress of the MOSFETs at this operating point affirms the benefits of realizing ZVS and implementing synchronous rectification for the primary-side and secondary-side switches, respectively.

On the other hand, as a result of optimizing the system methodically, the primary-side switches experience ZVS even at light loads. Figure 6-5(a) and Figure 6-5(b) depict experimental waveforms $V_{DS}$ and $V_{GS}$ for lagging switch $Q_3$ and leading switch $Q_4$, respectively. These waveforms correspond to turn-on switching transitions at an output power level of $1.1 \, kW$, which is about 10% of the rated output power for this converter. As shown in this figure, both
sets of primary switches experience ZVS in this light-load condition. This result suggests that the optimization procedure described in CHAPTER 5 and the underlying ZVS models presented in CHAPTER 3 provide an effective means for selecting proper system parameters. The verification of ZVS at light load is critical for the lagging switches. As detailed in CHAPTER 3 and CHAPTER 4, the lagging switches are susceptible to losing ZVS at light load.

6.4. Efficiency Evaluation

Verifying the efficiency profile of the optimized PSFB converter implementation is a critical step toward validating the success of the optimization procedure described in CHAPTER 5. It is noted that the efficiency profile of the system is one of the main two objectives.

![Efficiency Profile](image)

*Figure 6-6: The efficiency profile of the optimized prototype PSFB, compared with the predicted efficiency and the Energy Star® [5] efficiency profiles.*
considered during the optimization process. The experimental evaluation described in this section follows the efficiency evaluation guidelines already discussed in section 4.3. Therefore, for the sake of brevity, those guidelines are not repeated here. During this evaluation, the efficiency of the converter was measured at different output power levels, from about 10% to 100% of the rated load. Accordingly, Figure 6-6 presents the experimental efficiency profile of the optimized prototype PSFB converter. In this plot, the efficiency profile predicted by the optimization procedure for the selected optimal design and the Energy Star® efficiency profile reference are also plotted for comparison.

As shown in Figure 6-6, the optimized prototype PSFB converter demonstrates a peak efficiency and a full-load efficiency of 97.5% and 97.1%, respectively. Moreover, the system demonstrates 93.4% efficiency at 10% of the rated output power. This relatively high efficiency at light load is made possible by the realization of ZVS across a wide load envelope, which further confirms the proper design of this system. Moreover, as shown in this figure, the measured efficiency profile of the optimized prototype PSFB converter is 3-10% higher than the industry standard efficiency profile offered by the Energy Star standard [5] for computer servers. Furthermore, Figure 6-6 demonstrates that the efficiency profile predicted by the optimization procedure of CHAPTER 5 is very accurate. The predicted efficiency profile is in very good agreement with the measured system efficiency from 10% up to about 70% of the rated load. The predicted efficiency profile slightly overpredicts the measured system efficiency from 70% to 100% of the rated load. However, this is not an unexpected outcome due to the possibility of residual losses in the system that are not captured by the loss models presented in CHAPTER 5. Moreover, Figure 6-7 presents the loss budget of the optimized PSFB converter at 10 kW. As a
result of optimization, in total the primary and secondary side MOSFETs only dissipate about 70 W (i.e. 29% of the total loss) at this power level.

At this point, the optimized prototype PSFB converter has been demonstrated to achieve its primary design goals. First, a power density of $75.7 \, W/\text{in}^3$ is achieved, which is two times the power density of the original prototype PSFB converter. Second, the efficiency profile projected by the optimization procedure is achieved by the optimized prototype PSFB converter, with a peak efficiency of 97.5%. Nevertheless, a further post-optimization step can be taken to compare the measured efficiency profile of the optimized prototype PSFB converter with that of the original prototype PSFB converter presented in CHAPTER 4.

Accordingly, Figure 6-8 compares the measured efficiency profile of the optimized prototype PSFB converter with the measured efficiency profile of the original prototype PSFB converter presented in CHAPTER 4. As shown in this figure, the optimized prototype PSFB converter outperforms the original prototype PSFB converter at most of the operating points.
Specifically, the optimized prototype PSFB converter demonstrates a 0.5% higher peak efficiency compared to the original prototype PSFB converter. Similarly, the optimized prototype PSFB converter offers a 0.5% efficiency advantage over the original prototype PSFB converter at rated load. However, at light load, the original prototype PSFB converter demonstrates a 0.4% efficiency advantage over the optimized PSFB converter. One possible reason for this difference is that the optimized prototype PSFB converter features synchronous rectification in comparison to passive rectification in the original prototype PSFB converter. It is known that one drawback of synchronous rectification is the efficiency penalty at light load compared to the passive rectification [144]-[146].

Figure 6-8: Efficiency comparisons between the optimized prototype PSFB converter, designed in CHAPTER 5, and the original prototype PSFB converter, presented in CHAPTER 4.
Generally, improving the efficiency of power converters (and specifically those that employ synchronous rectification) at light load has received substantial treatment in the literature. In fact, numerous specialized schemes have been presented in the literature to improve system efficiency at light load for various types of power converters. Some of these techniques include bulk voltage reduction, burst-mode control, variable switching frequency control, and phase shedding [147]-[150]. Although these schemes can be effective in improving the efficiency of a DC-DC converter with synchronous rectification, they are not well suited for the current study. This is mainly because adopting any of these specialized schemes would contradict the design approach of optimizing the PSFB converter in its standard structure and control strategy, as described in CHAPTER 2. Instead, a more fundamental approach is pursued in this study. This investigation involves a fine-tuning exercise utilizing the existing design parameters of the PSFB converter in its standard structure and control strategy.

As part of this fine-tuning exercise, a set of experimental procedures was carried out at light load to evaluate the sensitivity of the system to various design parameters. This investigation revealed an unexpected sensitivity of system losses on switching frequency at light load. Figure 6-9 presents the experimental total system losses (as well as the predicted values) at light load (i.e. $P_o = 1.1 \text{ kW}$) for a few different switching frequency values, $f_{sw}$. At light load, in general, conduction loss is not a major contributor to the total system loss. Magnetic component losses, switching losses, and stray losses mainly govern the system efficiency in this condition. For well-designed soft-switching converters, the primary switches are expected to operate under ZVS conditions even at light load. Indeed, this is the case for the optimized prototype PSFB converter even at 10% rated load. Consequently, the total loss of the system at light load is expected to be dominated by magnetic component losses and stray losses.
The most important characteristic of Figure 6-9 is the shape of the total loss profile rather than the exact total loss values measured. As expected, the system loss increases at both extremes of the switching frequency range considered. Very low switching frequencies are expected to produce high losses in magnetic components due to the increased maximum flux density, $B_{pk}$, in each core. This increased flux density results from the increase in the corresponding peak current of the magnetic component at low switching frequency. On the other hand, very high switching frequencies are also expected to produce high losses in magnetic components, because core losses are proportional to operating frequency. Therefore, the relationship between magnetic component losses and the converter switching frequency is subject to competing trends. Since these trends are material dependent, it is difficult to determine which sensitivity will prevail in a general sense for a given magnetic component.
It is clear that the loss models presented in CHAPTER 5 accurately predict the general trend for total losses shown in Figure 6-9. In addition, the optimization process described in CHAPTER 5 selected a switching frequency value of 98 kHz. This value appears near the center of the minimum total loss window between 75 kHz and 125 kHz. However, the shape of the total loss profile shown in Figure 6-9 is of importance here. Note that this profile demonstrates an almost flat trend in a broad frequency range, rather than a sharp trough. In fact, the maximum difference between the total losses in the switching frequency range between 75 kHz and 125 kHz is less than 10 W. This difference in total losses is so small that it is very difficult for the optimization procedure to distinguish the exact switching frequency associated with minimum total loss. To put this in context, this difference is less than 1% of the output power at this power level and less than 0.1% of the rated power of this system. Consequently, to locate the exact “minimum-loss” switching frequency at any particular load condition, a very precise loss model that is able to distinguish between very small loss values must be implemented. Considering the error margins associated with the component loss models presented in CHAPTER 5, achieving this goal is extremely difficult. Therefore, the designer should be aware of the limitations of the theoretical model for fine-tuning the system parameters.

Accordingly, as the final step of the optimization process, the designer may consider fine-tuning the switching frequency on the bench in order to extract some marginal efficiency improvements for the system. Note that this extra step is recommended only after utilizing the optimization procedure described in CHAPTER 5 and implementing the selected optimal design. In fact, attempting to optimize the converter design on the bench without employing a methodical and systematic approach, such as the one presented in CHAPTER 5, is not likely to produce good results. For the optimized prototype PSFB converter considered here, fine-tuning
the switching frequency on the bench at light load determined that modest efficiency improvements could be obtained by setting the switching frequency to 88 kHz. This value is hereafter referred to as the “fine-tuned” switching frequency for this system:

\[ f_{sw}(tuned) = 88 \text{ kHz} \]  
(6-1)

It is noted that the fine-tuned switching frequency value of 88 kHz is not far from the switching frequency of the optimal design (i.e. 98 kHz) that was selected by the optimization procedure. Nevertheless, as already mentioned, the very subtle difference between the light-load total loss values at these two switching frequencies is hardly recognizable by the optimization procedure.

As a final step in the optimized prototype PSFB converter evaluation, the system efficiency profile was measured a second time after configuring the system to operate at the fine-

![Figure 6-10: Efficiency comparisons of the optimized prototype PSFB converter, before and after switching frequency fine-tuning.](image)

\[ \text{Optimized PSFB Converter After } f_{sw} \text{ Fine-Tuning} \]

\[ \text{Optimized PSFB Converter} \]
tuned switching frequency. The resulting efficiency profile is plotted in Figure 6-10 along with the efficiency profile of the optimized prototype PSFB converter without this change (i.e. operating at $f_{sw} = 98 \text{ kHz}$). As shown in this figure, this small adjustment to the system switching frequency leads to marginal efficiency improvements at light load and at rated load. Specifically, the light-load, rated-load, and peak efficiencies are improved by 0.7%, 0.3%, and 0.1%, respectively. This result corroborates the benefit of performing bench-tuning of the switching frequency, as the final step to further boost the efficiency of an optimized PSFB converter.

Finally, the efficiency profile of the optimized and fine-tuned prototype PSFB converter is compared with the efficiency profile of the original prototype PSFB converter in Figure 6-11.

![Figure 6-11: Efficiency comparisons between the optimized and fine-tuned prototype PSFB converter (i.e. with $f_{sw}(tuned) = 88 \text{ kHz}$) and the original prototype PSFB converter.](image)
In contrast to the previous comparison shown in Figure 6-8, the optimized and fine-tuned prototype PSFB converter outperforms the original prototype PSFB converter at all operating conditions, including light load. As shown in Figure 6-11, the final optimized and fined-tuned prototype PSFB converter offers light-load, full-load, and peak efficiencies of 94.1%, 97.4%, and 97.6%, respectively.

The final outcome of the empirical evaluation procedures presented in this chapter further bolsters the claim that the PSFB topology in its standard structure and control strategy has great potential to achieve both very high efficiency and power density. However, this outcome relies heavily on a deep understanding of the underlying loss mechanisms of the system and the application of a systematic optimization of the system design parameters. This dissertation provides a set of previously unavailable tools that makes this process accessible to designers for the purpose of designing high-performance PSFB converters for demanding applications.
CHAPTER 7

CONCLUSION

7.1. Conclusion

Due to its soft-switching capability and ability to handle high power levels, the PSFB converter is an appealing topology in many industrial applications, such as datacenters. The advent of WBG semiconductors has enabled previously unachievable converter performance in terms of efficiency and power density. Nevertheless, optimizing the performance of complex topologies such as the PSFB converter requires understanding the interdependence of the various parameters of influence within the converter and their combinatorial effect on the performance metrics of interest.

The PSFB converter has many interdependent degrees of freedom that collectively affect the overall efficiency and performance of the system. Understanding the dependence of the ZVS mechanism on these degrees of freedom is critical to effectively optimize the PSFB converter, especially for WBG converters operating at high switching frequencies. The resonant inductor value \( L_r \), the switch output capacitance \( C_{os} \), the switching deadtime values, and the converter output power level are some of the main parameters that influence the efficiency of the system through the ZVS mechanism. This dissertation has identified the switching deadtime values as parameters of particular sensitivity for this topology. Subtle changes to the switching deadtime values can result in dramatic changes to the overall system efficiency, especially for certain combinations of other system parameters. This dissertation provides a set of empirically
validated analytical tools that provides new insight into the interdependence of these parameters and offers useful guidance to practitioners seeking to maximize the performance of this topology. Moreover, these analytical tools are employed in this dissertation during two empirical phases. In the first phase, the efficiency trends of a baseline 10-kW PSFB converter are analyzed with these tools and the converter is tuned with the available knobs in order to achieve higher efficiencies. In the second phase, these tools are employed to design and implement a 10-kW optimized PSFB converter, optimized for efficiency and power density.

The main contributions of this dissertation are as follows. First, an analytical treatment is provided for identifying the minimum and maximum switching deadtime values to achieve ZVS for each leg of the converter. This formulation takes into consideration all critical parameters upon which this selection depends, including the MOSFET output capacitance, the MOSFET body diode reverse recovery characteristics, the resonant inductor value, and the converter operating conditions. Second, this analytical formulation is empirically validated through the evaluation of a high-performance, 10 kW SiC-based prototype PSFB converter. This converter is evaluated across a wide range of component parameter values and operating conditions in order to quantitatively verify the timing threshold values provided by the analytical formulation. Third, an additional set of empirical results is utilized to perform a detailed trend analysis of the efficiency characteristics for the prototype converter under consideration. This analysis demonstrates the interdependence of several critical system parameters on determining the efficiency of this converter, primarily by their impact on the achievement of ZVS. Fourth, a MATLAB-based framework for optimizing the design of the PSFB converter with regard to efficiency and power density is presented. By leveraging loss models and volumetric models of various system components, this framework enables systematic multi-objective optimization of
the PSFB topology. This optimization enables designers of this topology to quantify the trade-off between efficiency and power density and assess the impact of specific component selection decisions. Fifth, the multi-objective optimization framework is utilized in order to design and implement an optimized prototype PSFB converter. This optimized design meets its primary design objective by simultaneously achieving improvements in both efficiency and power density compared to the original prototype PSFB converter. This outcome further validates the theoretical ZVS models presented in this dissertation, and illustrates the practical utility of the optimization procedure included herein. Sixth, by taking advantage of the trends identified in the provided analytical treatment and the empirical studies pertaining to the prototype PSFB converter, a set of practical suggestions is presented for optimizing the PSFB converter. These guidelines can be employed by designers seeking to maximize the performance of the PSFB converter in terms of efficiency and power density.

7.2. Future Work

One extension of this work would be to investigate the influence of the MOSFETs gate drive circuit on the ZVS transitions and to include its impact on the analytical ZVS models presented in this dissertation. It is noted that the impact of gate drive circuit latency on the required minimum deadtime values for achieving ZVS is often neglected in the literature. Consequently, gate drive circuit latency may have subtle but important implications for deadtime adjustment, which have not been studied in this dissertation.

Another extension of this work would be to investigate and model the effect of $C_{oss}$ hysteresis loss on the required inductive energy to achieve ZVS, especially at light load. As mentioned previously, the $C_{oss}$ loss mechanism has recently been made known and its implications are not still clearly understood by many designers, particularly for soft-switching-
based converters. Properly modeling the $C_{oss}$ loss mechanism could improve the efficacy of the ZVS models included in this dissertation.

Another extension of this work would be to include a more precise AC-resistance model of conductors in the optimization framework. Specifically, as mentioned in CHAPTER 5, the contribution of the proximity effect to the AC-resistance increase of conductors and windings did not receive adequate consideration due to the complex nature of this phenomenon. Including a reasonably accurate model of this phenomenon in the optimization framework can increase the accuracy of predictions.

Moreover, the converter transformer design did not undergo any optimization in this dissertation, as it was out of the scope of this work. As another extension to this dissertation, the transformer design can also be incorporated into the optimization procedure in order to implement a transformer that is fully optimized according to the main optimization objectives.
A.1. Hard-Switching Loss Estimation Algorithm from reference [103]

Figure A-1: The adopted flowchart from [103], showing the turn-on and turn-off hard-switching loss estimation procedure.
A.2. Validation of the Underlying Loss Models

Validating the loss models presented in section 5.4 is presented in this section. To perform this validation, the original PSFB prototype converter described in section 4.2 is employed. The measured efficiency profile of the converter is compared with the theoretical efficiency profile, which is obtained by utilizing the component loss models presented in section 5.4. It should be mentioned that this converter employs passive rectification, instead of synchronous rectification, on the secondary side. Accordingly, the calculation of rectifier losses for this example is based on diode conduction losses instead of synchronous rectifier losses.

Figure A-2 presents a comparison of the model predictions and measured values for the efficiency and total system losses of the original prototype PSFB converter. As shown in this figure, the underlying loss models provide a reasonably accurate prediction of the system

\[ P_{\text{out}} \text{(kW)} \]

\[ \eta \text{(\%)} \]

\[ P_L \text{(W)} \]

\[ P_{\text{out}} \text{(kW)} \]

\[ \text{Figure A-2: Actual and predicted efficiency and total system loss for the prototype converter of Figure 4-2 (} L_{\text{shim}} = 20 \text{ } uH, T_{d,\text{lead}} = 200 \text{ } ns, T_{d,\text{lag}} = 200 \text{ } ns). \]
efficiency over a wide range of output power levels. While slight discrepancies are observed between the model predictions and the measured results, the overall loss profile of the converter is accurately represented. The observed discrepancies can be attributed to loss mechanisms within the system, such as AC conductor impedances and nonlinear losses in magnetics, that are challenging to model accurately. In addition, there are undoubtedly stray losses in the system that the simple loss models presented in this chapter do not capture. This is why the predicted efficiency profile is higher than the measured efficiency profile at all considered load values. Therefore, the agreement shown in Figure A-2 is deemed sufficient to verify the implementation of the underlying system loss models. These models are considered sufficiently accurate to support the multi-objective optimization procedure that is the subject of CHAPTER 5.
A.3. MOSFET Candidates of the Optimization Procedure

Table A-1 presents the information of the MOSFET candidates that are used in the design of the optimized PSFB converter presented in CHAPTER 5.

<table>
<thead>
<tr>
<th>TABLE A-1: THE MAIN CHARACTERISTICS OF THE MOSFET CANDIDATES.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>------------------</td>
</tr>
<tr>
<td>$V_{DS}(\text{max})$</td>
</tr>
<tr>
<td>$R_{DS}(\text{on})$</td>
</tr>
<tr>
<td>$R_{SD}(\text{on})^1$</td>
</tr>
<tr>
<td>$I_D$</td>
</tr>
<tr>
<td>$R_{G,\text{int}}^2$</td>
</tr>
<tr>
<td>$C_{iss,\text{equ}(750V)}^3$</td>
</tr>
<tr>
<td>$C_{rss,\text{equ}(750V)}^4$</td>
</tr>
<tr>
<td>$C_{oss,\text{equ}(750V)}^5$</td>
</tr>
<tr>
<td>$C_{oss,\text{equ}(470V)}^5$</td>
</tr>
<tr>
<td>$Q_{oss}(750V)^6$</td>
</tr>
<tr>
<td>$E_{oss}(750V)^7$</td>
</tr>
</tbody>
</table>

---

1 Source-drain resistance (3rd quadrant).
2 Internal gate resistance.
3 $C_{iss,\text{equ}}(V_{DS}) = \int_{0}^{V_{DS}} \frac{V_{DS} C_{iss}(v) dv}{V_{DS}}$
4 $C_{rss,\text{equ}}(V_{DS}) = \int_{0}^{V_{DS}} \frac{V_{DS} C_{rss}(v) dv}{V_{DS}}$
5 $C_{oss,\text{equ}}(V_{DS}) = \int_{0}^{V_{DS}} \frac{V_{DS} C_{rss}(v) dv}{V_{DS}}$
6 $Q_{oss}(V_{DS}) = \int_{0}^{V_{DS}} C_{oss}(v) dv$
7 $E_{oss}(V_{DS}) = \int_{0}^{V_{DS}} \frac{V_{DS} C_{rss}(v) dv}{V_{DS}}$
A.4. Core Candidates of the Optimization Procedure

Table A-2 presents the information of the core candidates that are used in the design of the optimized PSFB converter presented in CHAPTER 5.

**Table A-2: The main characteristics of the core candidates.**

<table>
<thead>
<tr>
<th>Core Material</th>
<th>Relative Permeability ($\mu$)</th>
<th>$A_L^8 \frac{nH}{T^2}$</th>
<th>A (mm)</th>
<th>B (mm)</th>
<th>C (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetics 0055256A2 [133]</td>
<td>MPP26</td>
<td>26</td>
<td>35</td>
<td>40.77</td>
<td>23.3</td>
</tr>
<tr>
<td>Magnetics C055083A2 [134]</td>
<td>MPP60</td>
<td>60</td>
<td>81</td>
<td>40.77</td>
<td>23.3</td>
</tr>
<tr>
<td>Magnetics C055248A2 [135]</td>
<td>MPP173</td>
<td>173</td>
<td>233</td>
<td>40.77</td>
<td>23.3</td>
</tr>
<tr>
<td>Magnetics C055249A2 [136]</td>
<td>MPP300</td>
<td>300</td>
<td>403</td>
<td>40.77</td>
<td>23.3</td>
</tr>
<tr>
<td>Magnetics C055250A2 [137]</td>
<td>MPP550</td>
<td>550</td>
<td>740</td>
<td>40.77</td>
<td>23.3</td>
</tr>
</tbody>
</table>

\footnote{8 Inductance Factor.}
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