

CONTROL AND POWER MANAGEMENT SCHEMES FOR
DISTRIBUTED AND BATTERY POWERED SYSTEMS

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ABSTRACT

Battery systems are widely used in many applications including portable electronics, EVs/HEVs, and distributed smart power grids. In addition to battery technologies, the battery management system (BMS) plays a critical role in enabling the widespread adoption of battery-powered applications. This dissertation work focuses on addressing several issues and improving performance of several aspects of battery powered applications. These focused topics include online monitoring of battery impedance, charge balancing between battery cells during both discharging and charging operation, and power electronic topologies and control in order to improve reliability, efficiency, and density of the battery-powered applications.

In chapter 2, a practical method is presented in order to achieve accurate online battery impedance measurement while maintaining output voltage regulation of the power converter. The proposed method is based on converter duty cycle control and perturbation. As a result, all the external signal injection circuitries are eliminated.

In chapter 3 and 4, the charge balancing issue is addressed from the root by automatically adjusting the discharge/charge rate of each cell based on a new distributed battery system architecture with energy sharing control. The proposed energy sharing controller does not require any charge/energy transfer between the cells, thus eliminating the power losses during energy transfer process.

To gain insights into the dynamics of the energy sharing controlled distributed battery system, the state-space averaging small-signal modeling and controller design is performed in Chapter 5. Simulation and experimental results are presented for verification.

Single-inductor multiple-output DC-DC converter has gained increased popularity in the portable applications where a battery is used to power multiple loads. However, a common issue facing the SIMO converter design is the cross regulation between the multiple outputs during steady-state and dynamic operations. To address this issue, a power-multiplexed controller is presented in Chapter 6 which eliminates the cross regulation between the outputs by multiplexing the conduction of each output channels. Each output is independently regulated under steady-state and dynamic operations regardless of the operating mode, i.e., continuous or discontinuous conduction mode.

Chapter 7 summarizes this work and provides conclusions before discussing some possible future research directions related to this dissertation work.

LIST OF ABBREVIATIONS AND SYMBOLS

EVs	Electric Vehicles
PHEVs	Plug-in Hybrid Electric Vehicles
BMS	Battery Management System
SOC	State-of-Charge
SOH	State-of-Health
SIMO	Single-Inductor Multiple-Output
NiMH	Nickel-metal-hydride
$C_{\text{available}}$	The amount of charges remaining in the battery
C_{max}	The total amount of charges when the battery is fully charged
ANN	Artificial Neural Network
OCV	Open Circuit Voltage
CAN	Control Area Network
EIS	Electrochemical Impedance Spectroscopy
HCSD	Harmonic Compensated Synchronous Detection
PM	Power Multiplexed

DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
$V_{oc}(SOC)$	SOC dependent voltage source
$Z_{battery}$	Impedance of the battery
f_p	Perturbation frequency
V_{ac}	Amplitude of the AC component of the battery voltage
I_{ac}	Amplitude of the AC component of the battery current
ϕ_z	The phase of the battery impedance
V_{o_dc}	DC output voltage
D_{dc}	DC duty cycle
$V_{battery_dc}$	DC voltage of the battery
$I_{battery_dc}$	DC current of the battery
T_1	Instant when impedance measurement mode is triggered
d_{ac}	Small duty cycle sinusoidal perturbation signal
D_{ac}	Amplitude of the small duty cycle sinusoidal perturbation signal
$V_{battery-pp}$	Peak-to-peak value of the battery voltage
$I_{battery-pp}$	Peak-to-peak value of the battery current

M	Number of cycle $V_{\text{battery-pp}}$ and $V_{\text{battery-pp}}$ are measured
TH_1	Threshold for $V_{\text{battery-pp}}$
TH_2	Threshold for $I_{\text{battery-pp}}$
q	Quantization error
ADC	Analog-to-Digital Converter
LSB	Least significant bit
V_{range}	Input analog voltage range of the ADC
N	The number of bits of the ADC after analog to digital conversion
φ_v	Phase of the AC voltage
φ_i	Phase of the AC current
f_{sw}	Switching frequency
X_{valley}	Register in the digital controller that holds the valley value of the signal
X_{peak}	Register in the digital controller that holds the peak value of the signal
TI	Texas Instruments Corporation
d	Duty cycle of the power converter
C-rate	The rate at which the battery discharges or charges normalized to the capacity of the battery

DOD	Depth of discharge
OCV_{est}	Estimated OCV value of the battery
V_{ref}	Output voltage reference value of the power converter
V_{ref_dc}	DC Output voltage reference value of the power converter
V_{ref_ac}	AC Output voltage reference value of the power converter
f_k	K^{th} perturbation frequency
A_k	Amplitude of the sinusoidal wave with the frequency of f_k
θ_k	Phase delay of the sinusoidal wave with the frequency of f_k
B.C.	Balancing circuit
ZCS	Zero-current switching
BPM	Battery power module
DCR	DC resistance of the inductor
ESR	Equivalent series resistance of the capacitor
PCB	Printed circuit board
$V_{bus-ref}$	The DC bus voltage reference
V_{r-ref}	output voltage reference for the power converter in BPM_r
α_{vr}	Voltage multiplier in discharge mode

M_v	The sum of the voltage multiplier values in discharge mode
V_r	The output voltage of BPM_r power converter
V_{bus}	DC bus voltage
V_{pack}	Battery pack voltage
$G_{vB}(s)$	Continuous-time transfer function of the compensator used in the voltage control loop in discharge mode
$G_{vB}(z)$	Discrete-time transfer function of the compensator used in the voltage control loop in discharge mode
PID	Proportional-Integral-Derivative
SOC_{v-ref}	The reference SOC in discharge mode
β_{vr}	The SOC balancing loop multiplier in discharge mode
N_{v_active}	The number of active BPMs
δ_r	Enable/Disable multipliers
G_{dhgr}	DC voltage gain for the power converters in BPM_r in discharge mode
Z_{cellr}	Z_{cellr} is the internal impedance of the battery cell _r
V_{cell}	Cell voltage
I_o	Load current

DPWM	digital Pulse-Width-Modulation
CCCM	Constant current charging mode
CVCM	Constant voltage charging mode
I_c	Capacity current
V_{max}	The maximum charging voltage of the battery
M_i	The sum of voltage multipliers in charge mode
$I_{cell-avg}$	The average cell current in charge mode
$V_{cell-avg}$	The average cell voltage in charge mode
G_{chgr}	DC voltage gain for the power converter in BPM _r
η_r	Efficiency of the BPM _r
P_{or}	Output power of the BPM _r
P_{inr}	Input power of the BPM _r
T_{vr-dhg}	BPM _r output voltage control loop gain in discharge mode
$T_{socr-dhg}$	BPM _r SOC control loop gain in discharge mode
S_{lr}	Low-side switch in BPM _r power converter
S_{ur}	High-side switch in BPM _r power converter
T_s	Switching period of the BPM power converter

X	Equilibrium state vector
μs	Microsecond
$G_{vdr-dhg}(s)$	Duty cycle control to BPM_r converter output voltage transfer function in discharge mode
$G_{idr-dhg}(s)$	Duty cycle control to $cell_r$ current transfer function in discharge mode
$Z_{or}(s)$	Open loop output impedance of the BPM_r
$G_{socir-dhg}$	Cell _r current I_{cellr} to SOC_r transfer function for BPM_r
T	Sampling period of the SOC value
Q	Rated capacity of the cell in coulomb
$F_{mr-dhg}(s)$	DPWM _r modulator gain in discharge mode
$T_{vr-dhg-uncomp}(s)$	uncompensated BPM output voltage loop gain in discharge mode
RHP	right-half-plane
$G_{vBr}(s)$	Continuous-time BPM output voltage control loop compensator in discharge mode
$G_{vBr}(z)$	Discrete-time BPM output voltage control loop compensator
$T_{outer-dhg-uncomp}(s)$	Uncompensated outer loop gain in discharge mode
$G_{vSOCr}(s)$	Continuous-time BPM SOC control loop compensator in discharge mode

$G_{vSOCr}(z)$	Discrete-time BPM SOC control loop compensator in discharge mode
$G_{vdr-chg}(s)$	Duty cycle control to BPM input voltage transfer function in charge mode
$G_{idr-chg}(s)$	Duty cycle control to cell _r current transfer function in charge mode
$G_{socir-chg}$	cell _r current to cell _r SOC transfer function in constant current charging mode
$T_{vr-chg-uncomp}(s)$	uncompensated BPM input voltage loop gain in charge mode
$T_{outer-dhg-uncomp}(s)$	Uncompensated outer loop gain in charge mode
$G_{cell}(s)$	Average cell current control loop compensator
$G_{vcellrd-chg}(s)$	Duty cycle control to cell _r voltage transfer function
$G_{vmB}(s)$	Average cell voltage control loop compensator
<i>PMIC</i>	Power management integrated circuit
<i>RF</i>	Radio frequency
<i>LCD</i>	Liquid crystal display
<i>SOC</i>	System-on-chips
f_o	Switching frequency of the output switches in SIMO converter
T_d	Dead time between the commutation of the output switches

V_{in}	Input voltage of the SIMO converter
ΔI_{Ll}	Change in the inductor current
S_{or}	r^{th} output switch
V_{or}	Output voltage of r^{th} channel in SIMO converter
$T_{rs_chl_opt}$	Optimal inductor current reset value for channel one
$PCBS$	Parallel connected battery strings
$SCBG$	Series connected battery groups
N_p	The number of cells in parallel connection
N_s	The number of cells in series connection

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CHAPTER 1

INTRODUCTION

1.1 Overview

Electrochemical batteries are widely used in a variety of applications such as portable electronics, Electrical Vehicles (EVs)/Plug-in Hybrid Electric Vehicles (PHEVs), and distributed microgrids to store and supply electrical energy thanks to their high energy density [1-6]. The battery, such as lithium-ion chemistry, is typically comprised of two electrodes which are isolated by a separator and soaked in the electrolyte in order to facilitate the movement of ions [A12-A13]. While the battery chemistry has evolved over the past few decades [7, 12-13], the growth of battery capacity and energy density is slower than desired for many applications such as EVs and mobile devices.

In parallel with the advances of battery technology, battery management system (BMS) performance is another key factor enabling the widespread adoption of technologies such as EVs/PHEVs [1, 6-7, 11, 14] and distributed microgrids [2-5], among other emerging applications. The BMS plays a critical role in ensuring safe, reliable, and efficient operation of the battery energy storage system (BESS).

A BMS typically incorporates several functional blocks, which are covered next in this chapter. Some of the common design techniques associated with each functional block are presented and discussed. This dissertation work focuses on addressing some of the issues/needs associated with battery systems and their applications including: (1) The need for practical online battery impedance measurement which can potentially be utilized in the future as an input

for effective diagnostic tool for state-of-charge (SOC) and state-of-health (SOH) estimation; (2) the need for more reliable and efficient battery cells SOC balancing during battery discharging and charging operation in order to avoid cell over/under charging/discharging while being able to increase system capacity utilization; (3) the need for high efficiency and high power density power electronic converters especially when battery is used to power multiple electronic loads.

1.2 Architecture of Battery Energy Storage Systems

A state-of-the-art battery energy storage system is comprised of two major parts, i.e., battery cells (e.g. put in the form of battery pack) and BMS. The major desired BMS functions include SOC estimation, SOH monitoring, control and management of discharge/charge operation, and temperature monitoring and cooling, communications [1-7]. Depending on the application, the battery energy storage systems vary widely in architecture, battery chemistry, functional blocks, size, thermal and mechanical design, among others.

Battery energy storage system is widely used in portable electronics applications such as cellular phone, tablet and notebook [8-10] to power various electronic loads such as application/baseband processor, Liquid Crystal Display (LCD) screen and RF power amplifier. In such portable electronics applications, the battery energy storage system typically consists of a single or a small number of lithium-ion battery cells in addition to several BMS functional blocks including:

- (1) Cell monitoring (voltage, current and temperature) and protection [40-41]
- (2) Charge control [42-43]
- (3) Fuel gauge to provide SOC estimation [42-43]

For high-power energy storage applications, such as EVs/PHEVs and distributed microgrids, the complexity, size, cost and weight of the battery system are increased substantially compared to that used in portable electronics applications [1-6, 11]. The battery pack in such high-power applications generally consist of a large number of battery modules connected in series and/or in parallel in order to provide higher voltage and current to the load. Each battery module is made up of many cells connected in series and/or parallel as well. Such modularized structure provides better controllability and higher robustness as the BMS control algorithms can be implemented at three different levels, i.e., cell level, module level, and pack level.

As the number of cells in the battery pack increases, the cell monitoring and protection circuitries get more complex, costly, and occupy larger space. More sophisticated BMS functions are required in order to guarantee efficient and robust operation of the battery system. One of the common issues associated with such high-power energy storage systems is the charge imbalance between the cells. During discharging (or charging) operation, the SOC values of the cells may be different due to reasons such as manufacturing tolerance, non-uniform temperature distribution across the cells/modules in the battery pack, and non-uniform aging. As a result, some of the cells are fully discharged or fully charged earlier than the other cells. In that scenario, the whole battery system should be shut down immediately in order to prevent overdischarging of the cells fully discharged, or prevent overcharging of the cells fully charged. This, however, would result in waste of the energy remaining in those cells which have not yet been fully discharged or result in not charging the system to its full potential during charging operation (system potential capacity is not fully utilized). To address this issue, cell balancing function is needed to ensure that the SOC values of the cells are balanced while they are being

discharged or charged and subsequently reach the end of discharge cycle or charge cycle simultaneously. It should be noted that in order to achieve cell balancing the cells may not be discharged or charged at the same rate due to different characteristics of each cell such as health condition, internal impedance, and capacity, among other factors.

In addition, thermal management is especially crucial in the high-power battery energy storage systems as the large amount of heat generated during discharging and charging operations can cause performance degradation, or in a worse case scenario, catastrophic failure of the battery pack if heat is not properly controlled and removed.

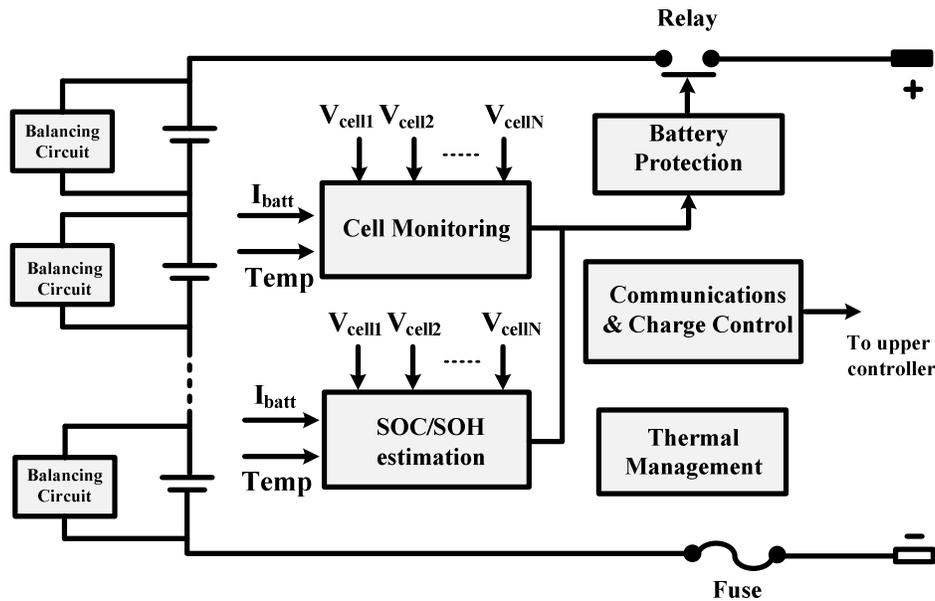


Figure. 1.1: Conceptual block diagram of a next-generation BMS

Fig. 1.1 illustrates key functional blocks of a next-generation BMS. Depending on the application requirement, the actual BMS used in a specific application may consist of only part of those features shown in Fig. 1.1. For instance, in portable applications, cell balancing circuitries and associated controller are not needed. Although it is significantly beneficial to have accurate estimation of the SOH of the battery while it is running, this feature has not yet been

fully demystified, and therefore, has not been extensively applied to the practical battery system applications due to the complexity of the factors which can impact the SOH of the battery. Each of the functional blocks shown in Fig. 1.1 are introduced in the following subsections.

A. Battery Pack/Cell(s)

Battery pack varies widely in size ranging from a single cell to thousands of cells depending on the application and single cell size/capacity. Different battery chemistries find use in different applications according to their unique performance characteristics and the application requirements. The most commonly used rechargeable battery chemistries include lithium-ion, lead acid, nickel-metal-hydride (NiMH), and nickel-cadmium. The characteristics of these commonly used battery chemistries are listed in Table 1.1.

Table 1.1: Characteristics of Several Popular Rechargeable Battery Chemistries [7, 12-13]

Battery Chemistry	Pros	Cons
Lithium-ion	<ul style="list-style-type: none"> ▪ High energy density ▪ Low memory effect ▪ Long cycle life ▪ Low self-discharge rate ▪ Light weight ▪ Low maintenance cost ▪ Less environmental impact 	<ul style="list-style-type: none"> ▪ More delicate ▪ Sensitive to overdischarge and overcharge ▪ Need protection circuit for safety
Lead acid	<ul style="list-style-type: none"> ▪ Rugged ▪ Economic cost 	<ul style="list-style-type: none"> ▪ Low specific energy ▪ Limited cycle life ▪ Lead is toxic and can't be disposed in landfills
Nickel-cadmium	<ul style="list-style-type: none"> ▪ Mature and well understood ▪ Long service life ▪ High discharge/charge rate ▪ Able to work at extreme temperatures ▪ Rugged and enduring 	<ul style="list-style-type: none"> ▪ Cadmium is toxic and can't be disposed in landfills
Nickel-metal-hydride	<ul style="list-style-type: none"> ▪ A practical replacement for Nickel-cadmium ▪ Higher specific energy than Nickel-cadmium 	<ul style="list-style-type: none"> ▪ Mild toxic metals

Due to the advantages including high energy density, long cycle life, low memory effect, less environmental impact, and low self-discharge rate, lithium-ion chemistry has received the most significant attention in the past decade and become increasingly popular in portable electronics, EVs/PHEVs, and distributed microgrids energy storage applications. The lithium-ion family of batteries has been gradually replacing the nickel and lead-acid based chemistries which has dominated the battery world until the 1990s [12-13].

B. Cell Monitoring and Protection

Voltage, current and temperature of each cell in the battery pack are constantly monitored for various purposes including

- 1) Protect the cell from overdischarge and overcharge which is hazardous to the cell, especially for lithium-ion chemistry
- 2) Protect the cell from being discharged/charged at excessive rates which can greatly shorten the usable capacity and cycle life of the cell
- 3) Maintain appropriate operating temperature range to optimize battery performance
- 4) Provide voltage, current and temperature inputs to the SOC and/or SOH estimation algorithms

C. State-of-Charge Estimation

State-of-charge (SOC) is one of the most important state indicators for the battery. It is generally defined as the ratio of the amount of charges remaining in the battery (Q_r) to the total amount of charges (Q_f) when the battery is fully charged, as given by

$$SOC = \frac{Q_r}{Q_f} \quad (1.1)$$

In other words, SOC indicates the amount of electrical energy the battery is able to supply before it is depleted. The purposes of battery SOC estimation include but are not limited to the following:

1. Avoid overdischarging/overcharging of the battery
2. User convenience
3. Required for cell balancing

A variety of approaches have been proposed in the literature as those presented in [12-18] to estimate the SOC of the battery. These SOC estimation methods can be classified into the following categories:

- 1) Coulomb counting method [12]. By integrating the current flowing in and out of the battery over time, the amount of charges available in the battery can be estimated. Despite its simplicity, the coulomb counting method does not take into account some key factors that can affect the accuracy of SOC estimation, such as the temperature variation, charge/discharge rate and battery aging effect. Moreover, the coulomb counting method is sensitive to the accuracy of the initial current value and current measurement.
- 2) OCV-based method [14]. This method requires that the battery stay in relaxation mode for sufficient amount of time, e.g. one hour, prior to open-circuit-voltage (OCV) measurement, which is not practical for online real-time applications. In addition, this method is sensitive to the voltage measurement error. Fig. 1.2 sketches the relationship between the OCV and SOC of a lithium-ion battery. It can be observed that the voltage curve is flat over the SOC range of 30% to 70%. This implies that even a small measurement error can cause significant SOC estimation inaccuracy.

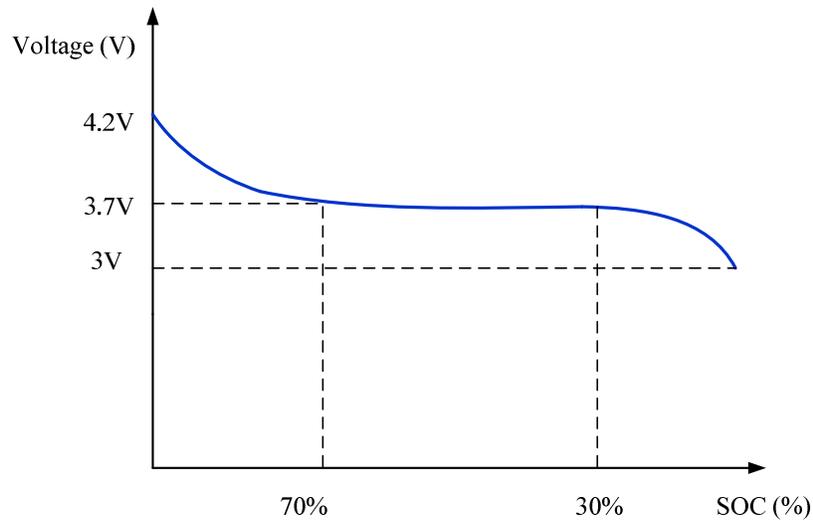


Figure. 1.2. A sketch of OCV vs. SOC for a lithium-ion battery

- 3) Electrochemical model-based methods [18]. Despite their accuracy, this type of methods generally are based on solving the detailed nonlinear differential equations which describe the electrochemical behavior of the battery. This requires significant computational resources, and therefore, are not suited for online real-time applications.
- 4) Electrical circuit model-based methods [19-22]. This type of methods require electrical battery models which characterize electrochemical behavior and dynamics of the battery. Adaptive and non-linear techniques, such as extended Kalman filter and sliding-mode observer, can be used to improve the accuracy of the electrical circuit models. However, these techniques would increase the complexity of implementation. Moreover, the estimation error could be large due to the noise present in the system.
- 5) Computational intelligence-based methods, such as artificial neural network (ANN), fuzzy logic method and support vector regression methods [23-25]. The disadvantage of this type of methods is the need for learning/training process with a large amount of prior data/knowledge.

D. State-of-Health Estimation

State-of-health (SOH) is another important state indicator for the battery. Unfortunately, there has been no established definition of the SOH. In some literature [20, 23, 26], SOH is defined as the ratio of the present usable/available capacity (C_a) to the rated capacity of the battery (C_r), as given by

$$SOH = \frac{C_a}{C_r} \quad (2)$$

SOH can be used as a measure of the health condition of the battery and its ability to deliver specified performance compared with a fresh battery. Like human being, the health condition of the battery tends to deteriorate over time due to irreversible physical and chemical changes occurring with usage [13].

In general, capacity and impedance variation of the battery are regarded as the leading indicators of the SOH of the battery [15-16, 20, 23, 26]. Unlike the estimation of the SOC, SOH estimation does not usually have stringent requirement of the tracking/estimation speed due to much slower dynamics associated with the variation of the SOH. Several SOH estimation methods have been presented in the literature, the majority of which fall into two categories, i.e., capacity estimation and computational intelligence-based techniques [27-30].

AC battery impedance data have been shown to be effective in reflecting variations in the electrochemical processes which reveal the changes taking place in the battery electrode surface and diffusion layer [31]. Therefore, AC impedance of the battery can potentially be utilized as an effective tool for assessing the health condition of the battery, as will be discussed in details later in this chapter.

E. Battery Modeling

A model which represents the electrochemical characteristics and dynamics of the battery is essential for the states (e.g., SOC and SOH) estimation, circuit simulation and analysis, and battery design and characterization. A wide variety of battery models have been presented in the literature [18-20, 26-31]. These models have varying degrees of complexity and accuracy. In general, these models fall under three categories, i.e., electrochemical models, analytical models and electrical circuit models.

As mentioned earlier, electrochemical models are based on detailed nonlinear differential equations which describe the chemical reactions that occur inside the battery. Despite their high accuracy, these models do not usually find practical use in real-time applications due to the need of detailed knowledge of the battery chemical processes and much computational resources.

Analytical models are basically the simplified electrochemical models with reduced order of equations [32-34]. One of the example analytical models is called Peukert's law which describes the relationship between the discharge rate and the runtime of the battery [34]. Peukert's law, however, does not consider many other factors, such as recovery effect of battery.

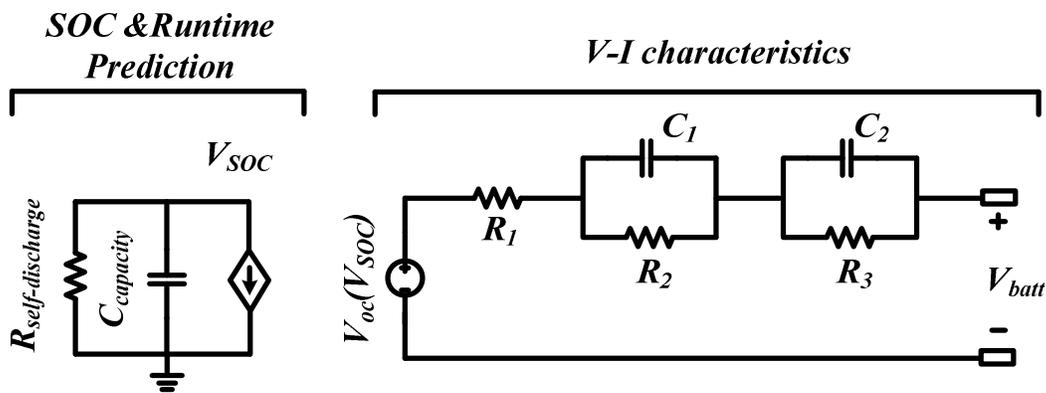


Figure.1.3: An example electrical battery model[19]

To overcome the disadvantages of the previous two type of models, the electrical circuit models are more commonly utilized. Electrical circuit model, comprised of voltage source, resistances and capacitances, is capable of capturing I-V characteristics of the battery during

discharging and charging operation. Fig. 1.3. shows an example electrical circuit battery model [19]. By identifying the RC parameters of the model based on the measured voltage, current and temperature information, the SOC and SOH of the battery can be estimated in real time. There are some other battery models which combine the analytical model and electrical circuit model, as the one presented in the literature [20].

F. Cell Balancing

In multi-cell battery systems, in order to ensure charge balance between the battery cells during discharging and charging operation, cell balancing circuits and controls are needed as an integral part of the BMS. More details regarding the cell balancing will be available later in this chapter.

G. Charge Control

Different battery packs have different charge rate limit depending on the chemistry, capacity and series/parallel configuration of the cells being used. The objective is to achieve highest possible charging speed without compromising the charging efficiency, safety and life of the battery. This would require coordination of BMS and battery charge controller [40-41].

H. Thermal Management

The chemical reactions that occur inside the battery is dependent on temperature. The nominal battery performance is generally specified over a temperature range which may vary by applications. Operating at high and low temperatures can cause the battery performance to deviate from the nominal performance. For instance, operating at low temperature results in lower usable capacity of the battery. Therefore, thermal management is necessary for the battery system in order to deliver its specified performance. By performing heat-transfer analysis of the

battery pack based on its cell chemistry and architecture, liquid or air cooling can be used to remove the heat.

I. Communication

Communication is another important building block of the BMS functions. For example in the EVs/PHEVs applications, the BMS is usually coupled to other vehicle systems which communicate with the BMS via CAN communication interface. In some cases, there may also be system programming, monitoring and data logging requirements using RS232 series bus [13].

1.3 Battery Impedance Measurement

While the battery can be electrically modeled as a combination of voltage source, capacitors and resistors, it is a challenging task to accurately identify each of the model parameters which adaptively vary with many factors in real time, such as SOC, temperature, discharge/charge rate. Impedance, as a lumped representation of the RC network in the model, can be an effective tool to reveal the electrochemical characteristics of the battery. The impedance of the battery provides useful information on the performance of the battery and can also help to detect trouble spots hidden in the battery since the degradation of electrodes and electrolyte should be reflected in the variation of the impedance [12-13]. The battery impedance variations across different frequency ranges are revealed to be directly correlated to the health condition of the battery [15, 30-31]. Therefore, battery impedance measurement can potentially be used as an effective tool to assess the SOH of the battery.

The battery AC impedance spectroscopy can also be used to estimate the SOC of the battery by comparing the measured electrochemical impedance spectrum against the long-term experimental data collected across the full SOC range [15].

Offline battery impedance measurement methods, such as electrochemical impedance spectroscopy (EIS), has been extensively studied in the literature [28-31]. In EIS, a small charge neutral AC voltage/current signal is applied to the battery and the current/voltage response of the battery is captured to determine the impedance of the battery at a given frequency. A frequency sweep over a specified frequency range is performed in order to draw an impedance spectrum of the battery. Since the EIS measurement are performed sequentially, it can take a long period of time to complete, which make it not ideal for online real-time applications such as EVs/PHEVs and smart grids. In addition, EIS measurements require extra signal injection circuit/hardware. For these reasons, EIS measurement is generally limited to lab characterization and testing.

Despite rapidly growing demands in real-time applications, online fast battery impedance measurement has not been discussed extensively in the literature. A method named "Harmonic Compensated Synchronous Detection (HCSD)" is presented in [31] where an AC current signal composed of a sum of sinusoidal waves with a range of frequencies is injected to the battery. The impedance of the battery at each frequency of interest is then determined simultaneously. The duration of a complete measurement cycle can be reduced to a period of the lowest injected frequency. However, this method still requires signal injection through external circuits. Moreover, this method have only been tested under the scenario where the battery is directly connected to an emulated load. This rarely is the case in practical online applications where the battery typically is interfaced to the load via a DC-DC switching power converter in order to provide necessary voltage/current regulation. The transfer function and impedance of the power converter or power system may impact the accuracy of the impedance measurement with the HCSD method.

One of the major focuses of this dissertation work is on proposing and developing a true online battery impedance measurement method. In the proposed method, instead of injecting AC signal through external generator, the duty cycle value of the DC-DC power converter that interfaces the battery to the load is perturbed in a sinusoidal manner at a given frequency around its steady-state DC value. The resulted sinusoidal ripples of the battery voltage and battery current are measured in order to determine the AC impedance of the battery at the perturbation frequency. The proposed method can be performed either continuously or periodically without interrupting the normal operation of the battery system and DC-DC power converter. This work also provides an example where the obtained impedance data is utilized for online SOC estimation of lithium-ion batteries.

1.4 Cell Balancing

The second focus of this dissertation work is on cell balancing. As briefly introduced earlier in this chapter, cell balancing circuits and associated controller can be implemented as an integral part of the battery management system (BMS) in order to ensure uniform discharging/charging between the battery cells.

A wide variety of cell balancing methods have been presented in the literature which will be reviewed and discussed in details in chapter 3. In general, the cell balancing methods fall into two main categories: passive (dissipative) and active (energy-recovery) cell balancing schemes. Passive cell balancing schemes basically dissipate the excess energy of the cells that have higher SOC values in the form of heat. On the other hand, active cell balancing methods achieve cell balancing by transferring/redistributing the excess energy between the battery cells or between the cells and the pack. Therefore, active cell balancing schemes generally are more efficient but more costly and complex to implement than passive cell balancing schemes.

In this dissertation work, the cell imbalance issue is addressed from a totally different perspective than existing solutions. An energy sharing based cell balancing control scheme is proposed for a distributed battery energy storage system architecture. Instead of treating the cell balancing system and DC bus voltage regulation system as two independent systems, the proposed distributed battery system architecture with energy sharing controller combines these two systems into a single system. The re-designed DC-DC power stage with the proposed energy sharing controller is utilized to achieve SOC balancing between the battery cells and DC bus voltage regulation at the same time. The cells' SOC imbalance issue is addressed from the root by using the energy sharing control concept to automatically adjust the discharge/charge rate of each battery cell while maintaining total regulated DC bus voltage. The energy transfer between the battery cells which is usually required in the conventional cell balancing schemes is no longer needed. As a result, the power losses along the energy transfer path are eliminated. Due to the difference in the nature of discharging and charging operation, the energy sharing controller design and implementation are different in discharge and charge mode.

1.5 Cross Regulation of Single-Inductor Multiple-Output DC-DC Switching Converters

Single-Inductor Multiple-Output (SIMO) DC-DC switching converter is a cost-effective alternative to multiple-individual-switching-converter architecture in many applications such as battery-powered portable devices [35-39]. Fig. 1.4 shows a comparison between a multiple-individual-buck-converter architecture and a buck-derived SIMO converter powered by a single battery power source. The advantages of the SIMO converters include reduced number of components, footprint, and cost in addition to eliminating the mutual coupling between the power inductors.

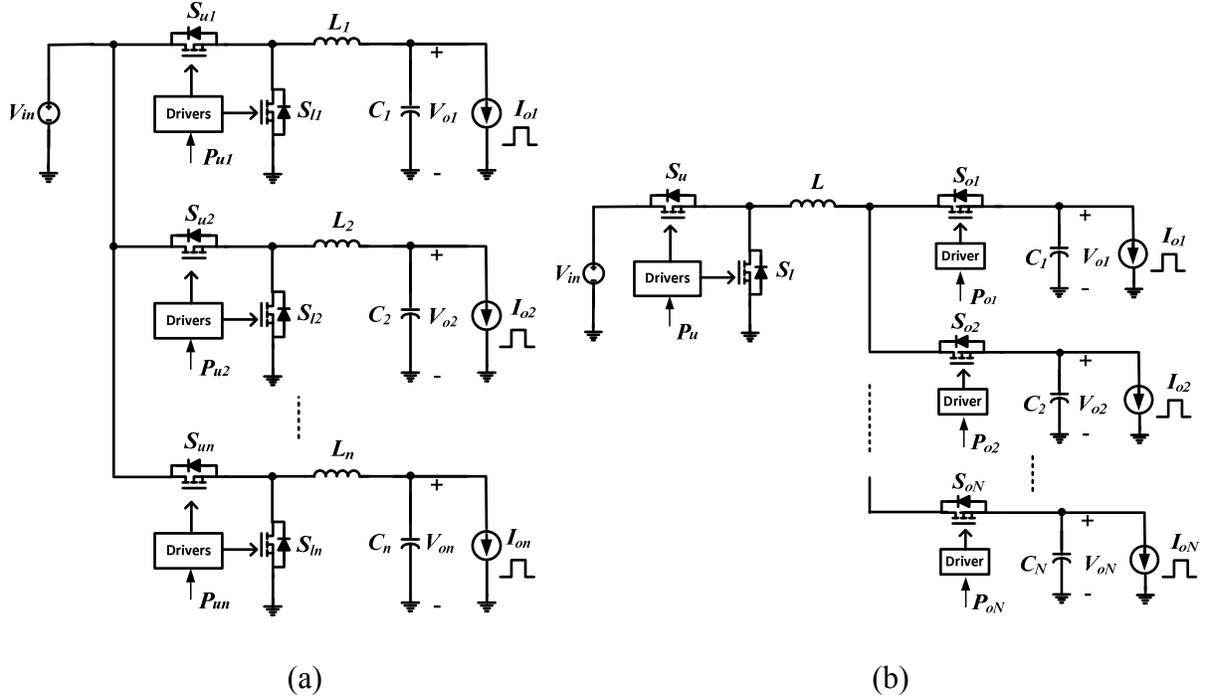


Figure. 1.4: Circuit diagram of (a) multiple switching DC-DC power converter architecture (b) single-input multiple-output switching DC-DC power converter architecture

However, due to the fact that the multiple output voltage rails are coupled to the same switching node in a SIMO converter, the cross regulation between the outputs can severely degrade the output voltage regulation performance during steady-state and dynamic operations and may even cause system instability in a worst case scenario. To address this issue, this dissertation work proposes a new control scheme called power-multiplexed control (PM control). By operating the output switches at a lower frequency than the power stage switches, each output is independently regulated when the corresponding output switch is turned on. This PM control scheme completely eliminates the cross regulation between the outputs under both steady-state and dynamic operations regardless of the operating mode, i.e., CCM (continuous conduction mode) or DCM (discontinuous conduction mode).

1.6 Dissertation Outline

Next chapter presents an online battery impedance measurement method. The theoretical basis of the proposed method is first introduced followed by implementation details of each block of the digital controller. The experimental results are then presented to validate the proposed method. An example is also provided at the end of Chapter 2 where the obtained impedance data are used to estimate the SOC of a lithium-ion battery.

Chapter 3 presents an energy sharing controller based on a distributed battery energy storage system architecture which results in achieving cell balancing between the battery cells while regulating the DC bus voltage during discharging operation. The distributed battery system architecture is first introduced and compared against the conventional centralized architecture in terms of structure, operation, control strategy, among others. Then the operation of the proposed energy sharing controller is introduced and discussed in details in the context of discharging operation. The steady-state analysis of the distributed battery system with the energy sharing controller is also presented in this chapter. The operation and design of each control loop are covered in Chapter 3. Experimental results are presented in the last section of Chapter 3 to demonstrate the effectiveness and feasibility of the proposed concept.

Since the battery charging operation is quite different than discharging operation by nature, the energy sharing controller proposed in Chapter 3 is upgraded by integrating the energy sharing control concept with a battery charging control algorithm in order to achieve cell balancing while the battery is being charged. The principle of operation of different control loops, including SOC balancing, BPM converter input voltage regulation and average cell current/voltage control loops, are discussed in details in Chapter 4. The experimental results for both constant current charging mode (CCCM) and constant voltage charging mode (CVCM)

operation are also given for verification. At the end of Chapter 4, several comments are made regarding the energy sharing controlled distributed battery system in terms of the size, cost, efficiency.

In order to understand the dynamics and provide insights to the energy sharing control loop design, small-signal modeling and analysis of the energy sharing controlled distributed battery system is performed and presented in Chapter 5. The small-signal models are constructed and associated transfer functions are derived for different operating modes including discharging, constant current charging and constant voltage charging mode. Based on the derived small signal models, the control loops are compensated by using the rule-of-thumb frequency-domain design guidelines. Simulation and experimental validation are conducted on a two-cell distributed battery system prototype to prove the effectiveness of the derived small signal models and designed compensators.

Chapter 6 presents the PM control for SIMO converters in order to eliminate the cross regulation between the outputs of a SIMO converter. The architecture of the SIMO topology and the basic operation principle of the PM control scheme are first presented and discussed. The steady-state operation analysis of the PM controlled SIMO converter during both DCM and CCM operations are also presented. Experimental results obtained from a two-output buck SIMO converter prototype are presented and discussed to verify the proposed concept .

The last chapter summarizes and concludes this dissertation research work in addition to giving some directions for future work.

CHAPTER 2

ONLINE BATTERY IMPEDANCE MEASUREMENT METHOD

2.1 Introduction

The electrochemical batteries have been extensively used for energy storage and supply in industrial, telecommunications, medical, electric utility, consumer and portable electronics applications [1-5, 1-7]. In the past decade, a variety of emerging applications that require batteries have received significant attentions including portable electronics (e.g. smart phones and tablets), EVs and smart grids. The battery energy storage system plays a key role in such applications because it can significantly impact the performance, life, cost, reliability and safety of such systems. While rapid progress has been made in terms of the battery technologies, few transformative advances have emerged in regard to the BMS that is needed to ensure efficient, safe and robust operation of the battery pack [7].

A state-of-the-art BMS typically implements various functions and capabilities including cell-level voltage, current and temperature monitoring and protection, battery pack prognosis and diagnosis, state of charge (SOC) estimation and state of health (SOH) estimation, cell balancing, and/or communications, among others [14-17, 27-30, 44-50]. The impedance of the battery is an important parameter because it provides useful information on the performance of the battery and can also help to detect trouble spots hidden in the battery system [15-17, 27-30, 44-50].

To achieve efficient power and energy management of the battery system, accurate SOC information of the battery is needed as a measure of the electrical energy remaining in the battery. Several SOC estimation methods have been proposed as in the literature [15-17, 27, 48-50, 57]. Some of the commonly used methods have been reviewed and compared in Chapter 1.

Among these methods, battery impedance based approaches can potentially result in higher accuracy of estimation as the impedance itself already takes into account several factors, such as capacity variation and temperature variation, which are usually neglected in other methods.

As the battery ages, the impedance of the battery tends to increase. Comparing the actual impedance with either the impedance when the battery was new or a reference impedance value that is set based on long-term experimental data can be utilized as a measure of the SOH of the battery [29]. AC impedance spectroscopy method [15-16, 30, 44, 46-47] can also be used to estimate the SOH of the battery based on analyzing the impedance spectra.

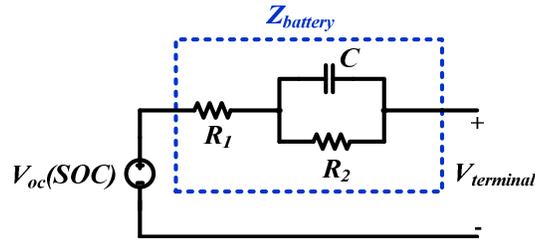


Figure. 2.1: A typical simplified electrical battery model

Fig. 2.1 shows a typical simplified electrical battery model. In addition to the SOC dependent-voltage source $V_{oc}(SOC)$, an ohmic resistor R_1 and one RC network are used to characterize the steady-state and transient response of the battery. R_1 , R_2 , and C constitute the battery impedance $Z_{battery}$. The value of $Z_{battery}$ depends on a number of factors including electrochemical properties, SOC, temperature, age and size of the battery [15-17, 27-30, 44-47].

Several battery impedance measurement methods have been proposed in the literature [28-30, 44-45]. These methods can be classified into two main categories: DC (direct current) load method and AC signal injection method. As illustrated in Fig. 2.2 (a), in the DC load method, the battery is first discharged with a DC load current of I_1 for a duration of T_1 and then with another load current of I_2 for a duration of T_2 . The DC impedance of the battery in this method is determined by

$$z_{battery_dc} = \frac{V_1 - V_2}{I_2 - I_1} \quad (2.1)$$

where V_1 and V_2 are the terminal voltages of the battery under DC load current values of I_1 and I_2 , respectively. As the name suggests, the DC load method yields only the ohmic DC resistance value of the battery.

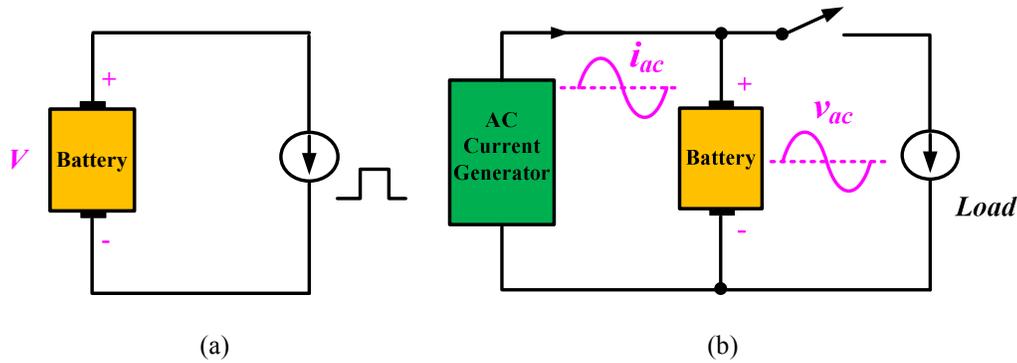


Figure. 2.2: (a) Circuit diagram of DC load impedance measurement method; (b) Circuit diagram of AC signal injection impedance measurement method

On the other hand, the AC signal injection method is more often used for AC impedance measurement of the battery. The basic idea of the AC signal injection method is to excite the battery with a small AC sinusoidal current/voltage signal at a given frequency f , as illustrated in Fig. 2.2 (b), and then measuring the AC voltage/current response of the battery to the injected AC current/voltage signal in order to determine the AC impedance of the battery by using (2.2).

$$z_{battery}(f) = \frac{V_{ac}}{I_{ac}} e^{j\varphi_z} \quad (2.2)$$

where V_{ac} and I_{ac} are the amplitudes of the AC component of the battery voltage and battery current, respectively, and φ_z is the phase of the battery impedance. The AC signal injection method is relatively complicated and costly due to the need for extra devices/circuitries to generate the required AC excitation signal and to measure the response.

Moreover, in what is referred to in the literature as “online impedance measurement” methods [28-30, 44-46], the battery under test is typically directly connected to an emulated constant current or constant resistive load (e.g. using a commercial battery tester), as illustrated in Fig. 2.2 (a) and (b), instead of being connected to an actual running system. In the latter case, a power converter is usually used to interface the battery with the load in order to provide necessary voltage/current regulation. Therefore, the transfer function and impedance of the power converter or power system, which is connected to the battery, might impact the accuracy of impedance measurement, which has not been discussed clearly in the literature [28-30, 44-45]. Other potential issues include system instability, interruption of the power converter normal operation, and/or noise and disturbance from the injected AC signal.

In this chapter, a true “online” battery impedance measurement method is first proposed. The term “online” here refers to the fact that the battery impedance measurement is performed during system operation. In the proposed method, instead of injecting AC signal through external generator, the duty cycle value of the DC-DC power converter, which is used to interface the battery with the load, is perturbed in a sinusoidal fashion at a given frequency around its steady state DC value (the duty cycle value needed to achieve a desired output voltage regulation). This duty cycle perturbation results in sinusoidal variations of the battery voltage and battery current around their corresponding steady-state DC values. The sinusoidal ripples of the battery voltage and battery current are then measured and used to determine the AC impedance of the battery at the perturbation frequency. The proposed method can be performed either continuously or periodically without interrupting the normal operation of the battery system and the power converter. Moreover, this chapter provides an example where the obtained impedance data is used for online SOC estimation of lithium-ion batteries.

The remainder of this chapter is organized as follows: the principle of operation of the basic online impedance measurement method is introduced and the implementation details are discussed in Section II. Section III presents the proof-of-concept experimental prototype results and discussion.

2.2 Online Battery Impedance Measurement

As mentioned earlier, in the battery-powered devices or systems, a DC-DC power converter is usually used to interface the battery with the load in order to provide voltage/current regulation. In many applications, this DC-DC power converter is usually bidirectional in order to allow for both charge and discharge operations of the battery system. A variety of DC-DC power converter topologies are available and the choice of the topology is mainly a function of target power level, power density, size and cost requirements, as well as integration and packaging simplicity for a given application.

A conventional non-isolated bidirectional DC-DC boost/buck converter, as shown in Fig. 2.3, is utilized in this work for illustration and validation. This bidirectional DC-DC power converter operates as a boost converter during discharge mode in order to step up the voltage to the voltage level required by the load and operates as a buck converter in battery charge mode in order to step down the voltage to the battery voltage.

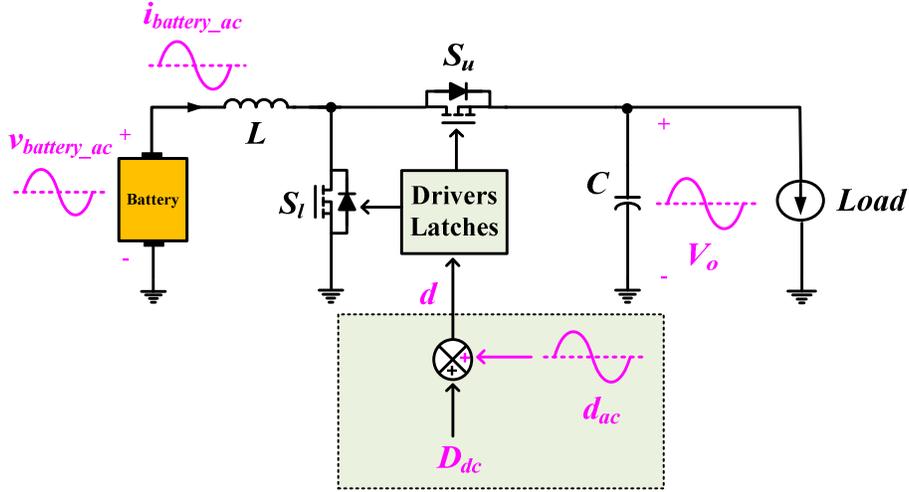


Figure. 2.3: Circuit diagram of a bidirectional DC-DC boost/buck power converter with the proposed impedance measurement method

Fig. 2.4 shows some key operating waveforms of the bidirectional DC-DC buck/boost converter with the proposed impedance measurement method. In order to supply a desired output voltage V_{o_dc} during the steady-state operation, the power converter needs to have a DC duty cycle value D_{dc} . The DC voltage of the battery and DC current of the battery are $V_{battery_dc}$ and $I_{battery_dc}$, respectively. As shown in Fig. 2.4, once the impedance measurement mode is triggered at T_1 , a small duty cycle sinusoidal perturbation signal d_{ac} with an amplitude of D_{ac} at the perturbation frequency f_p is added to D_{dc} as given by

$$d(t) = D_{dc} + D_{ac} \cdot \sin(2\pi f_p t) \quad (2.3)$$

This small duty cycle perturbation will result in generating relatively small sinusoidal ripples superimposed over the DC output voltage of the power converter V_{o_dc} , over the DC voltage of the battery $V_{battery_dc}$, and over the DC current of the battery $I_{battery_dc}$ as given by (2.4) and (2.5).

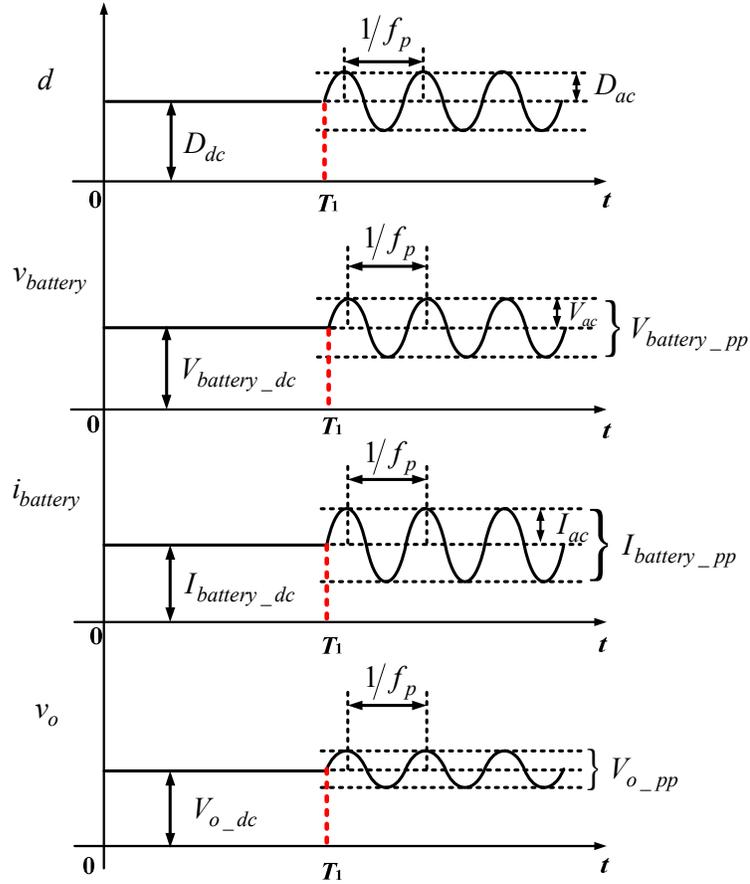


Figure.2.4: Operating waveforms of the battery system during the proposed impedance measurement process

$$i_{battery}(t) = I_{battery_dc} + I_{ac} \cdot \sin(2\pi f_p t + \phi_i) \quad (2.4)$$

$$v_{battery}(t) = V_{battery_dc} + V_{ac} \cdot \sin(2\pi f_p t + \phi_v) \quad (2.5)$$

In (2.4) and (2.5), $v_{battery}$ is the voltage of the battery and $i_{battery}$ is the current of the battery. All of these sinusoidal ripples are with the perturbation frequency of f_p . By measuring the peak-to-peak values (maximum-to-minimum values) of the battery voltage $V_{battery_pp}$ and the battery current $I_{battery_pp}$ during one perturbation cycle, the magnitude of the battery AC impedance at f_p can be determined based on (2.6). If there is a phase shift between the voltage and the current of the battery and/or phase information is needed, the phase of the battery impedance at f_p can be

determined by using (2.7), where $\varphi_v - \varphi_i$ is the phase shift between the voltage and the current of the battery.

$$|z_{battery}(f_p)| = \frac{V_{battery-pp}}{I_{battery-pp}} \quad (2.6)$$

$$\angle z_{battery}(f_p) = \varphi_v - \varphi_i \quad (2.7)$$

Fig. 2.5 shows a flowchart of the proposed online impedance measurement algorithm. This flowchart is divided into two parts. Part (a) describes the complete impedance measurement process. As illustrated in part (a), a small duty cycle sinusoidal perturbation is added to the duty cycle of the power converter which initiates the impedance measurement operation. Theoretically, only one perturbation cycle ($1/f_p$) is needed to measure the required peak-to-peak value of the battery voltage $V_{battery_pp}$ and battery current $I_{battery_pp}$. However, $V_{battery_pp}$ and $I_{battery_pp}$ are measured over M (more than one) consecutive perturbation cycles in practice in order to ensure that the system is not under transient condition during the impedance measurement process. The selection of the value of M is a tradeoff between the impedance measurement accuracy and the time that the impedance measurement process takes. In other words, the higher the value of M is, the higher accuracy the proposed online battery impedance measurement method would have, but the longer time the impedance measurement process would take. In the experimental prototype of this work, $M = 5$ is found to be a value that achieves a suitable tradeoff between accuracy and speed. Moreover, higher M value requires more memory storage space, which affects hardware size and cost. Part (b) of Fig. 2.5 shows the flowchart for online detection/identification of the system steady-state condition.

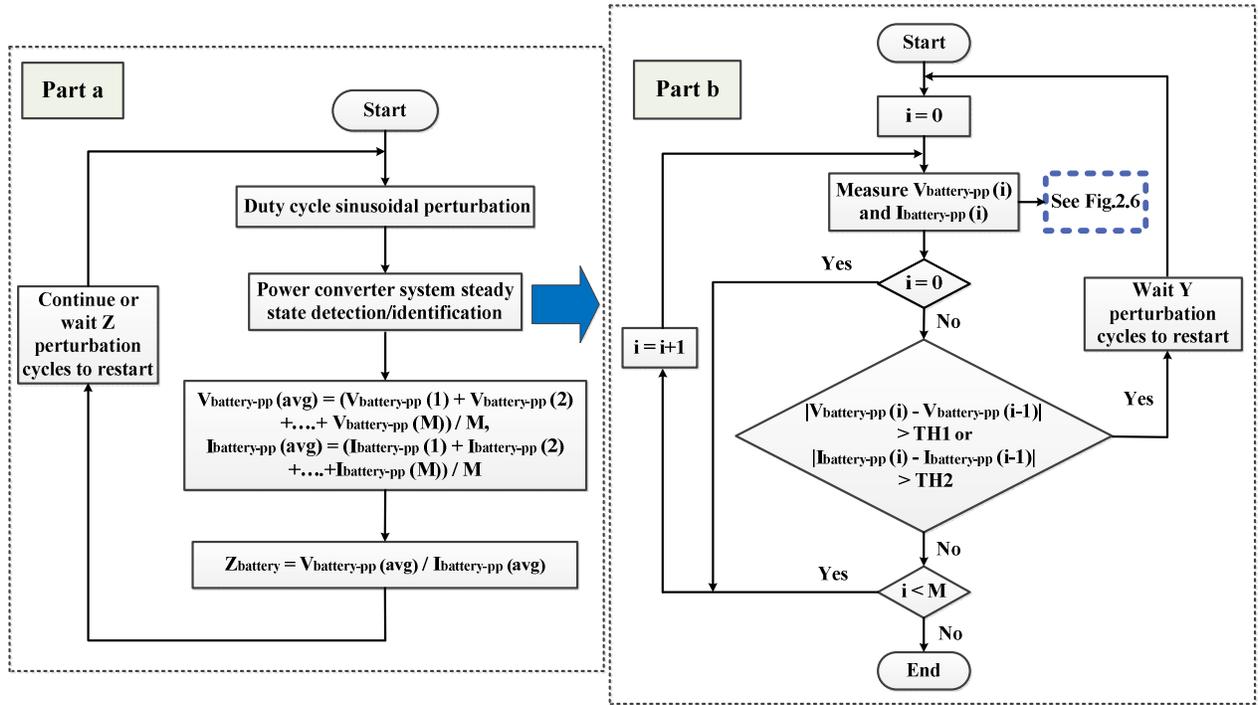


Figure. 2.5: The flowchart of the proposed online impedance measurement algorithm. Part (a) The complete online impedance measurement operation; Part (b) online detection/identification of the system steady-state condition

If $V_{\text{battery_pp}}$ and $I_{\text{battery_pp}}$ values do not vary over M perturbation cycles by more than the respective threshold value TH_1 and TH_2 , the system is considered under steady-state condition. Otherwise, the controller needs to wait for a duration of time which is equal to Y perturbation cycles before restarting a new cycle of system steady-state detection/identification. This operation continues until a confirmation that the system is under steady-state condition is obtained. The algorithm flowchart for the online detection of the peak and valley values of the battery voltage and battery current over M consecutive perturbation cycles is shown in Fig. 2.6, which is discussed in details later in this section.

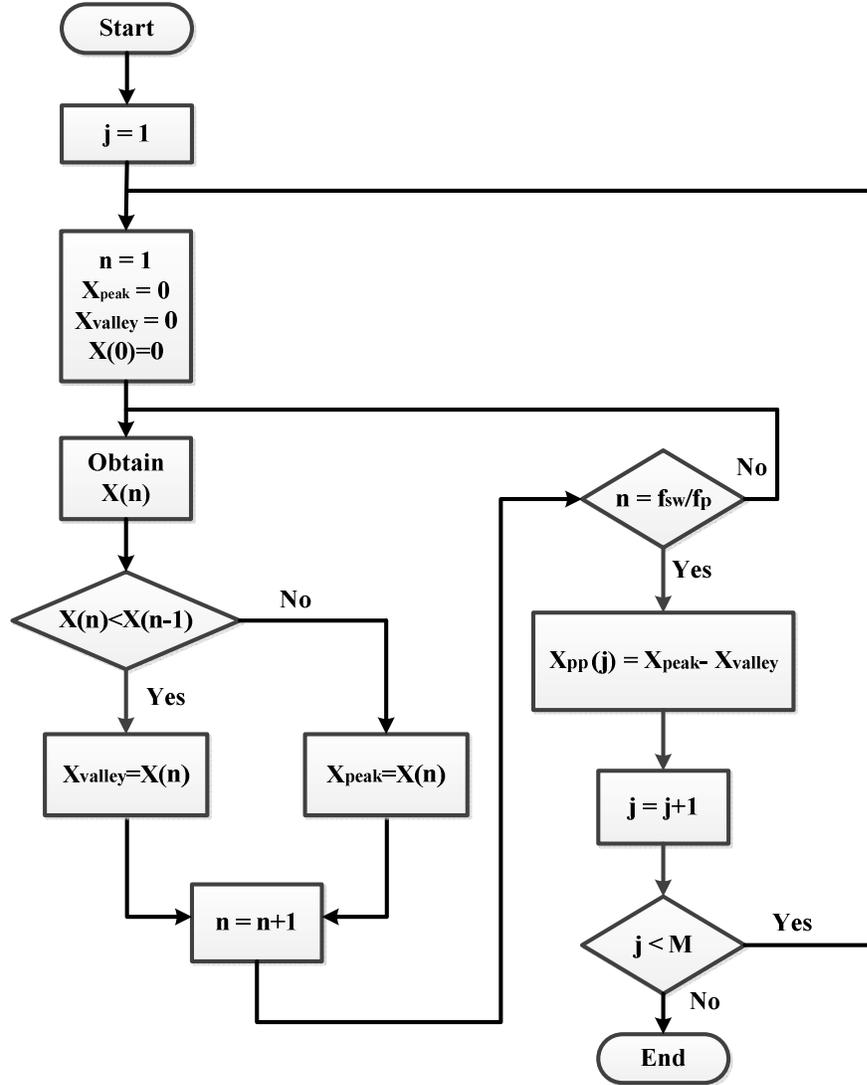


Figure. 2.6: The flowchart for online detection of the peak and valley values of the battery voltage or battery current over M perturbation cycle (used in the flowchart of Fig. 2.5)

In this chapter, the proposed online impedance measurement algorithm is implemented by using a digital controller. TH_1 and TH_2 are employed in order to account for the quantization error q caused by the ADC (Analog-to-Digital Converter) which is used for sampling of the battery voltage and current. The ADC quantization error q is the difference between the continuous analog waveform and the stair-stepped digital representation, and its value is

uniformly distributed between $-0.5 \times LSB$ and $+0.5 \times LSB$ (LSB stands for Least Significant Bit of the digital/binary number) as given by

$$-0.5 \cdot LSB \leq q \leq +0.5 \cdot LSB \quad (2.8)$$

The value of LSB is equal to the resolution of the ADC, $V_{range}/2^N$, where V_{range} is the full scale input analog voltage range of the ADC, and N is the number of bits (number of bits in the digital number or word) of the ADC. Therefore, the maximum quantization error q_{max} for battery voltage/current sampling can be expressed as

$$q_{max} = V_{range} / (2 \cdot 2^N) \quad (2.9)$$

Since the peak-to-peak value $V_{battery_pp}$ (or $I_{battery_pp}$) is obtained by subtracting the maximum value and the minimum value of $v_{battery}$ (or $i_{battery}$), there is a maximum quantization error in the worst case scenario in the calculation of $V_{battery_pp}$ (or $I_{battery_pp}$) which equals twice the quantization error given by (2.9). This maximum quantization error (q_{pp_max}) is given by

$$q_{pp_max} = V_{range} / 2^N \quad (2.10)$$

Based on this, TH_1 and TH_2 threshold values are defined as given by (2.11) and (2.12). TH_1 (for $V_{battery_pp}$) and TH_2 (for $I_{battery_pp}$) are used in the algorithm in order to account for the quantization error caused by the finite ADC resolution.

$$TH_1 = V_{range1} / 2^{N_1} \quad (2.11)$$

$$TH_2 = V_{range2} / 2^{N_2} \quad (2.12)$$

where V_{range1} is the full scale input analog voltage range of the ADC that is used to sample the battery voltage, N_1 is the number of bits of the ADC that is used to sample the battery voltage.

V_{range2} is the full scale input analog voltage range of the ADC that is used to sample the battery current, and N_2 is the number of bits of the ADC that is used to sample the battery current.

If the change in $V_{battery_pp}$ (or $I_{battery_pp}$) values over M consecutive perturbation cycles is less than TH_1 (or TH_2), then the system can be considered under steady-state condition. Otherwise, the system is considered under transient condition and another cycle of system steady-state detection/identification will need to be started after a duration of time that is equal to Y perturbation cycles.

As soon as the system steady-state condition status is confirmed, the $V_{battery_pp}$ and $I_{battery_pp}$ values over M consecutive perturbation cycles are averaged and used to determine the magnitude of the battery AC impedance based on (2.6). The proposed impedance measurement method can either be performed continuously or periodically by waiting Z perturbation cycles before restarting a new cycle of impedance measurement.

If there is a phase shift between the voltage and the current of the battery and it is desired to obtain the information of this phase shift as in (2.7), the time delay (t_d) between the peak of the battery voltage and the peak of the battery current is recorded in the digital controller. Then, the phase can be obtained by

$$\varphi_v - \varphi_i = 360^\circ \cdot t_d / (1/f_p) = 360^\circ \cdot t_d \cdot f_p \quad (2.13)$$

Fig. 2.6 shows the flowchart for online detection of the peak and valley values of the battery voltage or battery current over M perturbation cycles. X represents the battery voltage or battery current signal. A counter is used to count the number of switching cycles, and the initial value n of this counter is set to 1. Another counter is used to count the number of perturbation cycles, and the initial value j of this counter is also set to 1. One value of the signal X is obtained

per switching cycle, and therefore, the number of signal values obtained per perturbation cycle is equal to f_{sw}/f_p . As the value of n increases, if the value of X , i.e., $X(n)$, is less than its previous value $X(n-1)$, then this value is recorded as the current valley value in the X_{valley} register. Otherwise, this value is recorded as the current peak value in the X_{peak} register. When n reaches a value that is equal to f_{sw}/f_p indicating that a full perturbation cycle sampling and detection is completed, the values recorded in the X_{peak} and X_{valley} registers are the peak value and the valley value of the signal for this perturbation cycle, respectively. This operation continues for M perturbation cycles. Note that the ADC sampling rate of the signal can be set equal to the switching frequency (f_{sw}) and in this case only one ADC sample is used to obtain one value of the signal X per switching cycle. In order to minimize the error and achieve higher accuracy, the sampling rate of the ADC can be set higher than the switching frequency and multiple ADC samples per switching cycle (i.e., oversampling) are averaged in order to obtain one value of the signal X per switching cycle. This one value per switching cycle is what is needed in the flowchart of Fig. 2.6.

Measuring the DC impedance value by using the proposed method that utilizes the duty cycle perturbation of the power converter is relatively simple. Two values for the voltage of the battery (V_1 and V_2) and two values for the current of the battery (I_1 and I_2) are obtained for two duty cycle values (D_1 and D_2), respectively. Then the DC impedance can be calculated by

$$Z_{battery_dc} = \frac{V_1 - V_2}{I_2 - I_1} \quad (2.14)$$

2.3 Proof-of-Concept Experimental Results

A proof-of-concept experimental laboratory prototype is built in order to validate the proposed online impedance measurement method and its utilization in an example online SOC

estimation method. The experimental prototype consists of a 2.6 Ah 18650-size cylindrical lithium-ion battery cell [B8], a bidirectional buck/boost DC-DC power converter (as illustrated in Fig. 2.3), and a programmable electronic load. Main specifications for the battery used in this experiment are given in Table I. The switching frequency of the DC-DC power converter is 100 kHz. The proposed impedance measurement algorithm is implemented using TMS320F28335 microcontroller from Texas Instruments (TI) Corporation.

Table 2.1: Main Specifications of The Battery

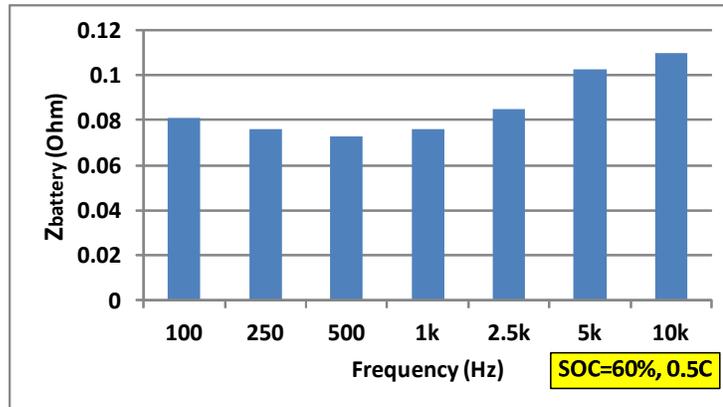
Chemistry	lithium-ion
Model number	30005-0
Nominal capacity	2600 mAh
Maximum voltage	4.2 V
Nominal voltage	3.7 V
Initial internal impedance	65 mohm at 1 kHz
Standard discharge/charge rate	0.5 C/0.5 C
Maximum discharge/charge rate	2 C/0.5 C

A. Battery Impedance Measurement Results

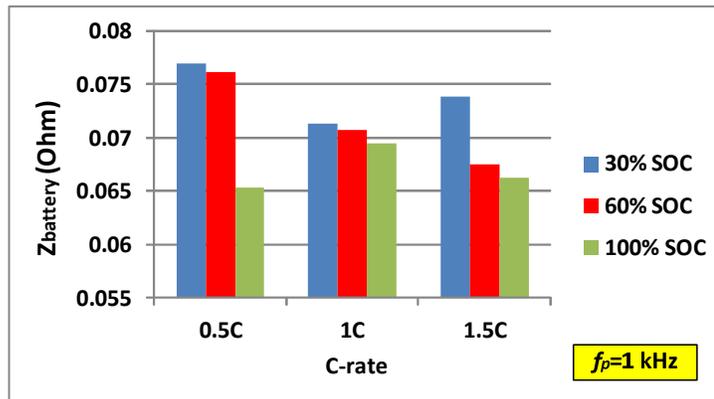
While the nominal value of the battery impedance is usually given in the specifications of the battery at AC 1 kHz [B8, B10-B13], the proposed impedance measurement method is used in this section in order to measure the impedance of the battery at several frequency values. These frequency values, including 100 Hz, 250 Hz, 500 Hz, 1 kHz, 2.5 kHz, 5 kHz, and 10 kHz, are selected as examples and not for limitation.

As discussed earlier in this chapter, the duty cycle value of the power converter is perturbed sinusoidally at a given frequency around its steady state DC value. In this section, the DC duty cycle value is set to 0.5 while the amplitude of the duty cycle sinusoidal perturbation signal is set to 0.02 ($0.02/0.5 \times 100\% = 4\%$ perturbation). Therefore, the duty cycle value varies from 0.48 to 0.52 in a sinusoidal manner as given by $d(t) = 0.5 + 0.02 \cdot \sin(2\pi ft)$. Fig. 2.7 (a) shows the measured impedance of the battery by using the proposed method at various frequencies at

the SOC of 60% while the battery is discharged at 0.5 C. It is shown in Fig. 2.7 (a) that the value of the impedance decreases as the frequency increases from 100 Hz to 500 Hz, and then gradually ramps up as the frequency increases from 500 Hz to 10 kHz. This trend of impedance variation matches the one presented in [B15].



(a)



(b)

Figure. 2.7: (a) The impedance of the battery at various perturbation frequencies, at the SOC of 60% and C-rate of 0.5C; (b) The impedance of the battery at various C-rates, various SOC's and at the perturbation frequency of 1 kHz

In order to examine the effects of the SOC value on the impedance of the battery, the impedance measurement is performed at different SOC values for different C-rates. Fig. 2.7(b) shows the impedance measurement data obtained at various SOC values (100%, 60%, and 30%)

and various C-rates (0.5 C, 1 C, and 1.5 C) when the duty cycle of the power converter is perturbed at 1 kHz. It can be observed from Fig. 2.7(b) that the impedance of the lithium-ion battery increases with the depth of discharge (DOD) for different C-rates. For example, when the battery is discharged at 0.5 C, the impedance of the battery increases from 65.28 m Ω to 76.92 m Ω as the SOC decreases from 100% to 30%. The experimental results/data at 1C and 1.5C discharge rates show similar trends. Note that the measured impedance of the battery at 1 kHz closely matches the one provided in the specification of the battery [B8].

Fig. 2.8 shows sample experimental waveforms during the process of the impedance measurements using the proposed method under selected frequency values and combinations of SOC and C-rate. Each waveform includes, from top to bottom, the voltage of the battery, the current of the battery, and the output voltage of the power converter. From the experimental waveforms shown in Fig. 2.8, it can clearly be observed that the sinusoidal ripple values of the output voltage of the power converter caused by the duty cycle perturbation are less than 5% of the corresponding DC values in most cases, and less than 10% of the corresponding DC values in all cases. This indicates that the proposed method does not interrupt the normal operation of the power converter. In addition, the complete impedance measurement process takes only a few sinusoidal perturbation cycles (five in this paper). These two features make the proposed impedance measurement method ideal for online applications. It should also be noted that the sinusoidal ripple values could be reduced by using smaller duty cycle perturbation values.

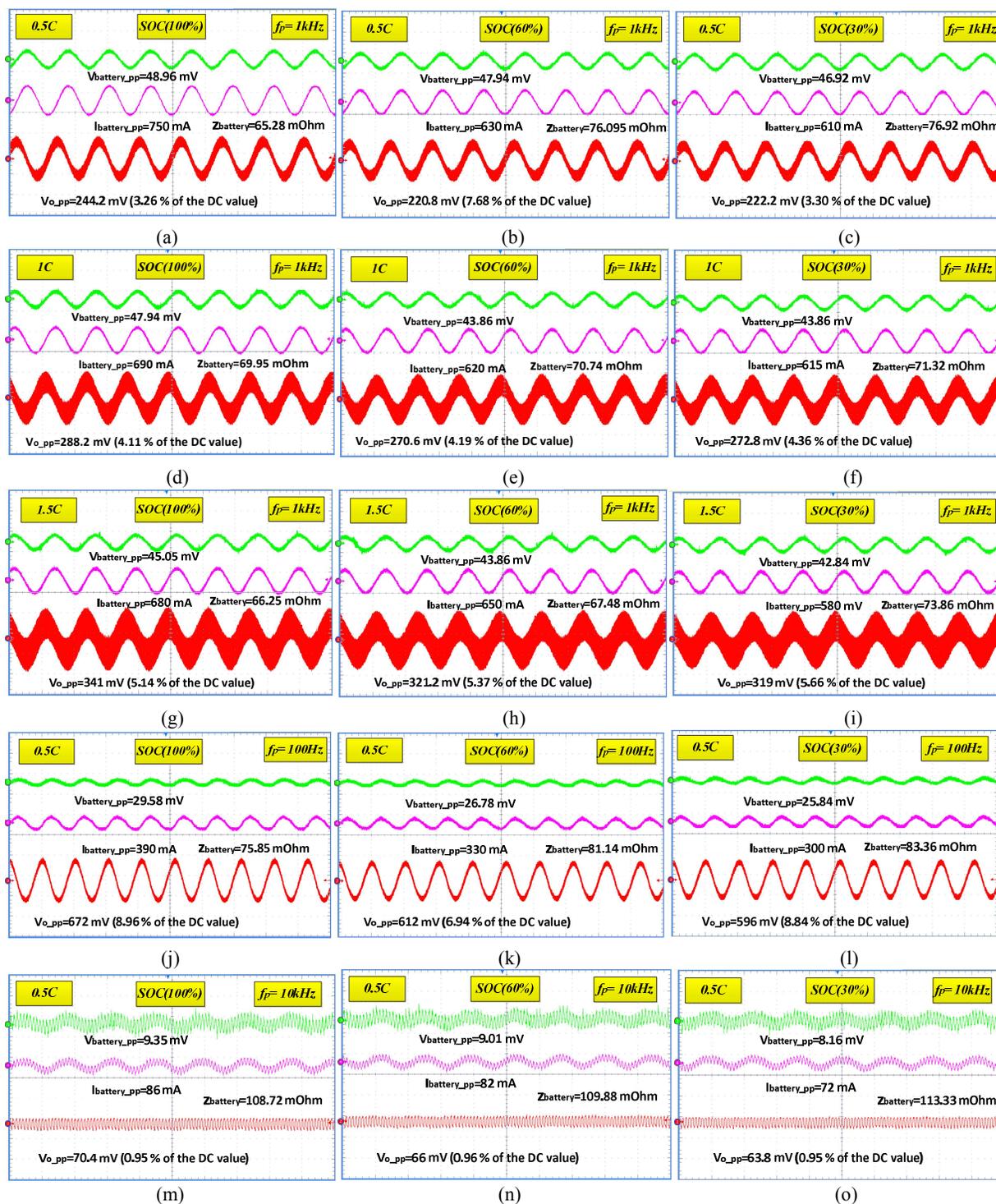


Figure 2.8: Sample experimental waveforms when the battery impedance measurements are performed under various C-rates, various SOC, and various perturbation frequencies (as marked on each part of the figure). Top (Green) trace: battery voltage (1 ms/div (a-o), 60 mV/div (a-i), 80 mV/div (j-l), 10 mV/div (m-o)), middle (pink) trace: battery current (1 ms/div (a-o), 500 mA/div (a-l), 100 mA/div (m-o)), bottom (red) trace: load/output voltage of power converter (1 ms/div (a-o), 110 mV/div (a-i), 300 mV/div (j-l), 110 mV/div (m-o)), all oscilloscope channels/traces are AC coupled

B. Online Impedance-Based SOC Estimation Results

The open-circuit voltage (OCV) of the battery is usually utilized as an indication of the SOC of the lithium-ion batteries [B7, B14]. To obtain an accurate open-circuit voltage (OCV), the battery needs to stay in rest/relaxation mode (i.e. under no load condition) for a long period of time (e.g. two hours) in order to reach electrochemical equilibrium prior to the OCV measurement. However, such a long period of rest time is not practical for online applications.

The measured impedance using the proposed method is utilized in this section in order to provide a practical online SOC estimation method for lithium-ion batteries. This is an example of how the proposed online impedance measurement method could be utilized for SOC estimation purposes. It could also be utilized for SOH evaluation by using one of the methods available in the literature [15-16, 29-30, 44, 46-47].

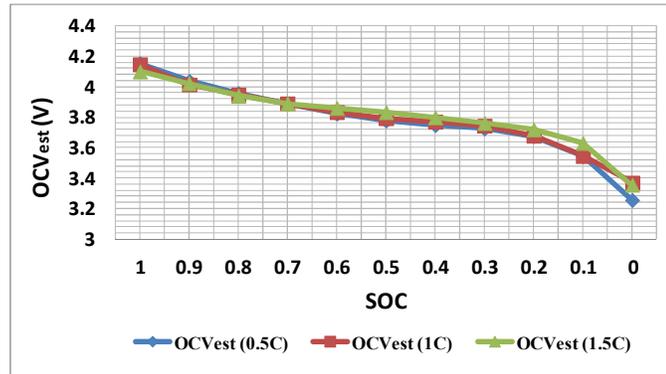


Figure. 2.9: Sample experimental curves for online estimated open circuit voltage versus SOC at various C-rates (the three lines overlap on most of the graph)

A new parameter, OCV_{est} , is defined as the online estimated open-circuit voltage of the battery which can be calculated by

$$OCV_{est} = V_{battery_dc} + I_{battery_dc} \cdot |z_{battery}| \quad (2.15)$$

where $|Z_{battery}|$ is the magnitude of the battery impedance in Ω , $V_{battery_dc}$ is the DC voltage of the battery in volts with the direction shown in Fig. 2.3, and $I_{battery_dc}$ is the DC current of the battery in amperes with the direction shown in Fig. 2.3. $I_{battery_dc}$ is positive when the battery is discharging and is negative when the battery is charging.

Based on the information of the battery impedance at 1 kHz (as an example) which were presented earlier in this section, and in combination with the measured DC voltage and DC current of the battery, the OCV_{est} versus SOC curves at various C-rates are plotted as shown in Fig. 2.9. It can be observed from Fig. 2.9 that these curves almost overlap. Therefore, this curve can be utilized to perform a simple online SOC estimation. Once the impedance of the battery is obtained, OCV_{est} can be calculated based on (2.15) and then the corresponding SOC value can be estimated by mapping the calculated OCV_{est} value to the OCV_{est} versus SOC curve shown in Fig. 2.9.

C. Comments on Temperature Effect on The SOC Estimation for Lithium-Ion Batteries

Temperature is a key factor that affects the accuracy of the SOC estimation [15-17, 27, 48-49, 52, 57-58], which has not been sufficiently addressed in the literature. For example, in the conventional coulomb counting method, the value of the battery capacity is usually assumed to be the rated capacity at a nominal temperature without compensation as a function of the temperature [16]. Other example SOC estimation methods include model-based methods [48-49]. While in these model-based methods the Resistance-Capacitance (RC) parameters of the battery model account for the temperature effects, other variables like OCV that are also temperature dependent are not accounted for. In the proposed online impedance-based SOC estimation method for lithium-ion batteries, in addition to taking the temperature effects into account in the measured battery impedance itself, different OCV_{est} versus SOC curves at

different operating temperatures can be measured if needed in order to further compensate for the temperature variations. Based on the real-time measured temperature value of the battery, the corresponding OCV_{est} versus SOC curve can be used for SOC estimation.

2.4 Summary

This chapter first presents a basic online impedance measurement method for electrochemical batteries. Instead of performing external AC voltage/current signal injection, the impedance measurement is achieved through the control of the DC-DC power converter interfacing the battery with the load/system. As a result, the signal generation circuits/devices required by the conventional impedance measurement methods are eliminated, leading to reduced cost, design complexities and size of the overall system.

The proposed online impedance measurement method can be performed either continuously or periodically without interrupting the normal operation of the battery system and power converter. Also, the complete impedance measurement process takes only a few perturbation cycles, which makes the proposed method well suited for real-time battery impedance monitoring.

In addition, a practical online SOC estimation method for lithium-ion batteries is provided in this chapter based on the obtained information of the battery impedance. With the proposed method, there is no need to put the battery in rest/relaxation mode for a long period of time in order for the battery to reach electrochemical equilibrium prior to the OCV measurement. Experimental results have validated the effectiveness of the proposed online impedance measurement method and its utilization in the online SOC estimation.

CHAPTER 3

ENERGY SHARING CONTROLLER IN BATTERY DISCHARGE MODE

3.1 Introduction

This chapter presents an energy sharing based cell balancing control scheme for a distributed battery energy storage system architecture where the cell balancing system and the DC bus voltage regulation system are combined into a single system. The battery cells are decoupled from one another by connecting each cell with a small lower power DC-DC power converter. The small power converters are utilized to achieve both SOC balancing between the battery cells and DC bus voltage regulation at the same time. The battery cells' SOC imbalance issue is addressed from the root by using the energy sharing concept to automatically adjust the discharge/charge rate of each cell while maintaining a regulated DC bus voltage. Consequently, there is no need to transfer the excess charge/energy between the cells for SOC balancing which leads to reduced power losses.

In this chapter, the conventional centralized battery energy storage architecture is first reviewed in Section II where the cell balancing issue and commonly used solutions are reviewed. Section III presents the basic concept behind the distributed battery energy storage system architecture which the proposed energy sharing controller will be used for. The operational principle of the proposed energy sharing controller is discussed for discharging operation in Section IV. Theoretical steady-state analysis of the proposed energy sharing SOC balancing system during discharging operation is presented in Section V. Proof-of-concept experimental

prototype results are presented and discussed in Section VI. The last section summarizes this chapter.

Due to the differences in operation between the battery discharge mode and charge mode, the energy sharing controller presented in this chapter could not be applied to the charging operation directly without modifications. Next chapter will propose an upgraded battery charging controller with energy sharing that works for charging operation.

3.2 Centralized Battery Energy Storage System Architecture

A number of battery cells are usually connected in series in order to supply higher voltage and higher power to the load in a wide range of applications, including EVs/HEVs, aerospace battery systems, smart grids, and laptops [59-72]. While significant efforts are made by designers to select the battery cells such that they are as identical/matched as possible, the battery cells would still have mismatches between each other in practice due to manufacturing tolerances, different self-discharge rates, uneven operating temperature across the battery cells, and non-uniform aging process, among others. As a result, the SOC values of the battery cells connected in series are likely to diverge from one another during discharging/charging operation, which can result in degraded battery energy utilization and overdischarge/overcharge for some of the battery cells. This in turn may cause many serious problems such as battery deterioration, overheating, and even catching fire in a worst case scenario [60, 68-69].

To address the cells SOC imbalance issue, cell balancing circuits and associated controller are implemented as an integral part of the BMS in order to minimize non-uniform discharging/charging between the cells.

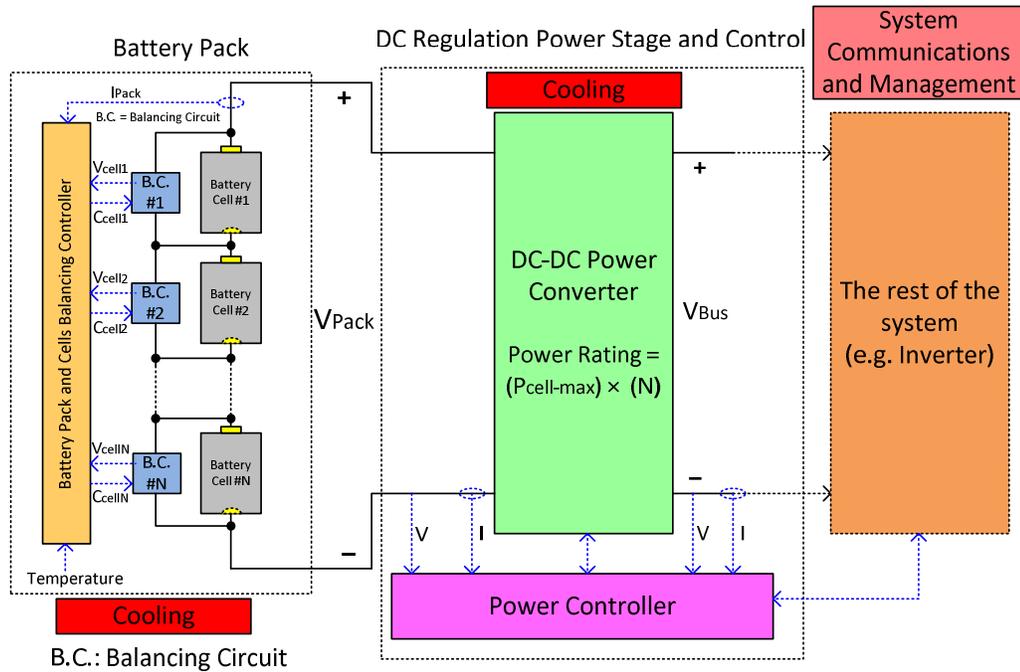


Figure 3.1: The simplified block diagram of a conventional battery energy storage system architecture for electric vehicles application example

Fig. 3.1 illustrates a simplified block diagram of a conventional battery energy storage system architecture for EVs [60-61, 65, 70], used as an example application in this chapter. This architecture is named as "centralized architecture" to distinguish it from the distributed architecture which the proposed energy sharing controller will be used for. In the centralized architecture, a high power (referred to as "large" in this paper) DC-DC power converter (power rated at Y) is utilized to regulate the DC bus voltage to the rest of the system (e.g., power inverter driving the electric motor that propels the EV). To achieve SOC balancing between the battery cells connected in the same string, each cell is equipped with a dedicated cell balancing circuit ("B.C." used for abbreviation in Fig. 3.1). Meanwhile, a cell balancing controller is employed in order to control and manage the operation of the cell balancing circuits.

A wide variety of cell balancing methods have been presented in the literature [59, 61-67, 73-79]. In general, the cell balancing methods fall under two main categories: passive and active cell balancing schemes. Table 3.1 shows the classification of some example cell balancing methods presented in the literature. A typical passive cell balancing method is to connect a shunt resistor and a switch in parallel with each battery cell [59]. The excess energy is dissipated through the shunt resistors in the form of heat. This scheme has the advantages of low cost, simple circuit configuration, and ease of implementation. However, this comes at the expense of additional energy dissipation and heat.

Table 3.1: Classification of Some Example Cell Balancing Methods

BALANCING CATEGORY	TECHNIQUE	PROS	CONS	LITERATURE
Passive	Shunt resistor	<ul style="list-style-type: none"> ▪ Simple ▪ Low cost 	<ul style="list-style-type: none"> ▪ 0% efficiency 	[59]
Active	Cell to cell (charge transfer between adjacent cells)	<ul style="list-style-type: none"> ▪ Relatively simple ▪ Modest control complexity 	<ul style="list-style-type: none"> ▪ Low efficiency ▪ Low balancing speed 	[61][62]
Active	Cell to cell (charge transfer between arbitrary cells through multi-winding transformer)	<ul style="list-style-type: none"> ▪ High efficiency ▪ High balancing speed 	<ul style="list-style-type: none"> ▪ Not practical if cell count is high ▪ Hard to fabricate symmetrical windings 	[63]
Active	Cell to module (charge transfer between galvanic isolated converter)	<ul style="list-style-type: none"> ▪ Relatively simple ▪ Modest efficiency ▪ High balancing speed 	<ul style="list-style-type: none"> ▪ High power isolated converter ▪ Complicated control 	[76][77]
Active	Cell bypassing (cell disconnected from the current path)	<ul style="list-style-type: none"> ▪ Relatively simple ▪ Modest balancing speed 	<ul style="list-style-type: none"> ▪ High current switch ▪ Low efficiency 	[78][79]

Active cell balancing methods are more promising to be utilized in the next-generation EVs/PHEVs and smart grid battery energy storage systems due to its ability to achieve high efficiency. Instead of dissipating the excess energy, active cell balancing methods achieve cell balancing by transferring the excess energy between the battery cells. Depending on how the

energy is redistributed between the cells, active cell balancing methods can be classified into the following categories: cell to cell, cell to module, bypassing. In general, the efficiency of the active balancing circuits with appropriate design is above 90% compared to 0% efficiency of passive balancing.

Switched-capacitor based circuits are commonly used to transfer energy between cells, thanks to its simplicity [61]. To achieve higher efficiency of energy transfer, resonant switched-capacitor balancing circuit can be utilized such as the one presented in [62], where a small inductor is added to form a resonant tank with the capacitor. Zero-current switching (ZCS) operation can be achieved at the turn-off switching transition of the MOSFETs, leading to reduced power losses. However, with this type of balancing circuit, energy are only transferred between adjacent battery cells. If the energy is to be transferred from the battery cell on one end of the battery string to the cell on the other end, a significant portion of the energy can be lost along the energy transfer path.

To overcome this issue, multi-winding transformer based balancing circuits can be utilized, as in [63]. The balancing circuit topology presented in [63] allows the energy to be transferred between arbitrary cells in the battery string. However, the multi-winding transformer based balancing circuits typically suffer from two major issues. The first issue is that the balancing performance of the circuit depends heavily on the symmetry of the transformer windings. Another issue is that it is difficult to fabricate a transformer with several tens or hundreds of symmetrical windings for high power applications where a large number of battery cells are connected in series. A common solution to this issue would be to modularize the battery cells and then use an additional balancing circuit stage to balance the modules. However, this would lead to increased system design complexity, cost and size.

Another commonly used cell balancing method is bypassing the cell whose SOC is the lowest during discharging or the highest during charging [78-79]. The downside of this type of methods is that the power switch must have high current rating in order to handle the high current of the battery string during bypassing. This would also result in more power loss.

In this work, instead of utilizing a centralized battery system architecture, a distributed architecture is used where the cell balancing system and DC bus voltage regulation system are combined into a single system. The re-designed DC-DC power stage with the proposed energy sharing controller realizes cell balancing while maintaining the DC bus voltage regulation. Consequently, there is no need to transfer the charge/energy between the cells in order to redistributing the energy. This helps eliminate the power loss along the charge/energy transfer path in addition to simplifying the system design. The details for the proposed concept will be discussed in the following sections.

3.3 Basics Behind the Distributed Battery System Architecture

Fig. 3.2 block diagram illustrates the concept basis of the distributed battery energy storage system architecture. Rather than connecting the battery cells in series to form a battery string and regulating the voltage of the battery string through a high power DC-DC power converter rated at Y as illustrated in Fig. 3.1, cells are decoupled from one another by connecting each cell with a lower power DC-DC power converter rated at Y/N , where N is the number of the battery cells in the string.

As illustrated in Fig. 3.2, the output of each small DC-DC power converter is connected in series in order to generate a higher DC bus voltage for the rest of the system or load. This forms a string of several battery power modules (BPMs), where each module consists of a battery cell and an open-loop DC-DC power converter within itself, i.e., the converter has no

independent closed-loop control from the other converters, but its current and voltage information are sensed and fed to an external controller. It is also an option to have more than one cell in series or in parallel per BPM, in order to reduce cost and complexity, but at the expense of performance degradation.

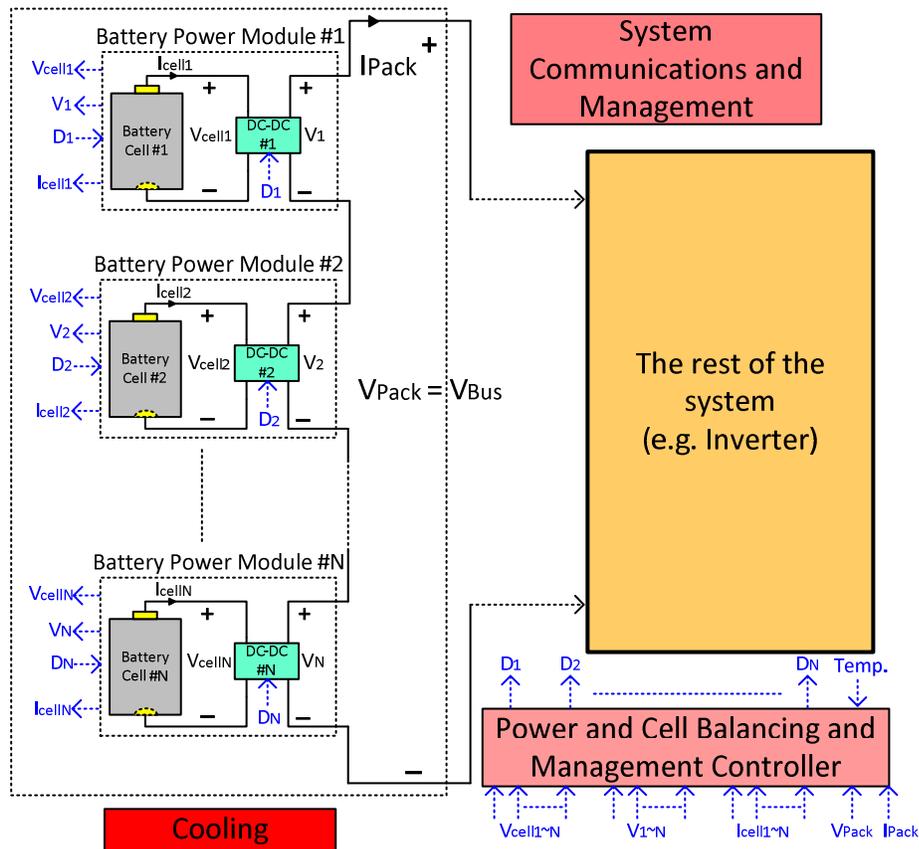


Figure.3.2: The simplified block diagram of the distributed battery energy storage system architecture with the proposed energy sharing control for EV application example

The N BPMs' external energy sharing controller outputs the control signals (duty cycles D_1 through D_N) to the DC-DC power converters in the N BPMs in order to regulate the BPMs' output voltages V_1 through V_N , to regulate discharge/charge rate of each battery cell for SOC balancing, and to maintain DC bus voltage at the desired value. The small DC-DC power converters are utilized here to achieve SOC balancing between the battery cells while

maintaining DC bus voltage regulation. Therefore, there is no need to use two independent converter systems for cell balancing and DC bus voltage regulation as seen in the centralized architecture. This leads to reduced system design complexity. Moreover, from the system point of view, if the small low-power DC-DC converters are well designed with comparable or higher efficiency than the big high-power DC-DC converter that is utilized in the conventional architecture, the cell balancing is achieved with effectively 100% efficiency in the proposed architecture (i.e., there are no additional power losses caused by cells SOC balancing operation).

The small DC-DC power converter used in each BPM needs to be bidirectional in order to allow for both charging and discharging operations. The DC-DC power converter needs to be of the isolated type when isolation is required. A variety of candidate isolated and non-isolated topologies are available for this application [71-72, 80-83, 92-94]. For simplification, the conventional non-isolated bidirectional DC-DC buck/boost converter is used in this work for illustration and verification. This bidirectional power converter operates as a DC-DC boost converter with the battery cell as the input and the DC bus as the output during discharging operation, and operates as a DC-DC buck converter with the DC bus as the input and the battery cell as the output during charging operation. The selection of the power converter circuit topology is a function of many variables such as the target BPM power rating, power conversion efficiency, power density, cost, integration/packaging simplicity, and EMI requirement.

It should be noted that the output-series connected multiple converters architecture itself is not new and has been utilized in many applications, such as those on photovoltaic applications [84-86]. Another concept is presented in [87] which utilizes distributed battery architecture. However, the basic concept in [87] is based on calculating the duty cycle values and discharge intervals required to achieve cell balancing and output voltage regulation by using theoretical

steady-state equations instead of a closed-loop controller. These equations are obtained under the assumption that the converters are ideal, where the parasitics components and other non-ideal factors are neglected, such as the on-state resistance of the MOSFETs, DCR (DC Resistance) of the inductor, ESR (Equivalent Series Resistance) of the capacitor and PCB (Printed Circuit Board) traces' resistance, among others. One possible way to achieve the desired cell current and output voltage in [87] is by manually tuning the duty cycle values. But this is not practical for on-line operation. The energy sharing controller concept and architecture proposed in this chapter address these challenges, as will be discussed next.

3.4 Principle of Operation of The Energy Sharing Controller in Discharge Mode

This section focuses on the discussion of the operational principle of the proposed energy sharing controller during discharging operation. This energy sharing controller is comprised of two closed-control loops in discharge mode, i.e., BPM output voltage regulation control loop (voltage control loop for short) and SOC balancing control loop.

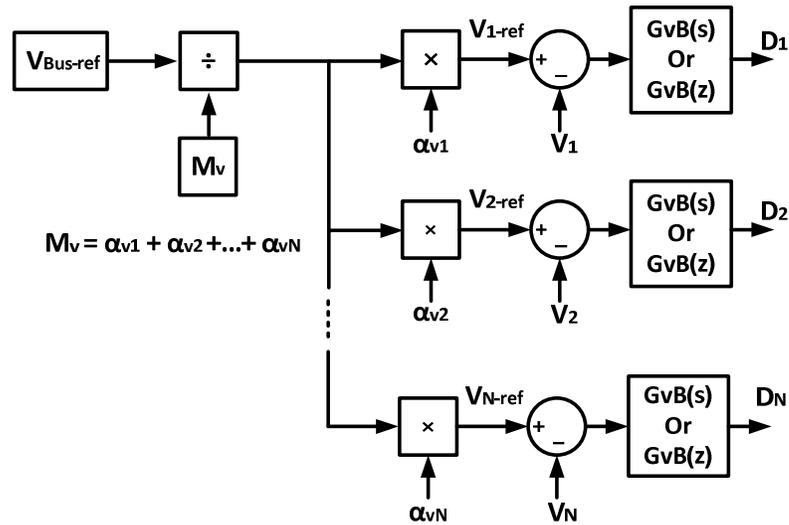


Figure. 3.3: Part I of the energy sharing controller's basic block diagram during discharging operation, i.e., the BPM output voltage regulation control loop

Fig. 3.3 illustrates the control block diagram of the voltage control loop. The DC bus voltage reference (which is also the battery pack voltage reference in this case) $V_{\text{Bus-ref}}$ is specified and used to derive the output voltage reference for the power converter in each BPM (i.e., $V_{1\text{-ref}}$ through $V_{N\text{-ref}}$) by using equations (3.1) and (3.2).

$$V_{r\text{-ref}} = V_{\text{Bus-ref}} \cdot (\alpha_{vr} / M_v) \quad (3.1)$$

$$M_v = \alpha_{v1} + \alpha_{v2} + \dots + \alpha_{vN} \quad (3.2)$$

where α_{v1} through α_{vN} are the voltage loop multipliers, and $r = 1, 2, \dots, N$. These output voltage reference values for the BPMs are then utilized in the voltage control loop to regulate the output voltage for each BPM (V_1 through V_N). The initial voltage loop multiplier values $\alpha_{v1} = \alpha_{v2} = \dots = \alpha_{vN} = 1$, and therefore, the output voltages of the BPMs are initially equal and their sum is equal to $V_{\text{Bus-ref}}$, i.e., V_{bus} (or $V_{\text{pack}} = V_{\text{Bus-ref}}$). The output voltage of each BPM can be made different by making its corresponding voltage loop multiplier value (α_{v1} through α_{vN}) different, while keeping $M_v = \alpha_{v1} + \alpha_{v2} + \dots + \alpha_{vN}$ such that V_{bus} is always equal to $V_{\text{Bus-ref}}$ and thus DC bus regulation is maintained. The lower limit of the voltage loop multipliers are set to zero. The values of voltage loop multipliers have to be larger or equal to zero because according to equation (3.1) and (3.2), if some of the voltage loop multiplier values are positive while the others are negative, this will cause some V_{ref} values to be positive while the others to be negative, which should be prohibited.

The continuous-time transfer function $G_{vB}(s)$ or discrete-time transfer function $G_{vB}(z)$ of the compensator used in the voltage control loop can be a PI or PID type (Proportional-Integral-Derivative). $G_{vB}(z)$ is a discrete-time transfer function (in z-domain) which is utilized for digital controller implementation in the experimental work.

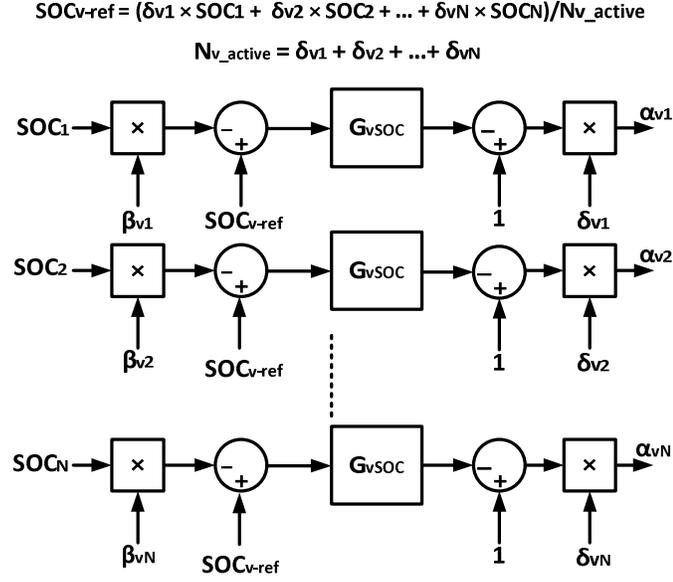


Figure.3.4: Part 2 of the energy sharing controller's basic block diagram during discharging operation, i.e., SOC balancing control loop

Fig. 3.4 illustrates the control block diagram of the second part of the proposed energy sharing controller in discharge mode, i.e., the SOC balancing control loop. The voltage loop multiplier values (α_{v1} through α_{vN}) are adjusted in order to control the discharge rate of each battery cell, and therefore, control the SOC values (SOC_1 through SOC_N) of the battery cells. The SOC values of the battery cells are compared to a reference SOC value (SOC_{v-ref}) in order to maintain balanced SOC values assuming that the SOH of all the battery cells are the same. This SOC reference value is generated by summing up the SOC values of all the battery cells (assume for now that the SOC balancing loop multiplier values $\beta_{v1} = \beta_{v2} = \dots = \beta_{vN} = 1$ and the Enable/Disable multiplier values $\delta_1 = \delta_2 = \dots = \delta_N = 1$, as will be discussed next) and then dividing the sum by the number of active cells, N_{v_active} , as given by (3.3) and (3.4)

$$SOC_{v-ref} = (\delta_{v1} \cdot SOC_1 + \delta_{v2} \cdot SOC_2 + \dots + \delta_{vN} \cdot SOC_N) / N_{v_active} \quad (3.3)$$

$$N_{v_active} = \delta_{v1} + \delta_{v2} + \dots + \delta_{vN} \quad (3.4)$$

If the SOC value of a battery cell is smaller or larger than the SOC reference value (i.e., the other battery cells' SOC values), this will affect its corresponding voltage loop multiplier value which in turn affects the output voltage reference value for that specific BPM. Since the output current of all BPMs in the string is the same, this different output voltage will affect the discharge rate of that specific cell because the output power of a BPM in this case is a function of the output voltage of the BPM. This operation will continue until the SOC values of all the battery cells are balanced. Adjusting the output voltage of a BPM while maintaining the total DC bus voltage regulated means that the energy drawn from that battery cell is controlled, which controls the discharge rate of that battery cell. This energy sharing control concept automatically and quickly results in SOC balancing between the battery cells in the battery pack. In Fig. 3.4, the compensator's transfer function G_{vSOC} utilized in the SOC balancing control loop can also be a PI or a PID type.

The plant that is controlled here is the control-to-output transfer function of the BPM boost converter. The inner loop (voltage control loop) should be designed to be faster than the outer SOC balancing control loop. The compensators, G_{vB} and G_{vSOC} , could be designed based on the rule-of-thumb frequency-domain controller design guidelines and criteria which includes crossover frequency (unit-gain bandwidth), stability margins. The detailed small-signal modeling and energy sharing controller design are presented in Chapter 5.

The SOC balancing loop multipliers (β_{v1} through β_{vN}) can be used to control (alter) the desired SOC value for a specific battery cell in order to make the SOC or discharge rate of a battery cell larger or smaller than it is for the rest of the battery cells. Each SOC balancing loop multiplier can have positive values from 0 to 1. It can be a function of the SOH of the battery cell (assuming that SOH information is available for each cell [68-69]). If this multiplier value is

larger, the SOC balancing control loop will think that this battery cell has a larger SOC value than it actually has and therefore it will discharge the battery cell at a faster rate, and vice versa. The β_{v1} through β_{vN} multipliers are added to the proposed controller for future utilization. These multipliers are not utilized in this paper and their values are set to $\beta_{v1} = \beta_{v2} = \dots = \beta_{vN} = 1$.

The Enable/Disable multipliers (δ_1 through δ_N) have values of either 1 or 0 in order to enable or disable a BPM control (if a BPM is to be removed from the system). Each BPM has two output terminals which can be connected after removing/disconnecting a BPM in order to maintain a working system. A BPM can manually be removed and the corresponding two terminals in the corresponding socket can manually be shorted/connected. A possible future work is to investigate methods to automatically realize bypassing of a BPM during online operation. This might require adding extra components. The Enable/Disable multiplier δ_r for a given BPM is set to zero only when the corresponding BPM is removed. When a BPM is removed from the system, the corresponding voltage loop multiplier (α_{vr}) for that BPM is equal to 0 because $\delta_r = 0$, as illustrated in Fig. 3.4, and the corresponding two output voltage terminals for that BPM are shorted in order to provide current flowing path. Once an Enable/Disable multiplier is set to zero, this will affect equations (3.2)-(3.4) and the SOC balancing and DC bus voltage regulation operations will continue as they should assuming that the maximum allowed output voltage of each BPM is not exceeded.

3.5 Steady-State Analysis of The Energy Sharing Controller in Discharge Mode

This section presents theoretical steady-state analysis of the energy sharing controlled distributed battery system during discharging operation. Fig. 3.5 shows the system configuration. To simplify analysis, assume that all the power converter components are ideal, which means the

parasitic values of the components are negligible, except for the internal impedance of the battery cell (Z_{cell}).

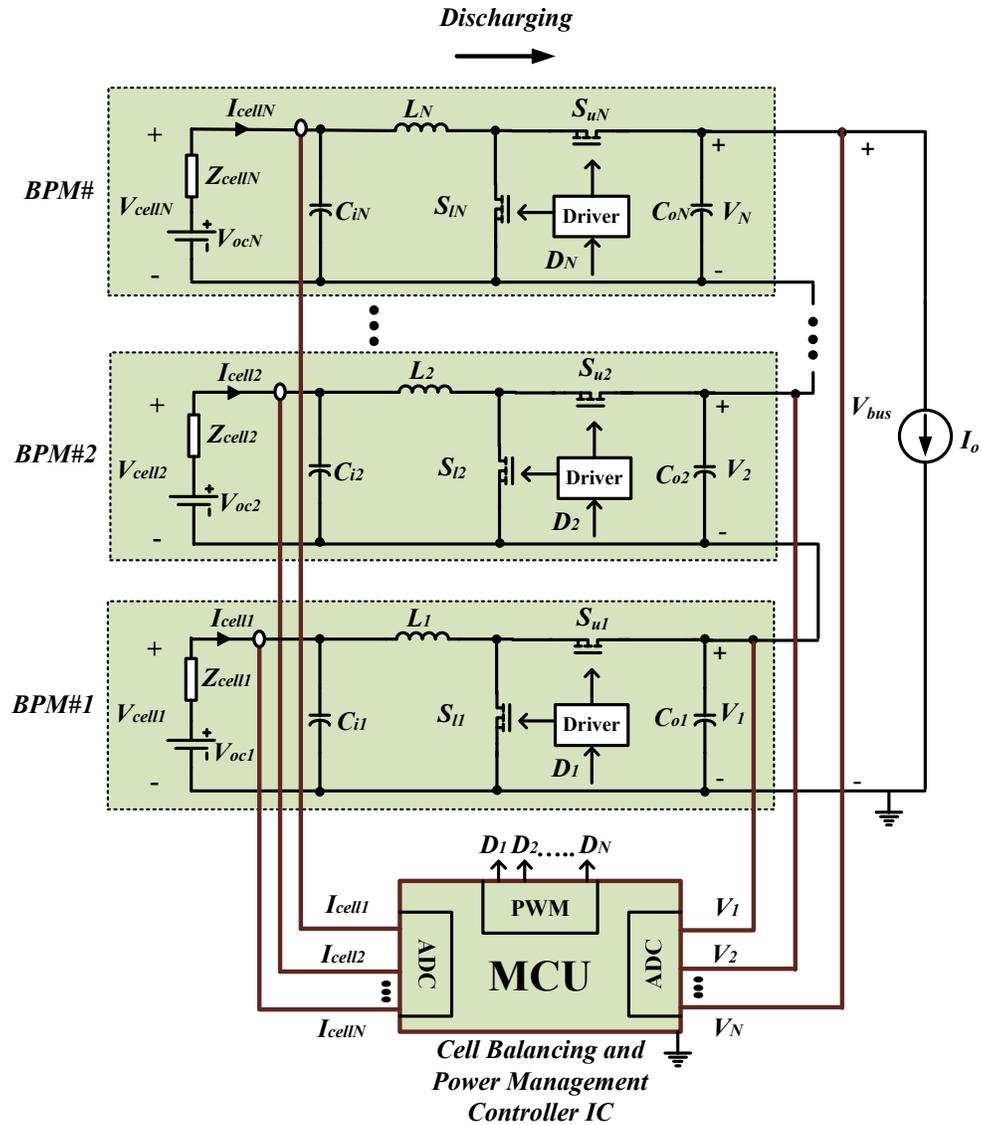


Figure. 3.5: System configuration of the distributed battery energy storage system architecture with the proposed energy sharing controller in discharge mode

For the boost converter topology in Continuous Conduction Mode (CCM) operation, the currents of the battery cells are given by

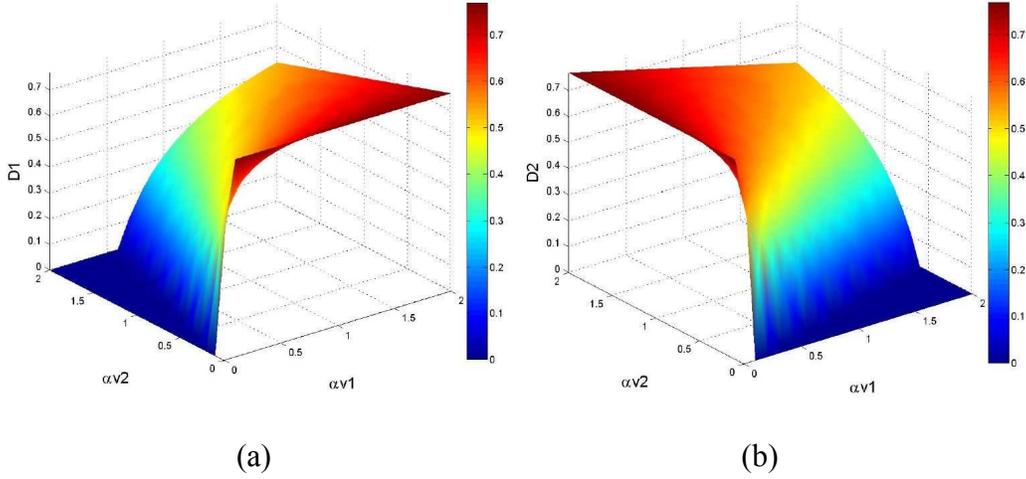


Figure. 3.6: (a) Duty cycle D_1 as a function of α_{v1} and α_{v2} , and (b) Duty cycle D_2 as a function of α_{v1} and α_{v2} for a two-BPM battery system in discharge mode

The relationship between the duty cycle (D_r) and the voltage loop multiplier (α_{vr}) for a N-BPM battery system is given by

$$\frac{\alpha_{vr}}{\alpha_{v1} + \alpha_{v2} + \dots + \alpha_{vN}} \cdot V_{bus} = \frac{1}{1 - D_r} \quad (3.10)$$

where $V_{cell} = 3.7$ V (nominal value) and $V_{bus} = 16$ V (used in the experimental work of this chapter). The relationship between D_r and α_{vr} for a two-BPM battery system is plotted in Fig. 3.6.

Since it is assumed that the power converter components are ideal, the average input and the average output power are equal. Therefore, the following equation can be obtained.

$$V_{cellr} \cdot I_{cellr} = V_r \cdot I_o \quad (3.11)$$

Substituting (3.6) into (3.11) yields

$$V_{cellr} \cdot I_{cellr} = \alpha_{vr} \cdot (V_{Bus-ref} / M_v) \cdot I_o \quad (3.12)$$

The current of the battery cell can be alternatively expressed as a function of the SOC of the battery cell as given by

$$I_{cellr} = Q \cdot (dSOC_r/dt) \quad (3.13)$$

where Q is the rated capacity of the battery cell, assuming that all the battery cells have the same capacity.

By substituting (13) into (12), the following equation can be derived,

$$dSOC_r/dt = \alpha_{vr} \cdot (V_{Bus-ref} / M_v) \cdot I_o / (Q \cdot V_{cellr}) \quad (3.14)$$

The proposed energy sharing controller dynamically control the voltage multiplier values α_{v1} through α_{vN} in order to achieve SOC balancing between the battery cells during discharging operation.

3.6 Proof-Of-Concept Experimental Prototype Results

A. Experimental Setup

To validate and evaluate the performance of the proposed energy sharing controller, a scaled-down distributed battery energy storage system prototype with the proposed energy sharing controller is built in the laboratory. The system configuration of the experimental prototype is illustrated in Fig. 3.5. The experimental prototype consists of two 18650-size cylindrical lithium-ion battery cells, two bidirectional DC-DC synchronous buck/boost power converters and a programmable DC electronic load (Chroma 6312) which is used to emulate the rest of the system after the DC bus. The proposed energy sharing controller is implemented using TMS320F28335 floating-point Microcontroller/DSP from Texas Instrument Inc. (TI). The digital compensators used in the SOC balancing control loop and the voltage control loop are both of PI type. The TMS320F28335 is simply utilized for the proof-of-concept prototyping, which has more than needed processing power and capabilities for the two-cell prototype in this work. In an actual product, depending on the number of cells and the desired performance, a controller with

sufficient processing power can be selected or a special purpose controller specifically designed for the battery system can be developed, in order to optimize the size and cost.

Each of the battery cells used as the inputs/power sources to the DC-DC buck/boost power converters has a rated capacity of 2.6 Ah, a nominal voltage of 3.7 V and a standard discharge/charge rate of 0.5 C (C=2.6Ah). The output of the two DC-DC buck/boost power converters are connected in series in order to provide higher bus voltage ($V_{\text{Bus-ref}}=16$ V). The bidirectional DC-DC buck/boost power converter in each BPM is designed with the parameters listed in Table 3.2.

Table 3.2: Main BPM Design Parameters

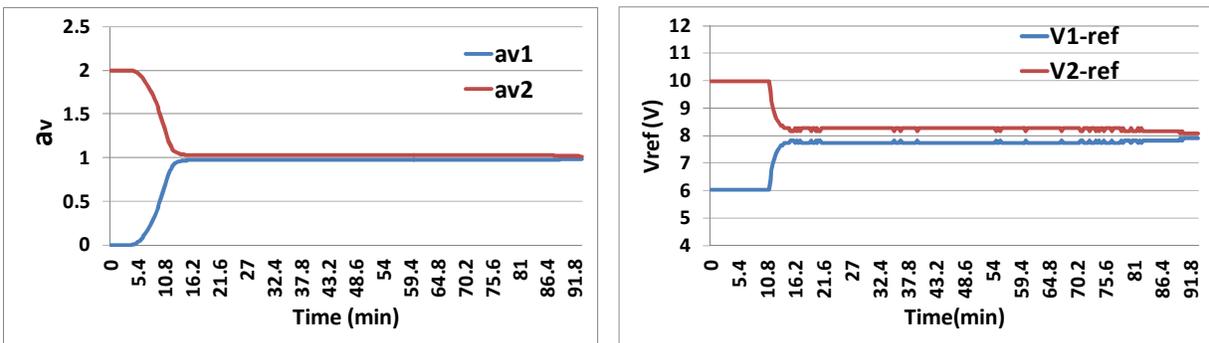
Parameter	Value
$V_{in}=V_{cell}$	3V-4.2V
V_o	6V-10V
L	100 μ H
C_o	220 μ F
f_{sw}	150 kHz
I_o (nominal)	0.65 A

The currents and voltages of the battery cells and the output voltages of the BPMs are sampled by TMS320F28335 built-in/integrated analog-to-digital converter (ADC) module once each switching cycle, i.e., 150 ksps. Each ADC channel in the module has a 12-bit resolution. The implemented digital Pulse-Width-Modulation (DPWM) block has a resolution of 10 bits. There is a variety of methods to estimate the SOC of a battery, including model-based methods as in [88-89] and impedance-based methods as in [60, 90-91]. The focus of this work is on presenting the energy sharing controller for SOC balancing and DC bus voltage regulation. The commonly used coulomb-counting based SOC estimation method is utilized in the experimental work of this paper. This method is simply based on integrating the current flowing in and out of the battery over time without the need for battery cell modeling or impedance measurement.

During system operation, the new SOC values of the battery cells are used/sampled by the SOC balancing loop controller once every 1 second, which is experimentally found to be a suitable value that achieves a good tradeoff between SOC balancing accuracy and speed. The new duty cycle values for the power MOSFET switches in the power converters are updated by TMS320F28335 built-in PWM module once each switching cycle. In order to plot the experimental results for the paper, the voltage/current data of the experimental prototype system are acquired in real-time by using a Keithley data acquisition system (INTEGRA SERIES 2701) in addition to the digital oscilloscope.

B. Experimental Results in Discharge Mode

To test the SOC balancing and DC bus voltage regulation performance of the proposed energy sharing controller during discharging operation, the initial SOC values of the two battery cells in the two BPMs are intentionally made different by 5%. The SOC value, SOC_1 , of the battery cell₁ is 95%, and the SOC value, SOC_2 , of the battery cell₂ is 100%. The initial voltage loop multiplier values, α_{v1} and α_{v2} , are set to be equal to 1. At the beginning of system operation, the SOC balancing loop controller is able to detect that the SOC value of the battery cell₂ is larger than that of the battery cell₁. Therefore, once the SOC balancing closed loop controller is activated, it naturally and quickly forces the voltage loop multiplier value, α_{v2} , for BPM₂ to go to a larger value than the voltage loop multiplier value, α_{v1} , for BPM₁, as shown in Fig. 3.7.



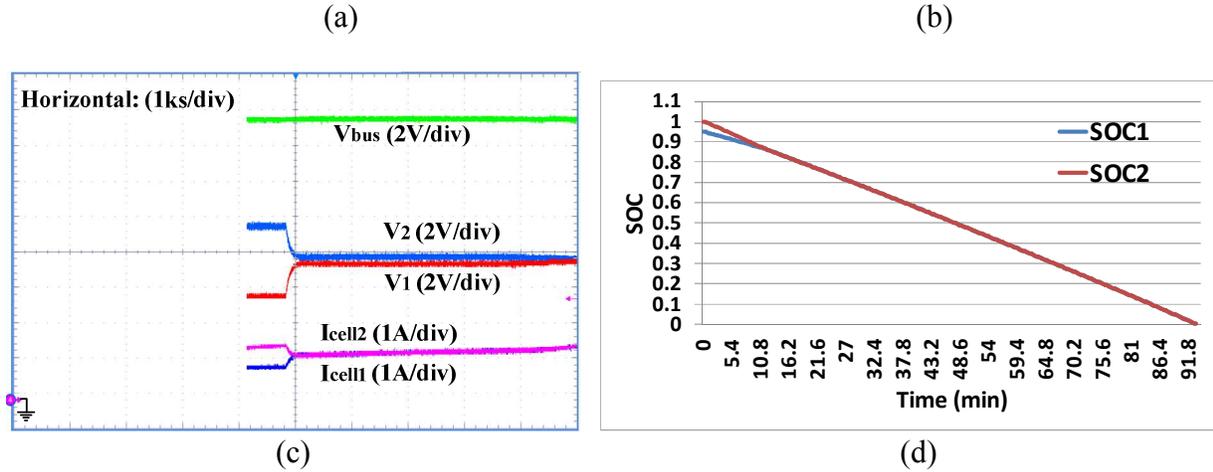


Figure 3.7: Experimental results for (a) voltage multiplier values; (b) BPM output voltage reference values; (c) from top to bottom: bus voltage, the output voltage for BPM₂, the output voltage for BPM₁, the current of the battery cell₂, and the current of the battery cell₁; (d) SOC values of the two battery cells, as the proposed energy sharing controller achieves SOC balancing during battery discharging operation under 5% initial SOC difference between the two battery cells

It can be observed from Fig. 3.7 (a) that α_{v2} reaches the pre-set maximum saturation value, $\alpha_{vmax} = 2$, while α_{v1} reaches the pre-set minimum saturation value, $\alpha_{vmin} = 0$. This is in order to make the output voltage of BPM₂ larger than the output voltage of BPM₁ in order to discharge battery cell₂ faster until SOC balancing is achieved. It can also be observed from Fig. 3.7 (a) that the voltage multiplier values get closer to each other by time until they are both approximately equal to one when both battery cells have the same SOC values as they discharge. Note that the reason why the voltage loop multiplier values are not exactly equal to one after the SOC values get balanced is that the power converters in the two BPMs are not exactly symmetrical due to components manufacturing tolerance, non-uniform PCB traces parasitics and

wiring/connections, among others. The SOC balancing control loop will automatically adjust the voltage loop multiplier values such that the desired SOC balancing is achieved and maintained.

As discussed in Section IV, the BPM output voltage reference for the BPM_r is equal to $V_{r-ref} = V_{Bus-ref} * (\alpha_{vr}/M_v)$. Based on this, once the energy sharing controller is activated, the output voltage reference for BPM₂, V_{2-ref} , should be equal to $V_{Bus-ref}=16$ V while the output voltage reference for BPM₁, V_{1-ref} , should be equal to 0 V. However, because the power converter operates as a boost converter in the discharge mode, the output voltage of the BPM should be higher than the input voltage (i.e., cell voltage, 3 V-4.2 V). For this reason, the minimum output voltage reference value, $V_{min-ref}$, is set to 6 V in this case, while the maximum output voltage reference, $V_{max-ref}$, is set to 10 V ($V_{max-ref} + V_{min-ref} = V_{Bus-ref} = 16$ V). Therefore, V_{1-ref} is forced to be 6 V at the beginning of the operation, while V_{2-ref} is forced to be 10 V, as shown in the experimental result of Fig. 3.7 (b). Then, these two output voltage reference values are utilized in the voltage control loop to regulate the output voltages (V_1 and V_2) for the two BPMs, as shown in Fig. 3.7 (c). The output power for each BPM is a function of the output voltage for the BPM under the same output current. Therefore, the battery cell₂ is discharged at a faster rate than the battery cell₁ at the beginning of the operation, as shown in Fig. 3.7 (d), where the SOC values of the two battery cells are plotted based on the acquired experimental data. It can also be observed from Fig. 3.7 (c) and (d) that as the controller operation progresses, the SOC values of the two battery cells gradually converge closer to each other which in turn makes the output voltage differences between the two BPMs to decrease gradually. Therefore, the discharge rates of the two battery cells gradually get closer to each other. As a result of the proper operation of the energy sharing controller, the SOC values of the two battery cells get balanced approximately $t=10.8$ minutes after the system operation starts, as shown in Fig. 3.7 (d). After that, the output

voltage for each BPM becomes equal because $\alpha_{v1} = \alpha_{v2} = 1$. The SOC balance condition between the two battery cells is maintained until the end of the discharging operation. It is also shown in Fig. 3.7 (c) that the currents of the battery cells ramp up at a faster rate at the end of the discharging operation. This is because the cell voltage drops faster at the end of discharging, more current needs to be drawn from the battery cells in order to deliver desired amount of energy to the load. In addition, the bus voltage, V_{bus} , is always regulated at $V_{Bus-ref} = 16$ V throughout the entire discharging process, as shown in Fig. 3.7 (c).

In most of the practical applications, such as electric vehicle, DC microgrid and laptop computer battery systems, the load current varies by time. Therefore, the SOC balancing performance of the proposed energy sharing controller is further evaluated under a load current transient condition. The initial SOC value of battery cell₁ is 95% while the initial SOC value of battery cell₂ is 100%. A load transient of 0.65 A to 0A is triggered at $t=33$ minutes after system operation starts. The experimental results/data are shown in Fig. 3.8. All results are consistent with the ones shown in Fig. 3.7 except that in this case the currents of the battery cells immediately drop to zero as the load current drops from 0.65 A to 0 A at $t=33$ minutes, as shown in Fig. 3.8 (d). The battery cells start to discharge again as the load current is turned back on from 0 A to 1 A at $t=38$ minutes. It can be observed from Fig. 3.8 (c) that the SOC values of the two battery cells get balanced at approximately $t=11$ minutes and the SOC balancing condition is well maintained until the end of the discharging operation without being interrupted/affected by the load current transients. Moreover, the bus voltage is always maintained at $V_{Bus-ref}=16$ V during the entire discharging operation.

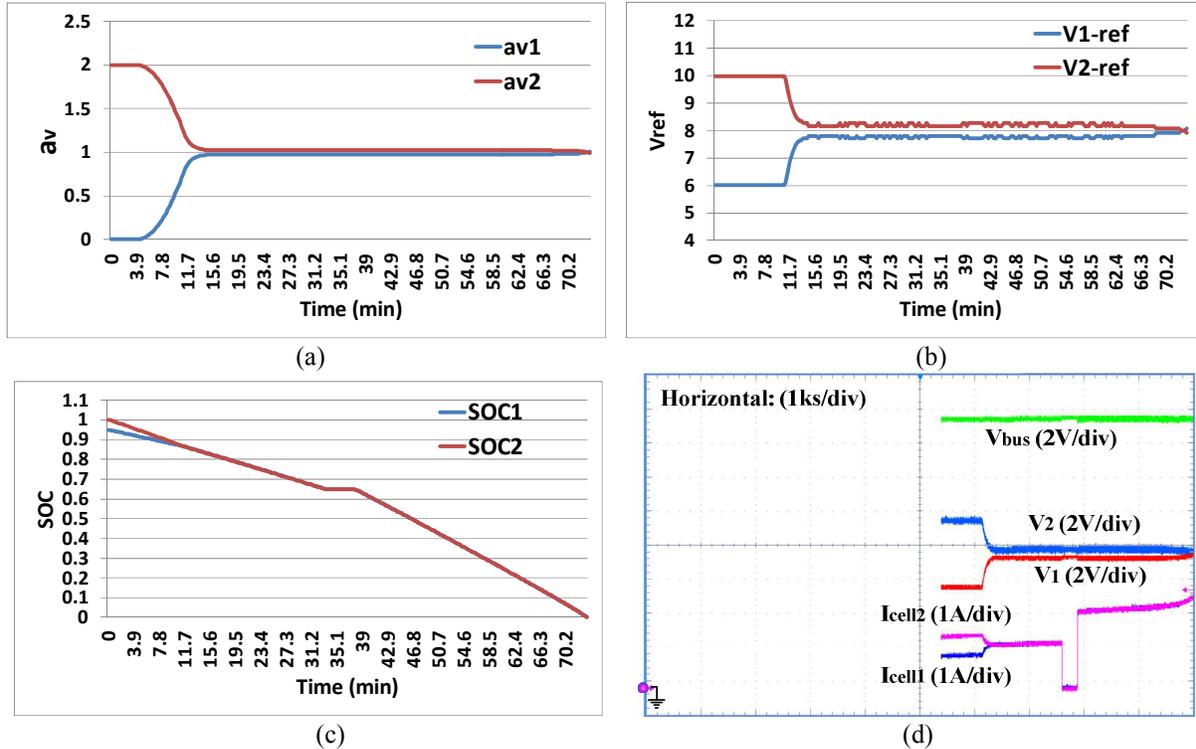


Figure 3.8: Experimental results for (a) voltage multiplier values; (b) BPM output voltage reference values; (c) SOC values of the two battery cells; (d) from top to bottom: bus voltage, the output voltage for BPM₂, the output voltage for BPM₁, the current of the battery cell₂, and the current of the battery cell₁, as the energy sharing controller achieves SOC balancing during discharging under 5% initial SOC difference between the two battery cells and load current transient

3.7 Summary

An energy sharing controller is proposed in this chapter based on a distributed battery energy storage system architecture. The re-designed DC-DC power stage and the proposed energy sharing controller are utilized to achieve SOC balancing between the battery cells while providing DC bus voltage regulation to the rest of the system or load. As a result, there is no need for two independent converter systems for cell SOC balancing and DC bus voltage

regulation. This leads to reduced design complexity of the battery energy storage system. The proposed energy sharing controller addresses the battery cells' SOC imbalance issue from the root by adjusting the discharge rate of each battery cell while maintaining total regulated DC bus voltage. The energy transfer between the battery cells that is usually required in the conventional cell balancing schemes is no longer needed, thus eliminating the power losses caused by the charge/energy transfer process.

The experimental prototype results validate the performance of the proposed energy sharing controller during discharging operation. The developed architecture and energy sharing controller is candidate for many battery energy storage applications including EVs/PHEVs (which utilize power distribution scheme that has a DC-DC power converter), DC microgrids, aerospace battery systems, laptop computers battery packs, and other portable devices with multi-cell battery energy storage.

CHAPTER 4

BATTERY CHARGING CONTROLLER WITH ENERGY SHARING

4.1 Introduction

The energy sharing controller proposed in last chapter addresses the cell balancing issue during battery discharging operation with high cell balancing speed and efficiency while eliminating the need for dedicated cell balancing circuits. Given the differences in the operation nature between battery discharge and charge mode, the energy sharing controller proposed in the last chapter is upgraded in this chapter in order to achieve cell balancing while the battery cells are being charged.

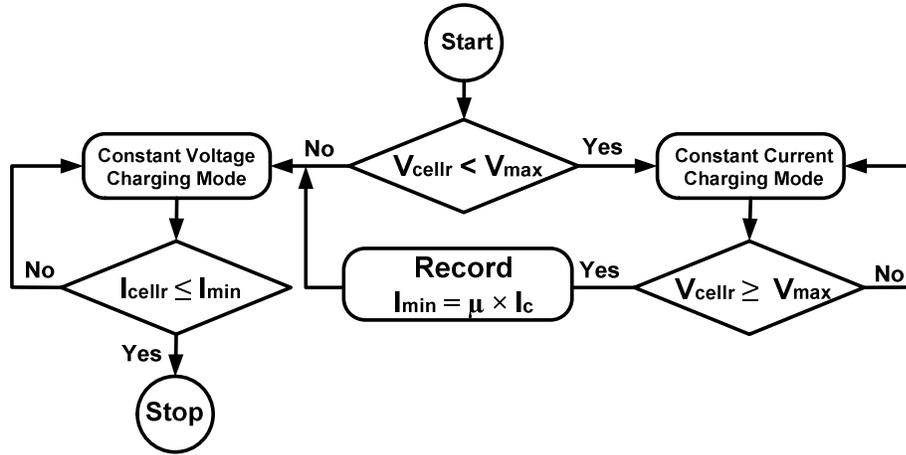
In this chapter, a conventional battery charging control algorithm is first reviewed and then integrated with the energy sharing control concept to produce a complete cell balancing solution for charging mode. The principle of operation of the upgraded battery charging controller with energy sharing is introduced and discussed. The steady-state analysis of the energy sharing controlled distributed battery system is also presented in the context of charging operation. Proof-of-concept experimental results are given to verify the feasibility of the proposed concept. At the end of this chapter, several comments are provided in terms of the cost, efficiency and complexity of the energy sharing controller for both discharging and charging operation.

4.2 Conventional Battery Charging Control Algorithm

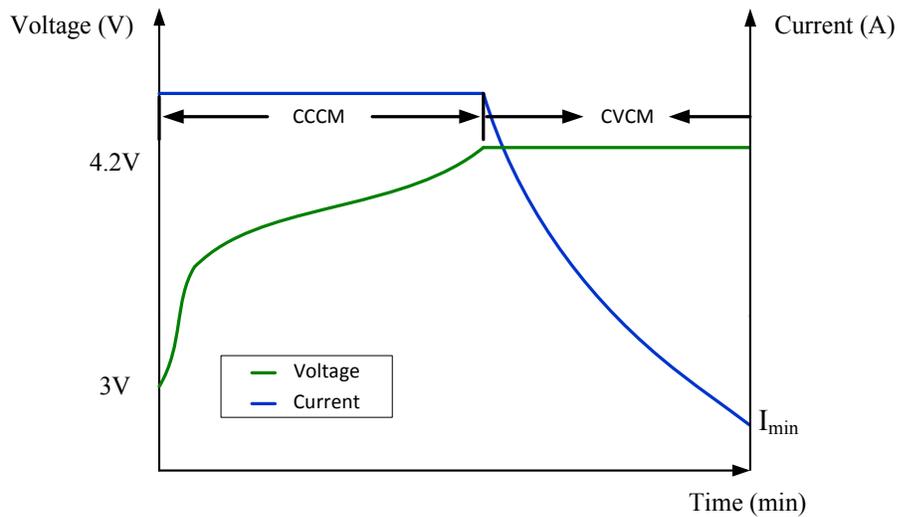
The commonly used battery charging control algorithm include two modes of operation, i.e., constant current charging mode (CCCM) and constant voltage charging mode (CVCM). Fig. 4.1 illustrates a simplified flowchart for the conventional battery charging control algorithm. The controller first operates in CCCM where the cell current is regulated at a desired level (e.g., $I_c/2$, where I_c is battery cell capacity current) until the cell voltage reaches a pre-set maximum value V_{\max} (e.g., 4.2 V for lithium-ion battery). Once this occurs, the controller will then enter CVCM where the cell voltage is regulated at V_{\max} in order to gradually fill up the battery while preventing the cell from being overcharged. The CVCM charging operation is terminated when the cell charging current drops to a certain percentage (e.g., $\mu=5\%$) of I_c .

To speed up the battery charging process in many applications, such as mobile devices and EVs/HEVs, a commonly used approach is to raise the charging current during the CCCM. This would require the battery cell to be capable of handling higher charging rate without compromising its cycle life.

In the next section, this conventional battery charging control algorithm will be integrated with the energy sharing concept in order to address the cell balancing issue during charging operation.



(a)



(b)

Figure. 4.1: (a) A simplified battery charging controller flowchart; (b) A typical charging curve for lithium-ion battery

4.3 Operation of Battery Charging Controller with Energy Sharing

As shown in Fig. 4.2, the charge mode for the distributed battery energy storage system with the upgraded battery controller with energy sharing requires applying a voltage at the DC bus ($V_{bus}=V_{pack}$). During charging operation, the power converters will be operating in buck

mode (with the DC bus as input and the battery cells as output) while realizing energy sharing based control in order to maintain desired SOC balancing between the cells.

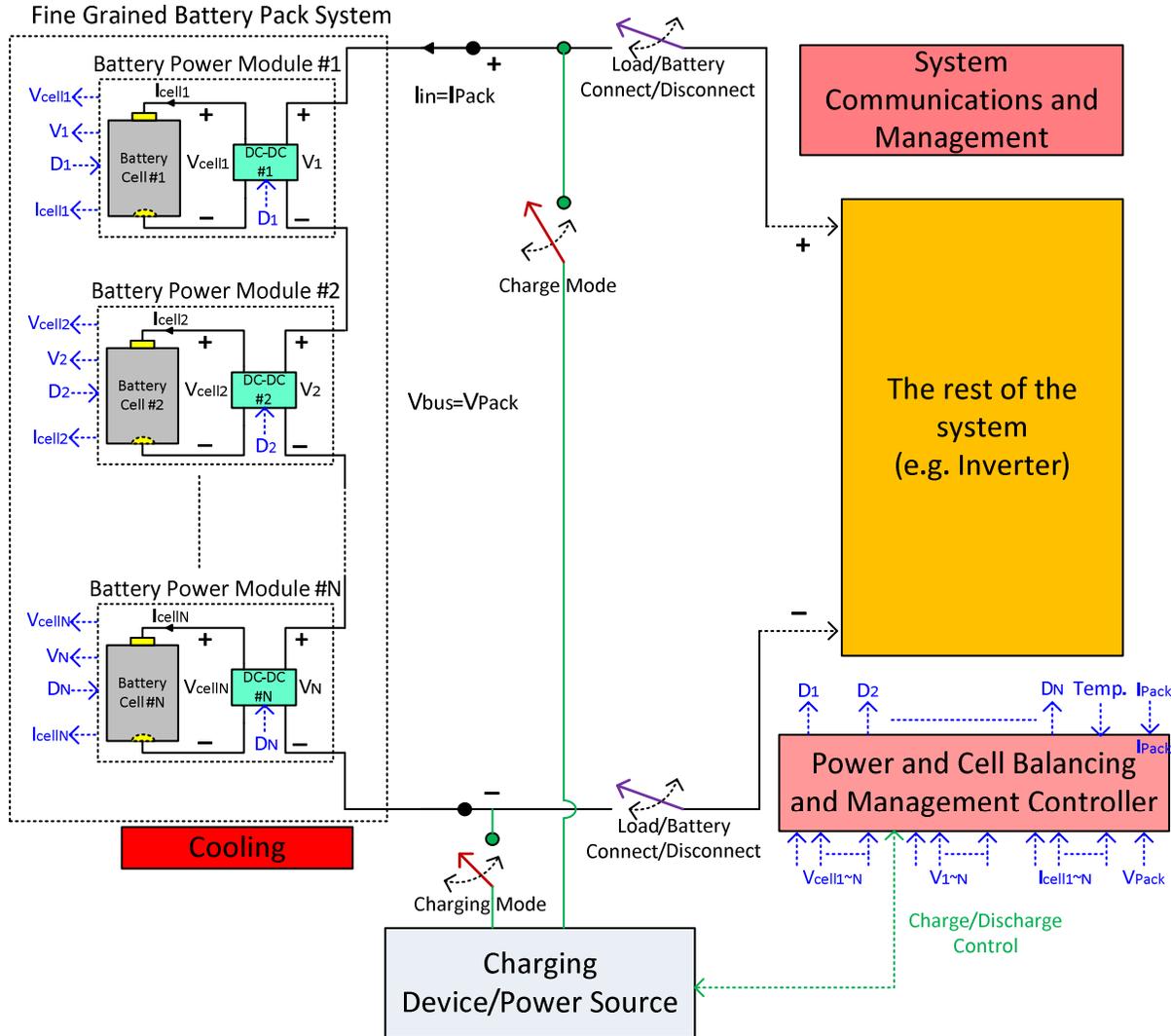


Figure.4.2: Block diagram of the distributed battery energy storage system with the proposed battery charging controller with energy sharing

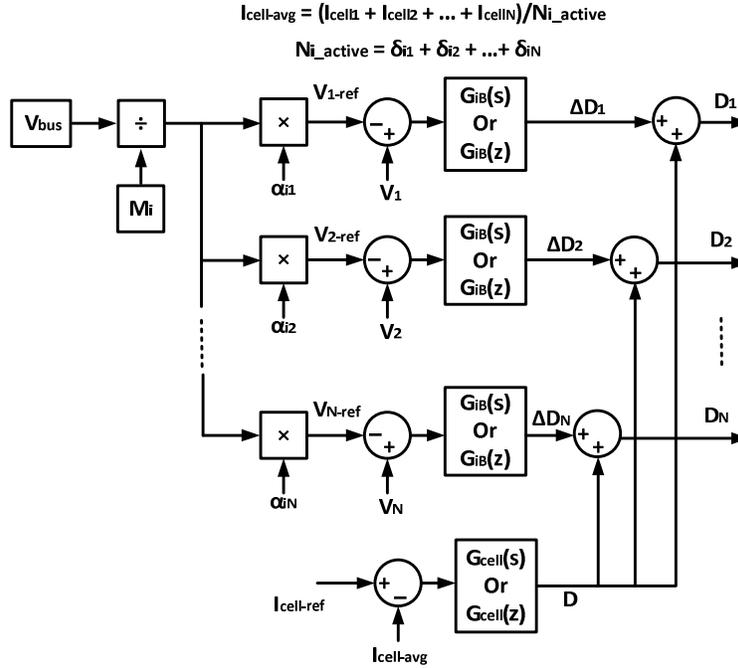


Figure. 4.3: Part 1 of the upgraded battery charging controller's basic block diagram during CCCM operation, i.e., the BPM input voltage control loop and average cell charging current control loop

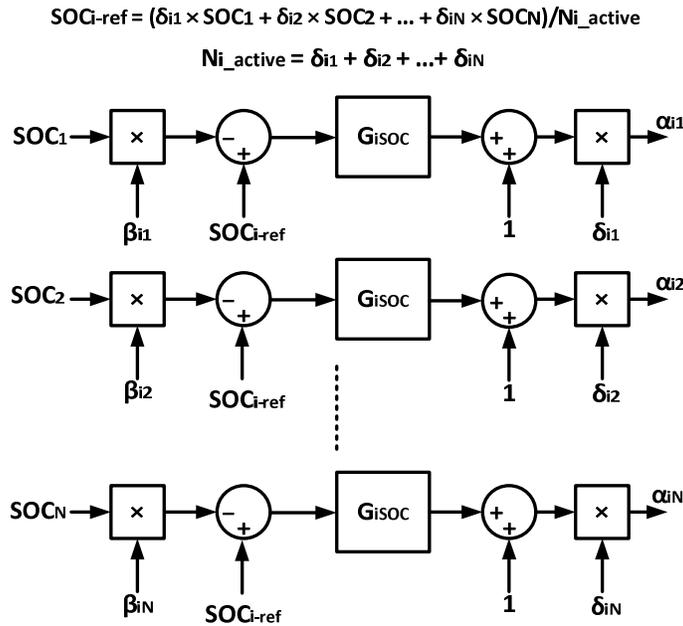


Figure. 4.4: Part 2 of the upgraded battery charging controller's basic block diagram during CCCM operation, i.e., SOC balancing control loop

Fig. 4.3 and Fig. 4.4 illustrate the control block diagrams of the upgraded battery charging controller with energy sharing in CCCM. The energy sharing controller in CCCM operates in a similar manner as in the discharge mode discussed in Chapter 3. It can be seen in Fig. 4.3 and 4.4 that the total input voltage (V_{bus}) of the charging source is shared among the BPMs according to the voltage multiplier values (α_{i1} through α_{iN}) that are generated by the SOC balancing control loop. The input voltage reference value, V_{r-ref} , for BPM_r is given by (4.1). Since the input current I_{in} (or I_{pack}) is the same for all of the BPMs and the power delivered to each battery cell is a function of the input voltage of each BPM. The voltage multiplier values are dynamically controlled through the SOC balancing control loop in order to achieve the SOC balancing between the cells during charging operation.

$$V_{r-ref} = V_{bus} \cdot (\alpha_{ir} / M_i) \quad (4.1)$$

$$M_i = \alpha_{i1} + \alpha_{i2} + \dots + \alpha_{iN} \quad (4.2)$$

The key difference between the operation of the energy sharing controller in the CCCM and the discharging mode is that, during the CCCM operation, an average cell charging current control loop is needed in addition to the voltage control loop and the SOC balancing control loop. This is in order to ensure that the average cell charging current given by (4.3) is regulated at the cell charging current reference value (e.g. 0.5C). This way the charging speed of the whole battery pack is controlled.

$$I_{cell-avg} = (I_{cell1} + I_{cell2} + \dots + I_{cellN}) / N_{i_active} \quad (4.3)$$

Fig. 4.5 illustrates the control block diagram of the battery charging controller during CVCM operation. The average cell voltage given by (4.4) is regulated at the maximum cell voltage reference value. All the BPMs will have the same duty cycle d .

$$V_{cell-avg} = (V_{cell1} + V_{cell2} + \dots + V_{cellN}) / N_{i_active} \quad (4.4)$$

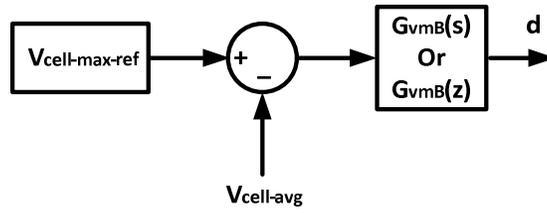


Figure. 4.5: The upgraded battery charging controller's block diagram during CVCM operation

4.4 Steady-State Analysis of The Energy Sharing Controller in Charge Mode

This section presents theoretical steady-state analysis of the energy sharing controlled distributed battery system during charging operation. Fig. 4.6 shows the system configuration of the distributed battery energy storage system architecture with the upgraded battery charging controller. To simplify analysis, assume that all the power converter components are ideal, which means the parasitic values of the components are negligible, except for the internal impedance of the battery cell (Z_{cell}).

For the buck converter topology in Continuous Conduction Mode (CCM) operation, the currents of the battery cells are given by

$$\left\{ \begin{array}{l} I_{cell1} = \frac{I_{pack}}{G_{chg1}} \\ I_{cell2} = \frac{I_{pack}}{G_{chg2}} \\ \quad \quad \quad M \\ I_{cellN} = \frac{I_{pack}}{G_{chgN}} \end{array} \right. \quad (4.5)$$

where G_{chg1} through G_{chgN} are the DC voltage gains for the power converters in BPM_1 through BPM_N in charge mode. D_1 through D_N are the duty cycles for the power converters (each duty cycle is equal to the buck high-side switch ON time divided by the switching period). I_{cell1}

through I_{cellN} are the currents of battery cell₁ through battery cell_N. I_{pack} is the battery pack current (i.e., input charging current).

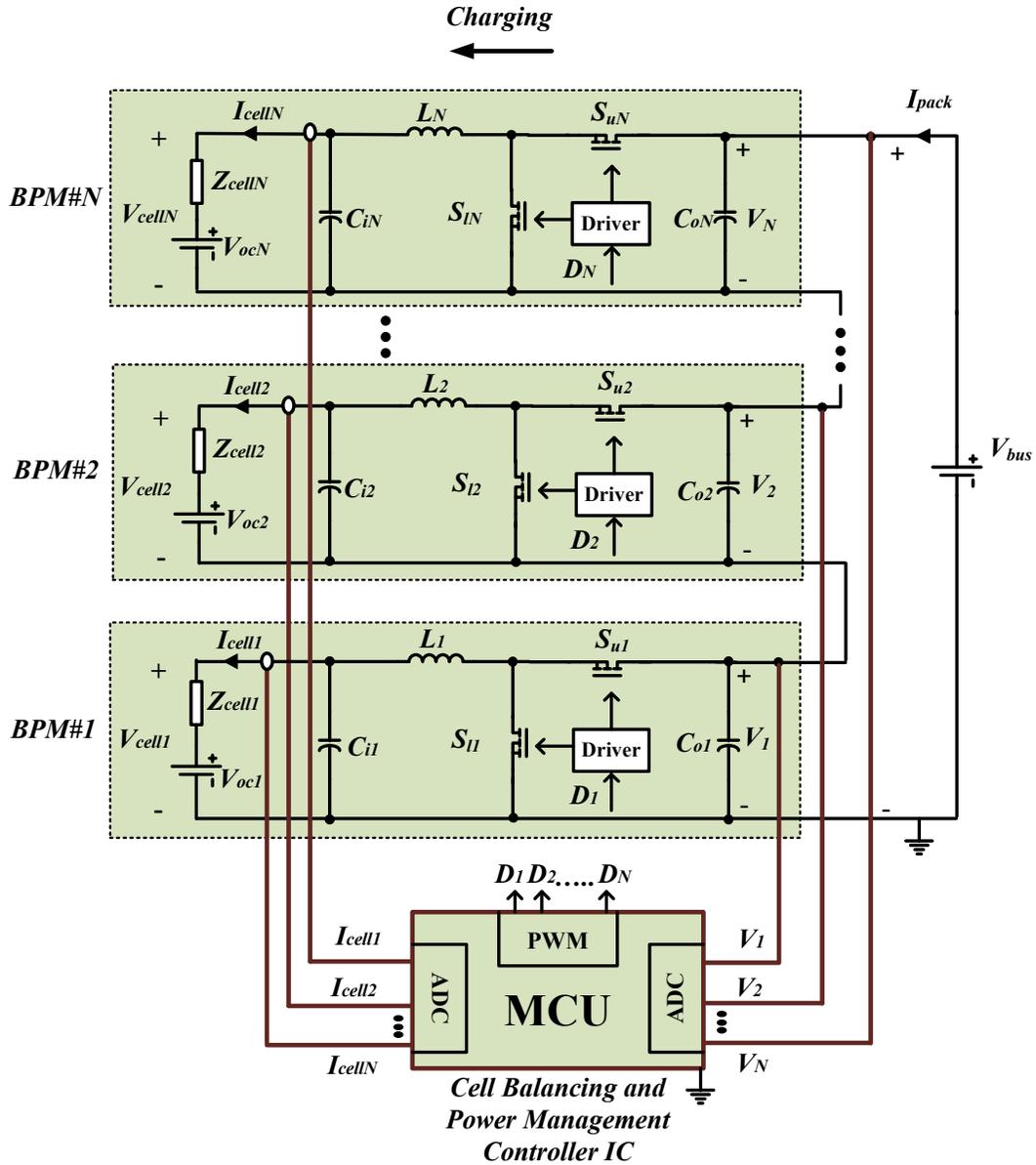


Figure. 4.6: System configuration of the distributed battery energy storage system architecture with the upgraded energy sharing controller in charge mode

As discussed in Section III, the input voltage V_r of the power converter in BPM_r is given by

$$V_r = V_{Bus} \cdot (\alpha_{ir} / M_i) \quad (4.6)$$

For the buck converter topology in CCM operation, the DC voltage gain is given by

$$G_{chgr} = (V_{ocr} + I_{cellr} \cdot Z_{cellr}) / V_r \quad (4.7)$$

where V_{ocr} is the open-circuit voltage of the battery cell; Z_{cellr} is the internal impedance of the battery cell.

By substituting I_{cellr} from (4.5) and V_r from (4.6) into (4.7), the following relationship can be derived

$$G_{chgr} = \frac{V_{ocr} + \frac{I_{pack}}{G_{chgr}} Z_{cellr}}{\frac{\alpha_{ir}}{M_i} V_{Bus}} \quad (4.8)$$

Solving for the DC voltage gain of the buck converter in BPM_r yields

$$G_{chgr} = \frac{V_{ocr} \pm \sqrt{V_{ocr}^2 + 4 \frac{\alpha_{ir}}{M_i} V_{Bus} I_{pack} Z_{cellr}}}{2 \frac{\alpha_{ir}}{M_i} V_{Bus}} \quad (4.9)$$

The relationship between the duty cycle (D_r) and the voltage loop multiplier (α_{ir}) for a N-BPM battery system in charge mode is given by

$$\frac{V_{cell}}{\frac{\alpha_{ir}}{\alpha_{i1} + \alpha_{i2} + \dots + \alpha_{iN}} V_{bus}} = D_r \quad (4.10)$$

where $V_{cell} = 3.7$ V (nominal value) and $V_{bus} = 16$ V (used in the experimental work of this chapter). The relationship between D_r and α_{ir} for a two-BPM battery system is plotted in Fig. 4.7.

Since it is assumed that the power converter components are ideal, the average input and the average output power are equal. Therefore, the following equation can be obtained.

$$V_{cellr} \cdot I_{cellr} = V_r \cdot I_{pack} \quad (4.11)$$

Substituting (4.6) into (4.11) yields

$$V_{cellr} I_{cellr} = \alpha_{ir} \frac{V_{Bus}}{M_i} I_{pack} \quad (4.12)$$

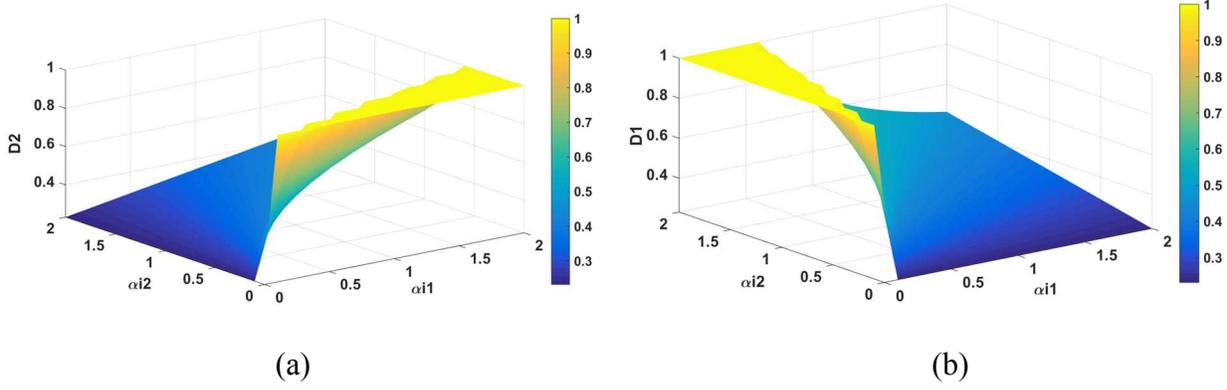


Figure.

4.7: (a) Duty cycle D_1 as a function of α_{i1} and α_{i2} , and (b) Duty cycle D_2 as a function of α_{i1} and α_{i2} for a two-BPM battery system in charge mode

The current of the battery cell can be alternatively expressed as a function of the SOC of the battery cell as given by

$$I_{cellr} = Q \frac{dSOC_r}{dt} \quad (4.13)$$

where Q is the rated capacity of the battery cell, assuming that all the battery cells have the same capacity.

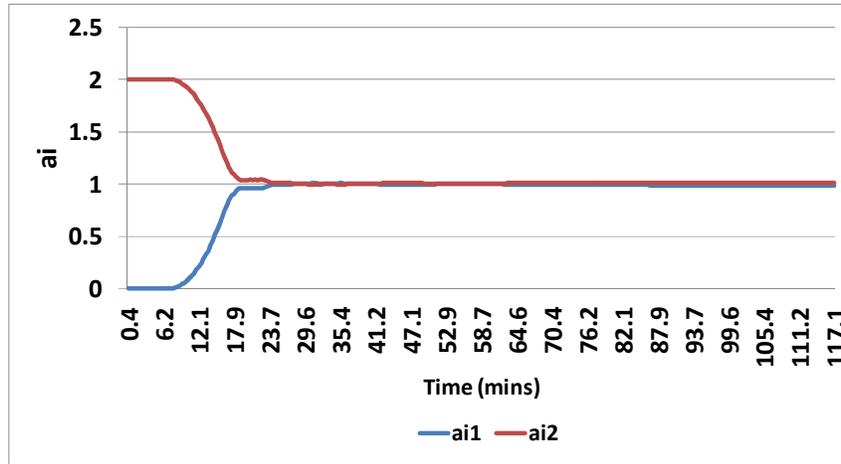
By substituting (4.13) into (4.12), the following equation can be derived,

$$\frac{dSOC_r}{dt} = \frac{\alpha_{ir} \frac{V_{Bus}}{M_i} I_{pack}}{QV_{cellr}} \quad (4.14)$$

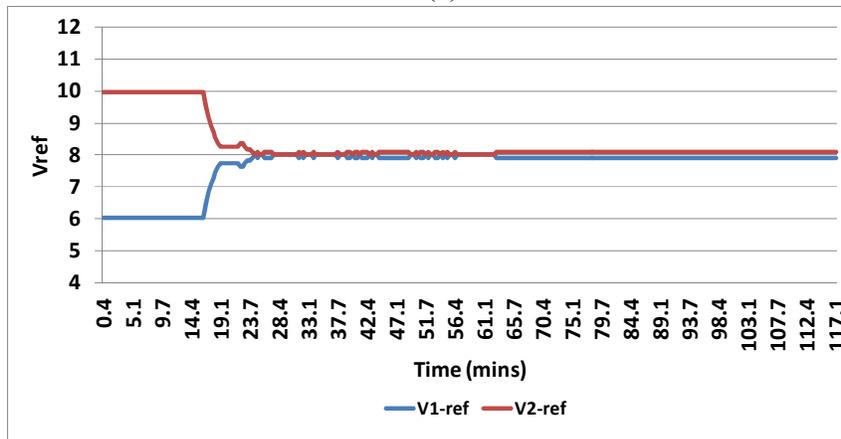
The upgraded energy sharing controller dynamically control the voltage multiplier values α_{i1} through α_{iN} in order to achieve SOC balancing between the battery cells during charging operation.

4.5 Experimental Results in Charge Mode

The performance of the upgraded battery charging controller with energy sharing is tested and evaluated during battery charging operation. The initial SOC values of the two battery cells in the two BPMs are intentionally made different by 5%. The SOC value, SOC_1 , of the battery cell₁ is 5%, and the SOC value, SOC_2 , of the battery cell₂ is 0%.



(a)



(b)

Figure. 4.8: Experimental results for (a) voltage multiplier values; (b) BPM input voltage reference values

As shown in Fig. 4.8 (a) and (b), at the beginning of the operation, the energy sharing controller is able to detect that the SOC value of battery cell₁ is larger than that of the battery

cell₂. Therefore, the voltage loop multiplier value (α_{i2}) for BPM₂ is forced to be larger than the voltage loop multiplier value (α_{i1}) for BPM₁, which makes the input voltage reference value (V_{2-ref}) for BPM₂ larger than the input voltage reference value (V_{1-ref}) for BPM₁. Because the input current is the same for the two BPMs in this case, the battery cell₂ is charged at a faster rate than the battery cell₁. The SOC values of the two battery cells gradually get closer to each other and get balanced at time $t=14.4$ minutes after the system charging operation starts. After this time, the voltage multiplier values for two BPMs are kept close to each other in order to maintain the SOC balancing between the two battery cells. As a result of the additional average cell current control loop, the average cell charging current of the two battery cells is regulated at 1.3A (0.5C) during CCCM operation but initially the charging rate of battery cell₂ is automatically controlled to be larger than the charging rate of battery cell₁, as shown in Fig. 4.9 (a), in order to balance SOC during charging operation.

As can be observed from Fig. 4.9 (a) and (b), the energy sharing controller enters CVCM when the cell voltage reaches 4.2 V at $t=98.4$ minutes. During CVCM operation, the charging currents of the battery cells naturally decrease in order to maintain the cell voltage regulated at 4.2 V. Consequently, the SOC values of the two battery cells ramp up at a lower rate in CVCM compared to CCCM. The CVCM operation is terminated when the cell charging current drops to 0.13 A. It is also shown in Fig. 4.9 (b) that the SOC balancing of the two battery cells are maintained until the end of the entire charging process without being interrupted/affected by the mode transition.

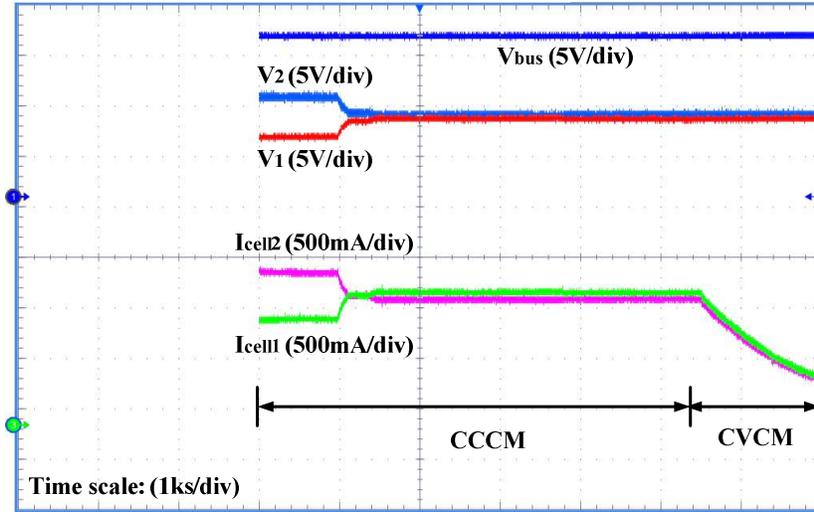
4.6 Additional Comments

A. Comment on the efficiency of the system

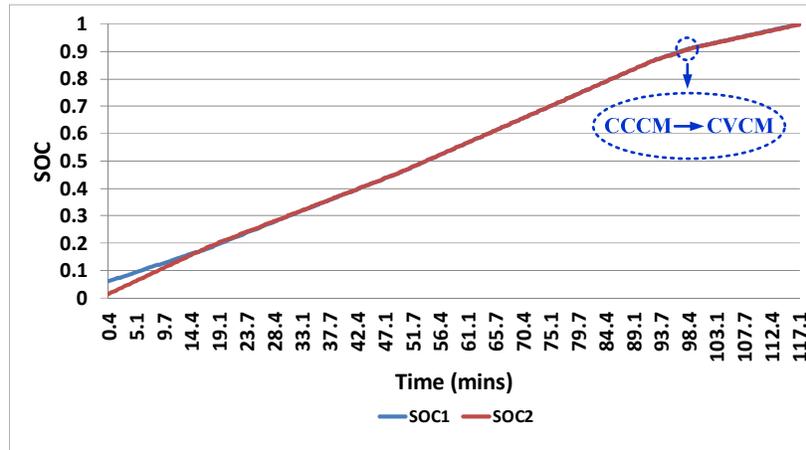
The efficiency (η) of the system is given by

$$\eta = \frac{P_{o1} + P_{o2} + \dots + P_{oN}}{P_{in1} + P_{in2} + \dots + P_{inN}} = \frac{\eta_1 \cdot P_{in1} + \eta_2 \cdot P_{in2} + \dots + \eta_N \cdot P_{inN}}{P_{in1} + P_{in2} + \dots + P_{inN}} \quad (4.15)$$

where η_1 through η_N are the efficiency values, P_{o1} through P_{oN} are the output power values, and P_{in1} through P_{inN} are the input power values of the power converters in BPM₁ through BPM_N, respectively.



(a)



(b)

Figure. 4.9: (a) SOC values of the two battery cells; (b) from top to bottom: bus voltage, the input voltage for BPM₂, the input voltage for BPM₁, the charging current of the battery cell₂, and the charging current of the battery cell₁, as the energy sharing controller achieves SOC balancing during charging under 5% initial SOC difference between the two battery cells

With an optimized design based on the state-of-art commercially available electronic devices and PCB layout technique, the bidirectional DC-DC buck/boost converter used in each BPM can achieve a peak efficiency of 96%-98%, therefore, the overall efficiency η of the complete system is 96%-98%. Compared to the conventional architecture where there are independent cell SOC balancing converter across each cell in addition to the high-power DC bus voltage regulation converter, the proposed architecture is expected to have comparable or higher efficiency because:

1) Power loss exists in the cell balancing converters in the conventional architecture. This power loss is caused by the energy transfer between the battery cells in order to achieve cell balancing. In this work, the same power conversion stage used for voltage regulation is also used for SOC balancing without the need to add additional SOC balancing circuits or converters for each cell.

2) High-power-rating devices are needed for the big high-power DC bus voltage regulation converter in the conventional architecture. Generally speaking, high-power-rating devices have higher parasitic component values which lead to higher power loss and lower efficiency than the small low-power converters utilized in this work.

B. Comment on the cost of the system

The cost incurred in the larger high-power DC-DC power converter in the conventional architecture is replaced by the cost incurred by the smaller lower-power DC-DC power converters in the distributed architecture. The cost and power loss of the cell balancing circuits or converters placed across the cells in order to achieve SOC balancing in the conventional architecture are eliminated when using the energy sharing controller architecture presented in

this work. The proposed energy sharing controller which is able to achieve DC bus voltage regulation in addition to SOC balancing is relatively simple.

C. Comment on current sensing

During discharging operation, the proposed energy sharing controller does not necessarily require current sensing. Current sensors are used in the discharging mode to obtain the currents of the cells in order to calculate the SOC values of the cells based on the conventional coulomb counting method. While it is one of the most accurate options to obtain SOC information and balance cells' SOC values for charge equalization, cell-voltage based charge balancing is commonly used in the literature, as in [63, 66-67, 73-74]. If cell-voltage based charge balancing is used, current sensing is not needed. In fact, the energy sharing controller also works for cell voltage-based charge balancing. The control diagram for cell-voltage based charge balancing for the proposed energy sharing controller is illustrated in Fig. 4.10. In Fig. 4.10, the cell voltages ($V_{cell1}, V_{cell2}, \dots, V_{cellN}$) replaces the SOC values ($SOC_1, SOC_2, \dots, SOC_N$) in Fig. 4.4.

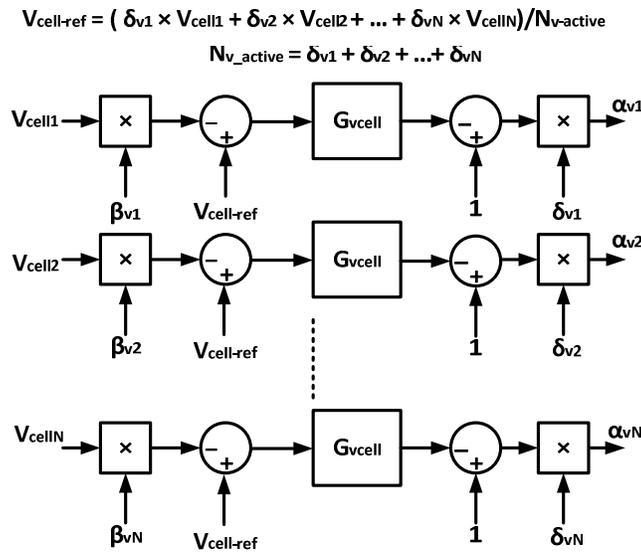


Figure. 4.10: Part 2 of the energy sharing controller's basic block diagram during discharging operation with cell-voltage based charge balancing control loop

During the charging operation, the proposed energy sharing controller does require current sensing for the battery cells. However, another option which can be used to reduce current sensing size and cost is to indirectly sense the current values. Instead of using the conventional sensing resistor method that results in additional power dissipation and increase in size and cost, the method that utilizes FET drain-source resistance ($R_{ds(on)}$) as an indirect way to sense the current can be utilized [95-96]. In the bidirectional buck/boost converter topology utilized in this work, two power MOSFETs are used as the switching devices. By measuring the voltage at the switching node (the point where the two FETs are connected), the current information can be obtained.

4.7 Summary

The energy sharing controller proposed in last chapter is upgraded in this chapter by integrating a battery charging control algorithm with the energy sharing concept in order to address the cell balancing issue during charging operation. The upgraded energy sharing controller also addresses the battery cells' SOC imbalance issue from the root by adjusting the charge rate of each battery cell while maintaining the average cell current to be regulated at the desired level. The energy transfer between the battery cells that is usually required in the conventional cell balancing schemes is also eliminated. This leads to increased efficiency of the battery system. The experimental prototype results validate the performance of the upgraded energy sharing controller during charging operation.

CHAPTER 5

SMALL-SIGNAL MODELING AND ENERGY SHARING CONTROLLER DESIGN

5.1 Introduction

An energy sharing controller has been proposed and developed in Chapter 3 to achieve cell balancing in battery discharge mode with high cell balancing speed and efficiency. The energy sharing concept is upgraded and integrated with a battery charging algorithm in Chapter 4 in order to achieve cell balancing during battery charging operation. Steady-state operation and analysis of the energy sharing controller has been presented in Chapter 3 and 4 for discharging and charging operation, respectively. In order to gain deeper insights into the dynamics of the energy sharing controlled distributed battery system and facilitate the energy sharing controller design, detailed small-signal modeling and analysis is performed in this chapter for each operating mode, i.e., discharge mode, constant current charging mode and constant voltage charging mode. In each mode, the corresponding small signal model of the system is first constructed followed by derivation of associated transfer functions. Finally, the control loops including BPM voltage, SOC balancing, average cell current and average cell voltage loops are compensated based on rule-of-thumb frequency-domain design guidelines and criteria, i.e., control bandwidth and stability margins.

Several different small-signal modeling techniques are introduced and discussed in [97], including basic AC modeling, state-space averaging, circuit averaging techniques. While the procedures of each modeling technique may vary, the end results are essentially the same. In this

paper, the state-space averaging method is employed to derive the small-signal models and associated transfer functions.

Section 5.2 to Section 5.4 of this Chapter presents the small-signal modeling analysis, transfer functions derivation in addition to the compensators design for various operating modes. Simulation model and experimental prototype results are presented and discussed in Section 5.5 in order to validate the effectiveness of the derived small signal models and controller design. Summary of this chapter is given in Section 5.6.

5.2 Energy Sharing Controller Modeling and Design For Discharge Operation

A. Small-Signal Model

Based on the control block diagrams shown in Fig. 3.3 and 3.4 in Chapter 3, the small-signal model for the energy sharing controlled distributed battery system in discharge mode can be derived as shown in Fig. 5.1. Note that all the variables shown in Fig. 5.1 are AC small signals. The transfer functions and symbols shown in Fig. 5.1 are described below. All the following transfer functions are for discharging operation unless otherwise noted. For generalization, all the transfer function are for r^{th} BPM.

$T_{vr-dhg}(s)$: BPM output voltage control loop gain;

$T_{socr-dhg}(s)$: SOC balancing control loop gain;

$G_{vdr-dhg}(s)$: duty cycle control to BPM output voltage transfer function;

$G_{idr-dhg}(s)$: duty cycle control to cell current transfer function;

$Z_{or}(s)$: BPM open loop output impedance transfer function;

$G_{socir-dhg}(s)$: cell current to cell SOC transfer function;

$G_{vr-dhg}(z)$: BPM output voltage control loop compensator;

$G_{socr-dhg}(z)$: SOC balancing control loop compensator;

$K_{dr-dhg}(s)$: BPM output voltage sensing gain (including the voltage sensor gain and the analog-to-digital converter gain);

$F_{mr-dhg}(s)$: PWM modulator gain;

$H_{cr-dhg}(s)$: digital controller computation delay model;

$ZOH_{vr-dhg}(s)$: zero order hold model for BPM output voltage sampling;

$ZOH_{icellr-dhg}(s)$: zero order hold model for cell current sampling;

$ZOH_{socr-dhg}(s)$: zero order hold model for cell SOC sampling;

The converter design parameters and equilibrium operating point (when the battery cells are balanced) are the same for all the BPMs. Therefore, the compensators design for all the BPMs are identical. The following section presents the derivation of the transfer functions for r^{th} BPM during discharging operation.

B. Derivation of Transfer Functions

In discharge mode, the BPM converters operate in boost mode with the battery cells being the inputs as shown in Fig. 5.2. The independent state variables of a BPM converter in this mode are the inductor current or cell current $i_{\text{cell}}(t)$ and the BPM converter output voltage $v(t)$. The input variables are cell open circuit voltage $V_{\text{oc}}(t)$ and output current or battery pack current $i_{\text{pack}}(t)$. The output variables are the same as the state variables.

Next, the state equations for r^{th} BPM during each subinterval are derived from Fig. 5.2. When S_{lr} is on and S_{ur} is off during $d_r T_s$ time duration, the state equations are

$$\begin{cases} L \frac{di_{\text{cell}r}(t)}{dt} = v_{\text{ocr}}(t) - i_{\text{cell}r}(t) \cdot Z_{\text{cell}r} \\ C \frac{dv_r(t)}{dt} = -i_{\text{pack}}(t) \end{cases} \quad (5.1)$$

where d_r is the duty cycle and T_s is the switching period of the BPM converter. Other variables are as defined in Fig. 5.2. When S_{ur} is on and S_{lr} is off during $(1-d_r)T_s$ time duration, the state equation is given by

$$\begin{cases} L \frac{di_{cellr}(t)}{dt} = v_{ocr}(t) - i_{cellr}(t) \cdot Z_{cellr} - v_r(t) \\ C \frac{dv_r(t)}{dt} = i_{cellr}(t) - i_{pack}(t) \end{cases} \quad (5.2)$$

Equations (5.1) and (5.2) can be rewritten in the following state-space form:

$$K \frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \quad (5.3)$$

$$K \frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \quad (5.4)$$

Where $K = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}$, $A_1 = \begin{bmatrix} -Z_{cellr} & 0 \\ 0 & 0 \end{bmatrix}$, $B_1 = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$, $A_2 = \begin{bmatrix} -Z_{cellr} & -1 \\ 1 & 0 \end{bmatrix}$, $B_2 = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$, $x(t) = \begin{bmatrix} i_{cellr}(t) \\ v_r(t) \end{bmatrix}$, and $u(t) = \begin{bmatrix} v_{ocr}(t) \\ i_{pack}(t) \end{bmatrix}$.

The next step is to evaluate the state-space averaged equilibrium equations. The averaged matrix A is

$$A = D_r A_1 + D_r' A_2 = D_r \begin{bmatrix} -Z_{cellr} & 0 \\ 0 & 0 \end{bmatrix} + D_r' \begin{bmatrix} -Z_{cellr} & -1 \\ 1 & 0 \end{bmatrix} = \begin{bmatrix} -Z_{cellr} & -D_r' \\ D_r' & 0 \end{bmatrix} \quad (5.5)$$

where $D_r' = 1 - D_r$

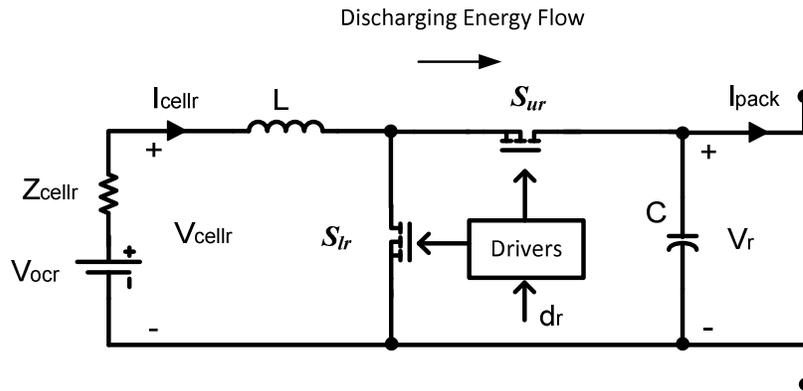


Figure. 5.2: Circuit diagram of the BPM operating as a boost converter in discharge mode

Similarly, the averaged matrix B is

$$B = D_r B_1 + D_r' B_2 = D_r \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} + D_r' \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \quad (5.6)$$

Then the equilibrium state vector X is

$$X = -A^{-1}BU = - \begin{bmatrix} -Z_{cellr} & -D_r' \\ D_r' & 0 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} V_{ocr} \\ I_{pack} \end{bmatrix} = \frac{1}{D_r'^2} \begin{bmatrix} D_r' I_{pack} \\ D_r' V_{ocr} - Z_{cellr} I_{pack} \end{bmatrix} \quad (5.7)$$

For the distributed battery system design presented in chapter 3, the equilibrium (DC) operating point parameters are listed in Table 5.1 and the BPM power stage parameters are given in Table 5.2.

The vector coefficient of $\widehat{d_r(t)}$ is

$$(A1 - A2)X + (B1 - B2)U = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} X + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{ocr} \\ I_{pack} \end{bmatrix} = \frac{1}{D_r'^2} \begin{bmatrix} D_r' V_{ocr} - Z_{cellr} I_{pack} \\ -D_r' I_{pack} \end{bmatrix} \quad (5.8)$$

where $\widehat{d_r(t)}$ is the small signal variation of $d_r(t)$ around its equilibrium operating point D_r .

Table 5.1: Equilibrium (DC) Operating Point Parameter Values in Discharge Mode

Parameter	Value
V_{cellr}	3.7V
V_r	8V
$V_{bus-ref}$	16V
M_v	2
$\alpha_{v1} = \alpha_{v2}$	1
Z_{cellr}	65m Ω
I_{pack}	0.65A
D_r	0.5492
D_r'	0.4508

Table 5.2: Main BPM Design Parameters

Parameter	Value
$V_{in} = V_{cell}$	3V-4.2V
V_r	6V-10V
L	100 μ H
C_o	220 μ F
f_{sw}	150 kHz
$I_{pack} (nominal)$	0.65 A
$Q (rated)$	2.6 Ah

The small-signal AC state equations therefore become

$$\begin{aligned} \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \widehat{i_{cellr}}(t) \\ \widehat{v_r}(t) \end{bmatrix} &= \begin{bmatrix} -Z_{cellr} & -D_r' \\ D_r' & 0 \end{bmatrix} \begin{bmatrix} \widehat{i_{cellr}}(t) \\ \widehat{v_r}(t) \end{bmatrix} \\ + \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} \widehat{v_{ocr}}(t) \\ \widehat{i_{pack}}(t) \end{bmatrix} &+ \frac{1}{D_r'^2} \begin{bmatrix} D_r' V_{ocr} - Z_{cellr} I_{pack} \\ -D_r' I_{pack} \end{bmatrix} \widehat{d}(t) \end{aligned} \quad (5.9)$$

When written in scalar form, (5.9) becomes

$$\begin{cases} L \frac{d\widehat{i_{cellr}}(t)}{dt} = -Z_{cellr} \widehat{i_{cellr}}(t) - D_r' \widehat{v_r}(t) + \widehat{v_{ocr}}(t) \\ \quad + \frac{1}{D_r'^2} (D_r' V_{ocr} \widehat{d}(t) - Z_{cellr} I_{pack} \widehat{d}(t)) \\ C \frac{d\widehat{v_r}(t)}{dt} = D_r' \widehat{i_{cellr}}(t) - \widehat{i_{pack}}(t) - \frac{I_{pack}}{D_r'} \widehat{d}(t) \end{cases} \quad (5.10)$$

Since the dynamics of the cell open circuit voltage variation $\widehat{v_{ocr}}(t)$ is very slow compared to the dynamics of the BPM converter, it can be assumed that the AC small signal variation of the cell open circuit voltage around its equilibrium point is 0, i.e., $\widehat{v_{ocr}}(t)=0$. Based on this, performing Laplace Transformation on (5.10) yields

$$\begin{cases} sL \widehat{i_{cellr}}(s) = -Z_{cellr} \widehat{i_{cellr}}(s) - D_r' \widehat{v_r}(s) + \frac{1}{D_r'^2} (D_r' V_{ocr} \widehat{d_r}(s) \\ \quad - Z_{cellr} I_{pack} \widehat{d_r}(s)) \\ sC \widehat{v_r}(s) = D_r' \widehat{i_{cellr}}(s) - \widehat{i_{pack}}(s) - \frac{1}{D_r'} I_{pack} \widehat{d_r}(s) \end{cases} \quad (5.11)$$

where s is the Laplace Transform operator ($s=j\omega$). Let the small signal variation of independent variable $\widehat{i_{pack}}(s) = 0$ and simplify (5.11) yields

$$\begin{cases} sL \widehat{i_{cellr}}(s) = -Z_{cellr} \widehat{i_{cellr}}(s) - D_r' \widehat{v_r}(s) + \frac{1}{D_r'^2} (D_r' V_{ocr} \widehat{d_r}(s) \\ \quad - Z_{cellr} I_{pack} \widehat{d_r}(s)) \\ sC \widehat{v_r}(s) = D_r' \widehat{i_{cellr}}(s) - \frac{1}{D_r'} I_{pack} \widehat{d_r}(s) \end{cases} \quad (5.12)$$

Based on (5.12), the following transfer functions can be derived

$$G_{vdr-dhg}(s) = \frac{\widehat{v_r}(s)}{\widehat{d_r}(s)} = \frac{-(sL+Z_{cellr})\frac{I_{pack}}{D_r'} + \frac{1}{D_r'}(D_r' V_{ocr} - Z_{cellr} I_{pack})}{(sL+Z_{cellr})sC + D_r'^2} \quad (5.13)$$

$$G_{idr-dhg}(s) = \frac{i_{cellr}(s)}{d_r(s)} = \frac{I_{pack} + \frac{1}{D_r'^2} SC(D_r' V_{ocr} - Z_{cellr} I_{pack})}{(SL + Z_{cellr})SC + D_r'^2} \quad (5.14)$$

Likewise, let the AC small signal variation of another independent variable $d_r(s) = 0$ and simplify (5.11) yields

$$\begin{cases} SL i_{cell}(s) = -Z_{cellr} i_{cell}(s) - D_r' v_r(s) \\ SC v_r(s) = D_r' i_{cell}(s) - i_{pack}(s) \end{cases} \quad (5.15)$$

Based on (5.15), the following transfer function can be derived,

$$Z_{or}(s) = \frac{v_r(s)}{i_{pack}(s)} = \frac{-(SL + Z_{cellr}) \frac{I_{pack}}{D_r'} + \frac{1}{D_r'} (D_r' V_{ocr} - Z_{cellr} I_{pack})}{(SL + Z_{cellr})SC + D_r'^2} \quad (5.16)$$

$$G_{socir-dhg}(s) = \frac{SOC_r(s)}{i_{cellr}(s)} = \frac{-T_s}{Q} \quad (5.17)$$

where T_s is the sampling period of the BPM output voltage, cell current and cell voltage and it is set to be $13.33\mu s$ (i.e., sampling frequency = 75 kHz); Q is the rated capacity of the battery cell in coulomb.

C. Compensator Design

a) Voltage Loop Compensator Design

According to the small-signal model shown in Fig. 5.1, the discrete-time transfer function of the r^{th} BPM converter plant in discharge mode $G_{pr-dhg}(z)$ includes the sampler, ZOH, the BPM output voltage sensing gain K_{dr-dhg} , the digital controller computation delay model $H_{cr-dhg}(s)$, in addition to the continuous-time plant $G_{vdr-dhg}(s)$. $G_{pr-dhg}(z)$ is given by (5.18) and its bode plot is represented by the dashed curve in Fig. 5.3.

$$G_{pr-dhg}(z) = Z\{ZOH_{vr-dhg}(s) \cdot H_{cr-dhg}(s) \cdot F_{mr-dhg}(s) \cdot G_{vdr-dhg}(s) \cdot K_{dr-dhg}\} = \frac{-0.0002276z^2 - 0.0002599z + 0.0007946}{z^3 - 1.99z^2 + 0.9914z} \quad (5.18)$$

where

$$ZOH_{vr-dhg}(s) = \frac{1 - e^{-sT_s}}{s};$$

$H_{cr-dhg}(s) = e^{-sT_d}$; T_d is the digital controller computation delay and it is equal to $T_d = 1.5T_{sw}$

in the experimental implementation;

$$F_{mr-dhg}(s) = \frac{1}{1024} ;$$

$$K_{dr-dhg} = 11.13.$$

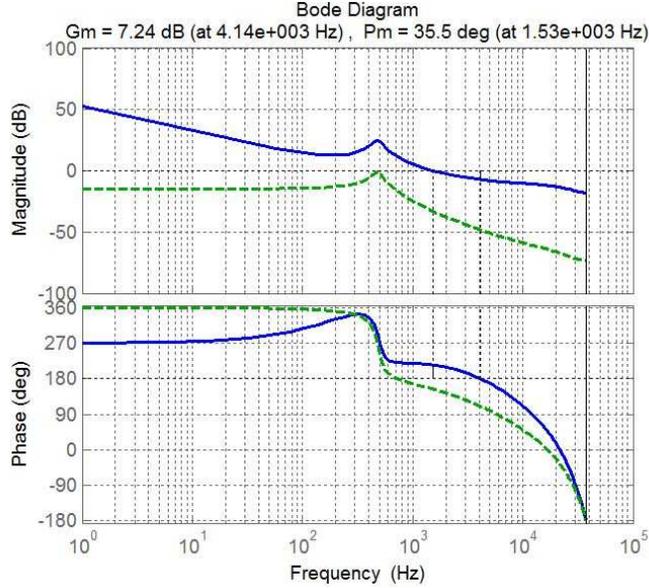


Figure. 5.3: The bode plot of the uncompensated (dashed curve) and compensated (solid curve)

BPM output voltage control loop gain in discharge mode

In this voltage control loop design, the target control bandwidth is limited by the right-half-plane (RHP) zero located at 3.87 kHz, as can be observed from the dashed curve in Fig. 5.3.

With a compensator $G_{vr-dhg}(z)$ given by (5.19), the compensated BPM output voltage control loop gain ($T_{vr-dhg}(z) = G_{pr-dhg}(z) \cdot G_{vr-dhg}(z)$) achieves a control bandwidth of 1.53 kHz and a phase margin of 35.5°, as shown on the solid curve in Fig. 5.3.

$$G_{vr-dhg}(z) = \frac{0.06059z - 0.06007}{z^2 - 1.99z + 0.9914} \quad (5.19)$$

b) SOC Balancing Loop Compensator Design

According to the small-signal model shown in Fig. 5.1, the uncompensated SOC loop gain (i.e., with unity SOC loop compensator gain) is given by (5.20) and its bode plot is represented by the dashed curve in Fig. 5.4.

$$T_{socr-dhg-uncomp}(z) = Z \left\{ G_{idr-dhg}(s) \cdot ZOH_{icellr-dhg}(s) \cdot G_{socir-dhg}(s) \cdot ZOH_{socr-dhg}(s) \cdot (-1) \cdot V_{bus-ref} \cdot \left(\frac{1}{M_v} \right) \right\} \cdot G_{dvref-dhg}(z) \quad (5.20)$$

where

$G_{dvref-dhg}(z) = \frac{Z\{ZOH_{vr-dhg} \cdot F_{mr-dhg} \cdot H_{cr-dhg}\} \cdot G_{vr-dhg}(z)}{1+T_{vr-dhg}(z)}$ is the transfer function from the reference BPM output voltage V_{r-ref} to duty cycle d_r in discharge mode;

$$ZOH_{icellr-dhg}(s) = \frac{1-e^{-sT_s}}{s};$$

$ZOH_{socr-dhg}(s) = \frac{1-e^{-sT_{soc}}}{s}$; T_{soc} is the sampling period for the SOC value in the outer SOC balancing loop. Since the SOC value of a battery cell varies very slowly compared to the switching period of the power converter, the sampling rate of the outer SOC loop does not have to be very fast. $T_{soc} = 1$ second is found to be a good trade-off between the hardware resource consumption, system stability and cell balancing speed.

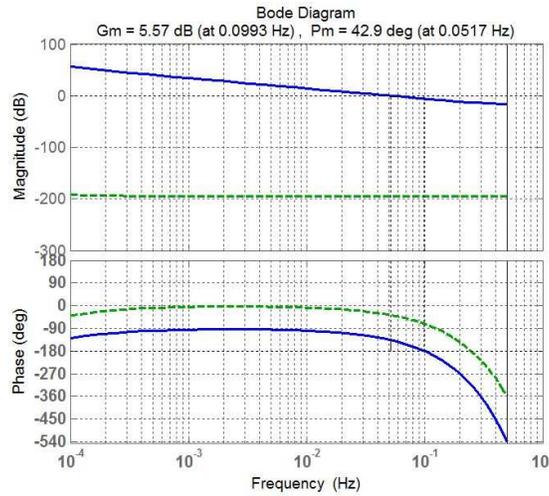


Figure. 5.4: The bode plot of uncompensated (dashed curve) and compensated (solid curve) outer SOC balancing control loop gain in discharge mode

With a compensator given by (5.21), the compensated SOC balancing loop gain achieves a control bandwidth of 0.0517Hz and phase margin of 42.9°, as shown on the solid curve in Fig. 5.4. Due to the slow sampling rate of SOC value (1Hz), it is expected that the control bandwidth of SOC balancing loop is much lower than that of inner BPM output voltage loop.

$$G_{SOCr-dhg}(z) = \frac{1700529423.7}{z-1} \quad (5.21)$$

5.3 Energy Sharing Controller Design in Constant Current Charging Mode

A. Small-Signal Model

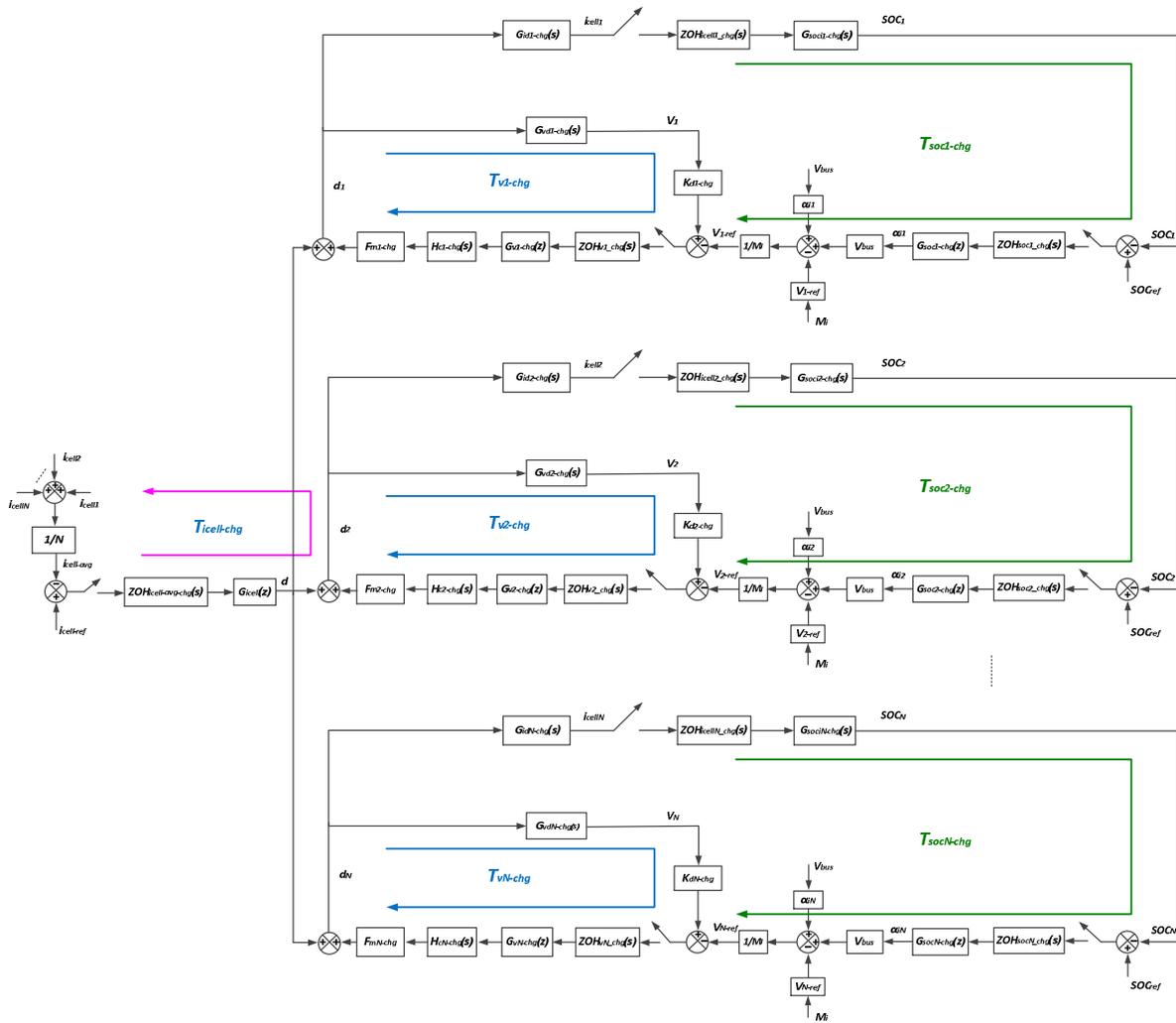


Figure 5.5: Small-signal model of the energy-sharing controlled distributed battery system in constant current charging mode

The charging operation is divided into two modes, i.e., constant current charging mode and constant voltage charging mode. This section will focus on constant current charging mode while the next section will focus on constant voltage charging mode.

Based on the basic control block diagrams shown in Fig. 4.3 and Fig. 4.4, the small-signal model for the energy sharing controlled distributed battery system in CCCM is derived as shown in Fig. 5.5. The transfer functions shown in Fig. 5.5 are described below. All the following transfer functions are for CCCM unless otherwise noted.

$T_{vr-chg}(s)$: BPM output voltage control loop gain;

$T_{socr-chg}(s)$: SOC balancing control loop gain;

$G_{vdr-chg}(s)$: duty cycle control to BPM input voltage transfer function;

$G_{idr-chg}(s)$: duty cycle control to cell current transfer function;

$G_{socir-chg}(s)$: cell current to cell SOC transfer function

$G_{vr-chg}(z)$: BPM input voltage control loop compensator;

$G_{socr-chg}(z)$: SOC balancing control loop compensator;

$K_{dr-chg}(s)$: BPM input voltage sensing gain (including the input voltage sensor gain and the analog-to-digital converter gain);

$F_{mr-chg}(s)$: PWM modulator gain;

$H_{cr-chg}(s)$: digital controller computation delay model;

$ZOH_{vr-chg}(s)$: zero order hold for BPM input voltage sampling ;

$ZOH_{icellr-chg}(s)$: zero order hold model for cell current sampling;

$ZOH_{socr-chg}(s)$: zero order hold model for cell SOC sampling.

$ZOH_{socr-chg}(s)$: zero order hold model for cell SOC sampling;

$ZOH_{i_{cell-avg-avg}}(s)$: zero order hold model for average cell current sampling.

Each BPM still consists of two independent control loops, i.e., BPM converter input voltage control loop and SOC control loop. In addition, all BPMs share an average cell current control loop. The following section presents derivation of the transfer functions associated with each control loop in CCCM.

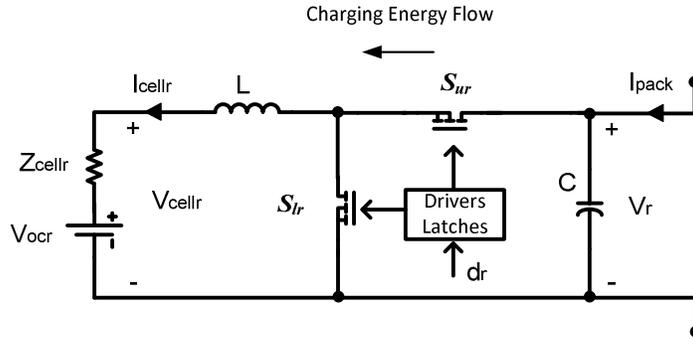


Figure. 5.6: Circuit diagram of r^{th} BPM operating as a buck converter in charge mode

B. Derivation of Transfer Functions

During charging operation, the converters operate as buck converters with the cells being the outputs as shown in Fig. 5.6. The independent state variables of each BPM converter in this case are the inductor current or cell current $i_{cell}(t)$ and the BPM input voltage $v(t)$. The input variables are cell open circuit voltage $V_{oc}(t)$ and input current or pack current $i_{pack}(t)$. The output variables are the same as the state variables.

Next, the state equations for r^{th} BPM during each subinterval are derived. When S_{ur} is on and S_{lr} is off during $d_r T_s$ time duration, the state equations are

$$\begin{cases} L \frac{di_{cellr}(t)}{dt} = v_r(t) - i_{cellr}(t) \cdot Z_{cellr} - v_{ocr}(t) \\ C \frac{dv_r(t)}{dt} = i_{pack}(t) - i_{cellr}(t) \end{cases} \quad (5.22)$$

When S_{lr} is on and S_{ur} is off during $(1-d_r)T_s$ time duration:

$$\begin{cases} L \frac{di_{cellr}(t)}{dt} = -i_{cellr}(t) \cdot Z_{cellr} - v_{ocr}(t) \\ C \frac{dv_r(t)}{dt} = i_{pack}(t) \end{cases} \quad (5.23)$$

Equations (5.22) and (5.23) can be rewritten in the following state-space form:

$$K \frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \quad (5.24)$$

$$K \frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \quad (5.25)$$

$$\text{Where } k = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}, x(t) = \begin{bmatrix} i_{cellr}(t) \\ v_r(t) \end{bmatrix}, u(t) = \begin{bmatrix} v_{ocr}(t) \\ i_{pack}(t) \end{bmatrix}, A_1 = \begin{bmatrix} -Z_{cellr} & 1 \\ -1 & 0 \end{bmatrix}, B_1 =$$

$$\begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}, A_2 = \begin{bmatrix} -Z_{cellr} & 0 \\ 0 & 0 \end{bmatrix}, \text{ and } B_2 = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$$

The next step is to evaluate the state-space averaged equilibrium equations. The averaged matrix A is

$$A = D_r A_1 + D_r' A_2 = D_r \begin{bmatrix} -Z_{cellr} & 1 \\ -1 & 0 \end{bmatrix} + D_r' \begin{bmatrix} -Z_{cellr} & 0 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} -Z_{cellr} & D_r \\ -D_r & 0 \end{bmatrix} \quad (5.26)$$

Similarly, the averaged matrix B is

$$B = D_r B_1 + D_r' B_2 = D_r \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} + D_r' \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \quad (5.27)$$

Therefore, the equilibrium state vector X is

$$X = -A^{-1} B U = - \begin{bmatrix} -Z_{cellr} & D_r \\ -D_r & 0 \end{bmatrix}^{-1} \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{ocr} \\ I_{pack} \end{bmatrix} = \begin{bmatrix} \frac{I_{pack}}{D_r} \\ \frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack} \end{bmatrix} \quad (5.28)$$

The equilibrium operating point parameters used in the charge mode are listed in Table 5.3.

Table 5.3: Equilibrium Operating Point Parameter Values in Charge Mode

Parameter	Value
V_{cellr}	3.7V
V_r	8V
V_{bus}	16V
M_i	2
$\alpha_{i1} = \alpha_{i2}$	1
Z_{cellr}	65mΩ
$I_{cell-ref}$	1.3A
I_{pack}	0.615A
D_r	0.4731
D_r'	0.5269

The vector coefficient of $\widehat{d}(t)$ is

$$(A1 - A2)X + (B1 - B2)U = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} X + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{ocr} \\ I_{pack} \end{bmatrix} = \begin{bmatrix} \frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack} \\ -\frac{I_{pack}}{D_r} \end{bmatrix} \quad (5.29)$$

The small-signal AC state equations therefore become

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \widehat{i_{cellr}}(t) \\ \widehat{v_r}(t) \end{bmatrix} = \begin{bmatrix} -Z_{cellr} & D_r \\ -D_r & 0 \end{bmatrix} \begin{bmatrix} \widehat{i_{cellr}}(t) \\ \widehat{v_r}(t) \end{bmatrix} + \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \widehat{v_{ocr}}(t) \\ \widehat{i_{pack}}(t) \end{bmatrix} + \begin{bmatrix} \frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack} \\ -\frac{I_{pack}}{D_r} \end{bmatrix} \widehat{d_r}(t) \quad (5.30)$$

When written in scalar form, (5.30) becomes

$$\begin{cases} L \frac{d\widehat{i_{cellr}}(t)}{dt} = -Z_{cellr}\widehat{i_{cellr}}(t) + D_r\widehat{v_r}(t) - \widehat{v_{ocr}}(t) \\ \quad + \left(\frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack}\right)\widehat{d_r}(t) \\ C \frac{d\widehat{v_r}(t)}{dt} = -D_r\widehat{i_{cellr}}(t) + \widehat{i_{pack}}(t) - \frac{I_{pack}}{D_r}\widehat{d_r}(t) \end{cases} \quad (5.31)$$

Again, it is assumed that $\widehat{v_{ocr}}(t)=0$ here. Then performing Laplace Transform on (5.31) yields

$$\begin{cases} SL\widehat{i_{cell}}(s) = -Z_{cellr}\widehat{i_{cell}}(s) + D_r\widehat{v_r}(s) + \left(\frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack}\right)\widehat{d_r}(s) \\ SC\widehat{v_r}(s) = -D_r\widehat{i_{cell}}(s) + \widehat{i_{pack}}(s) - \frac{I_{pack}}{D_r}\widehat{d_r}(s) \end{cases} \quad (5.32)$$

Let the AC small signal variation of another independent variable $\widehat{i_{pack}}(s) = 0$ and simplify

(5.32) yields

$$\begin{cases} SL\widehat{i_{cell}}(s) = -Z_{cellr}\widehat{i_{cell}}(s) + D_r\widehat{v_r}(s) + \left(\frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack}\right)\widehat{d_r}(s) \\ SC\widehat{v_r}(s) = -D_r\widehat{i_{cell}}(s) - \frac{I_{pack}}{D_r}\widehat{d_r}(s) \end{cases} \quad (5.33)$$

Based on (5.33), the following transfer functions can be derived,

$$G_{vdr-chg}(s) = \frac{\widehat{v_r}(s)}{\widehat{d_r}(s)} = \frac{(SL+Z_{cell})\left(-\frac{I_{pack}}{D_r}\right) - \left(\frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack}\right)}{(SL+Z_{cell})SC + D_r^2} \quad (5.34)$$

$$G_{idr-chg}(s) = \frac{\widehat{i_{cellr}}(s)}{\widehat{d_r}(s)} = \frac{-I_{pack} + SC\left(\frac{V_{ocr}}{D_r} + \frac{Z_{cellr}}{D_r^2} I_{pack}\right)}{(SL+Z_{cell})SC + D_r^2} \quad (5.35)$$

$$G_{socir-chg}(s) = \frac{SOCr(s)}{i_{cellr}(s)} = \frac{T_s}{Q} \quad (5.36)$$

C. Compensator Design

a) Voltage Loop Compensator Design

According to the small signal model shown in Fig. 5.5, the discrete-time transfer function of the converter plant in CCCM $G_{pr-chg}(z)$ includes the ZOH, the sampler, the BPM input voltage sensing gain K_{dr-chg} , the digital controller computation delay model H_{cr-chg} , in addition to the continuous-time plant $G_{vdr-chg}(s)$. $G_{pr-chg}(z)$ is given by (5.37) and its bode plot is represented by the dashed curve in Fig. 5.7.

$$G_{pr-chg}(z) = Z\{-ZOH_{vr-chg}(s) \cdot H_{cr-chg}(s) \cdot F_{mr-chg}(s) \cdot G_{vdr-chg}(s) \cdot K_{dr-chg}\} = \frac{0.0002245z^2 + 0.0006576z - 0.0005437}{z^3 - 1.99z^2 + 0.9914z} \quad (5.37)$$

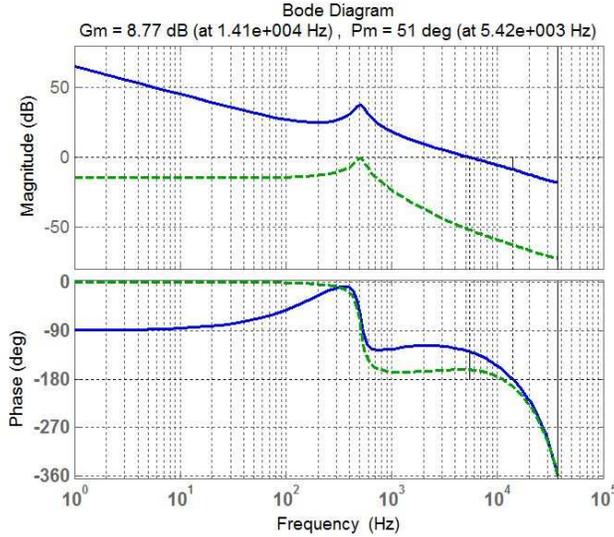


Figure.5.7: The bode plot of uncompensated (dashed curve) and compensated (solid curve) BPM input voltage control loop gain in CCCM

Unlike the voltage loop design in discharge mode where the control bandwidth is limited by the RHP zero, the target control bandwidth for the voltage loop design in CCCM can be set

higher. With a compensator given by (5.38), the BPM input voltage control loop gain ($T_{vr-chg}(z)=G_{pr-chg}(z) \cdot G_{vr-chg}(z)$) achieves a control bandwidth of 5.42 kHz and a phase margin of 51°, as shown on the solid curve in Fig. 5.7.

$$G_{vr-chg}(z) = \frac{449.9z^2 - 874.8z + 425.2}{z^2 - 1.669z + 0.6687} \quad (5.38)$$

b) SOC Balancing Loop Compensator Design

According to the small signal model shown in Fig. 5.5, the uncompensated SOC loop gain (i.e., with unity compensator gain) in CCCM is given by

$$T_{socr-chg-uncomp}(z) = Z \left\{ G_{idr-chg}(s) \cdot ZOH_{icellr-chg}(s) \cdot G_{socir-chg}(s) \cdot ZOH_{socr-chg} \cdot V_{bus} \cdot \left(\frac{1}{M_i} \right) \right\} \cdot G_{dvrefr-chg}(z) \quad (5.39)$$

where

$G_{dvrefr-chg}(z) = \frac{Z\{-ZOH_{vr-chg} \cdot F_{mr-chg} \cdot H_{cr-chg}\} \cdot G_{vr-chg}(z)}{1 + T_{vr-chg}(z)}$ is the transfer function from the reference output voltage V_{r-ref} to the duty cycle d_r for r^{th} BPM in CCCM;

$$ZOH_{icellr-chg}(s) = \frac{1 - e^{-sT_s}}{s};$$

$$ZOH_{socr-chg}(s) = \frac{1 - e^{-sT_{soc}}}{s}.$$

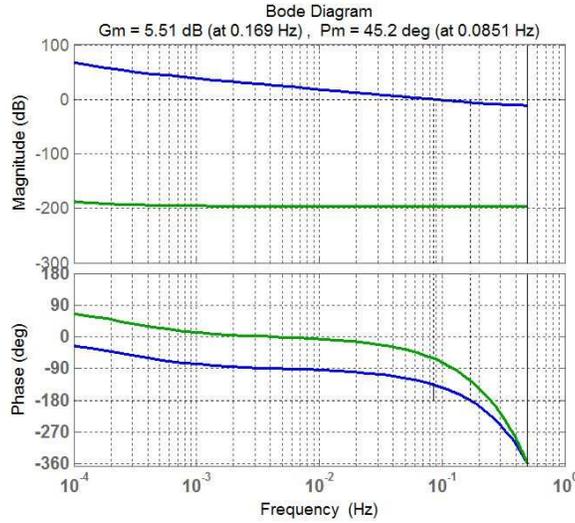


Figure. 5.8: The bode plot of uncompensated (dashed curve) and compensated (solid curve) outer SOC balancing control loop gain in constant current charging mode

With a simple integrator given by (5.40), the outer SOC balancing control loop gain achieves a control bandwidth of 0.0851 Hz and a phase margin of 45.2°, as shown on the solid curve in Fig. 5.8.

$$G_{SOCr-chg}(z) = \frac{3.379e9z-1.46e8}{z-1} \quad (5.40)$$

c) Average Cell Current Loop Compensator Design

According to the small-signal model shown in Fig. 5.5, the uncompensated average cell current control loop gain (i.e., with unity compensator gain) for a two-BPM system (used in the experimental prototype) is given by (5.41) and represented by dashed curve in Fig. 5.9.

$$T_{icell-chg-uncomp}(z) = Z \left\{ \frac{1}{2} \left(G_{icell d1-chg}(s) + G_{icell d2-chg}(s) \right) \cdot ZOH_{icell-avg-chg}(s) \right\} =$$

$$\frac{1.059z^3 - 3.171z^2 + 3.167z - 1.055}{z^4 - 3.979z^3 + 5.941z^2 - 3.945z + 0.9828} \quad (5.41)$$

where $ZOH_{icell-avg-chg}(s) = \frac{1-e^{-sT_s}}{s}$

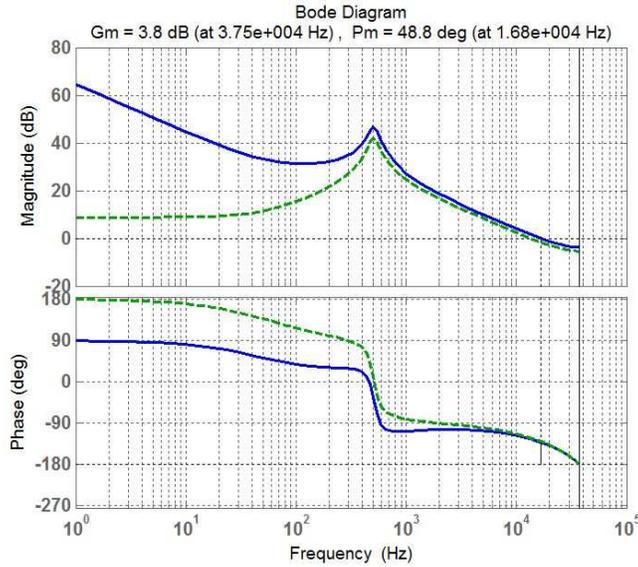


Figure.5.9: The bode plot of uncompensated (dashed curve) and compensated (solid curve) average cell current control loop gain

With a compensator given by (5.42), the average cell current control loop gain achieves a control bandwidth of 16.8 kHz and a phase margin of 48.8° as shown on the solid curve in Fig. 5.9.

$$G_{icell}(z) = \frac{1.236z - 1.184}{z - 1} \quad (5.42)$$

5.4 Energy Sharing Controller Design in Constant Voltage Charging Mode

A. Small-Signal Model

Based on the basic control block diagram shown in Fig. 4.5, the small-signal model for the energy sharing controlled distributed battery system in constant voltage charging mode can be derived as shown in Fig. 5.10. The transfer functions shown in Fig. 5.10 are described below. All the following transfer functions are for CCCM unless otherwise noted.

$T_{vcell-cvcm}(z)$: average cell current control loop gain;

$G_{vcellrd-chg}(s)$: duty cycle control d to cell voltage v_{cellr} transfer function for r^{th} BPM;

$G_{vcell}(z)$: average cell voltage control loop compensator;

$ZOH_{vcell-avg-chg}(s)$: zero order hold model for average cell voltage sampling.

The control structure in this mode is relatively simple and consists of only a single control loop, i.e., average cell voltage control loop $T_{vcell-cvcm}$, in order to regulate the average cell voltage at the desired level.

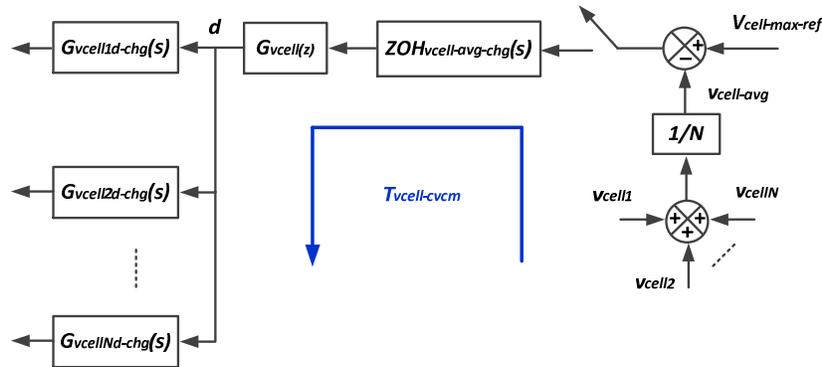


Figure. 5.10: Small-signal model of the energy-sharing controlled distributed battery system in

CVCM

B. Derivation of Transfer Function

$$G_{vcellrd-chg}(s) = \frac{vcellr(s)}{d(s)} = \frac{icellr(s)}{d(s)} Z_{cellr} = \frac{-I_{pack} + SC \left(\frac{V_{ocr}}{D} + \frac{Z_{cellr} I_{pack}}{D^2} \right)}{(SL + Z_{cellr})SC + D^2} Z_{cellr} \quad (5.43)$$

C. Average Cell Voltage Loop Compensator Design

According to the small-signal model shown in Fig. 5.10, the uncompensated average cell voltage control loop gain (i.e, with unity compensator gain) for a two-BPM system is given by (5.44) and represented by the dashed curve in Fig. 5.11.

$$T_{vcell-cvcm-uncomp}(z) = Z \left\{ \frac{1}{2} \left(G_{vcell1d-chg}(s) + G_{vcell2d-chg}(s) \right) \cdot ZOH_{vcell-avg-chg}(s) \right\} = \frac{0.06885z^3 - 0.2061z^2 + 0.2059z - 0.06857}{z^4 - 3.979z^3 + 5.941z^2 - 3.945z + 0.9828} \quad (5.44)$$

where $ZOH_{vcell-avg-chg}(s) = \frac{1 - e^{-sT_s}}{s}$.

With a compensator given by (5.45), the average cell voltage control loop gain achieves a control bandwidth of 16.8 kHz and phase margin of 48.8°.

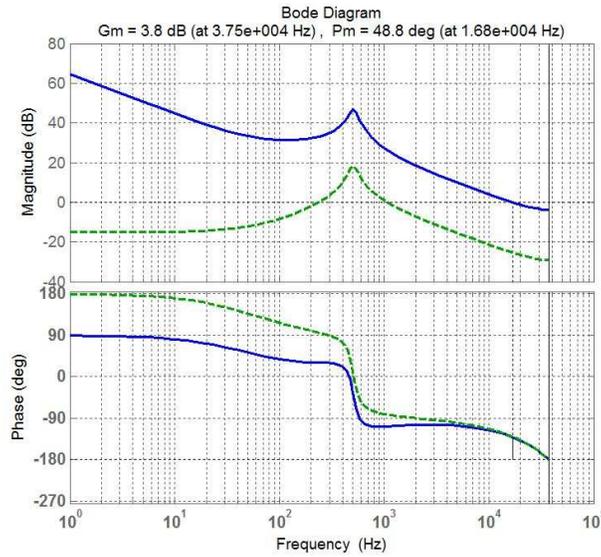


Figure. 5.11: The bode plot of uncompensated (dashed curve) and compensated (solid curve) average cell voltage control loop gain

$$G_{vcell}(z) = \frac{19.02z-18.22}{z-1} \quad (5.45)$$

5.5 Simulation and Experimental Model Validation

The derived small-signal models and designed compensators for different operating modes are validated using both simulation model and experimental prototype results. The simulation model (based on the derived transfer functions used in a mathematical block diagram based system model) built in MATLAB®/SIMULIK software package. The designed compensators for different control loops are implemented by using TMS320S28335 microcontroller and tested on a two-cell distributed battery system prototype. The design parameters of the simulation model and experimental prototype are the same and they are as listed in Table 5.2. The simulation and experimental results are shown in Fig. 5.12 through Fig. 5.13 for discharging operation and in Fig. 5.14 through Fig. 5.15 for charging operation.

It might be of importance to note that the MATLAB®/SIMULIK simulation model utilizes the derived small-signal transfer functions equations and compensators obtained in this paper. Therefore, if the resulted system dynamic responses from the experimental hardware match the dynamic responses obtained from the MATLAB®/SIMULIK simulation model, this implies that the developed small-signal model and compensators in this paper are valid.

The performance of the inner BPM output voltage control loop is first tested by disabling the SOC control loop in the discharge mode. The voltage loop multipliers (α_{v1} and α_{v2}) are initially set to be equal to 1 which results in $V_{1-ref} = V_{2-ref} = 8V$. Then the voltage loop multiplier values are varied against each other with α_{v1} being initially set to the minimum value 0 while α_{v2} is initially set to the maximum value 2. This leads to $V_{1-ref} = 6V$ and $V_{2-ref} = 10V$. As shown in Fig. 5.12, the simulation model results and the experimental results for each BPM output voltage

agree well with each other, i.e., they have the same response behavior such as shape, magnitude, and timing.

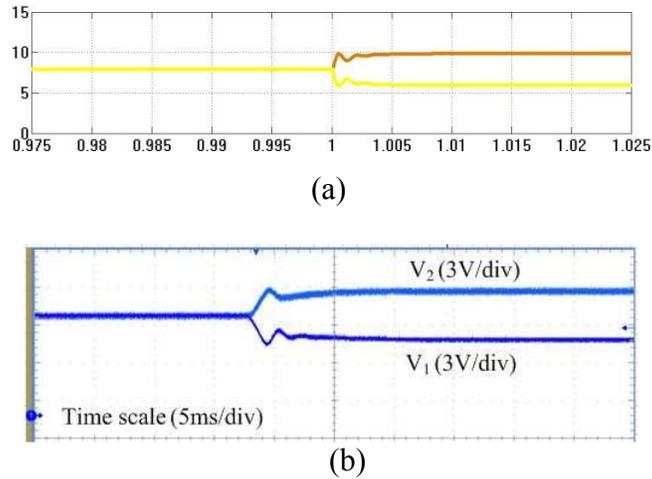


Figure 5.12: (a) Simulation model waveforms (top trace: V_2 ; bottom trace: V_1 ; horizontal axis unit: second; vertical axis unit: volt) and (b) experimental waveforms for the BPM output voltages when V_{1-ref} is changed from 8V to 6V while V_{2-ref} is changed from 8V to 10V

Then, the dynamics of the outer SOC control loop is tested in discharge mode (in this test, all loops including SOC balancing loop are enabled and are functional). The SOC value of the cell by nature changes very slowly under normal discharge rates (0.5C-2C) and as specified by the manufacturer of the battery cells. Therefore the SOC value of cell1 is intentionally and manually varied/stepped by 5% (80% to 75% in this case) in order to create a fast transient condition of SOC for testing purpose (This is done by stepping the estimated SOC value by the microcontroller by 5%). As the SOC value of cell1 is reduced to be lower than that of cell2, the SOC control loop automatically sets the voltage loop multiplier of BPM2 to be higher than that of BPM1 in order to discharge BPM2 faster than BPM1. As shown in Fig. 5.13, the output voltage of BPM2 is regulated by the closed-loop system at the maximum value while that of

BPM1 is regulated at the minimum value. The simulation model results also agree well with the experimental results as can be observed from Fig. 5.13.

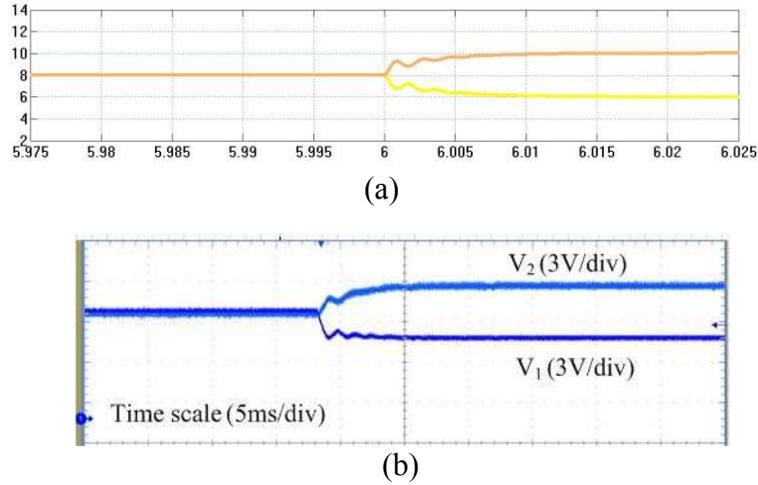


Fig. 5.13. (a) Simulation model waveforms (top trace: V_2 ; bottom trace: V_1 ; horizontal axis unit: second; vertical axis unit: volt) and (b) experimental waveforms for the BPM output voltages when $SOC1$ is suddenly changed from 80% to 75% under cell balanced condition where $SOC1 = SOC2 = 80\%$

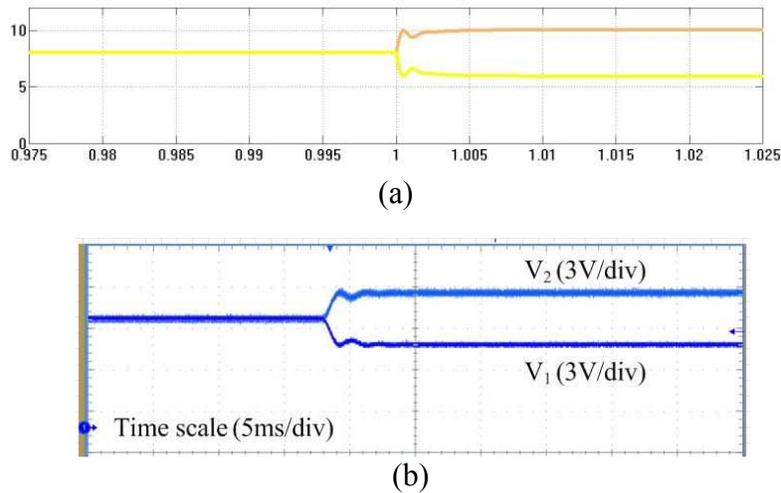
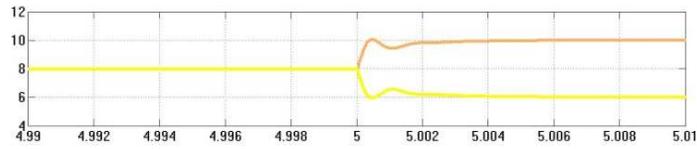
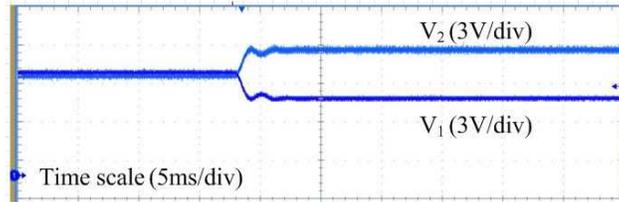


Figure. 5.14: (a) Simulation model waveforms (top trace: V_2 ; bottom trace: V_1 ; horizontal axis unit: second; vertical axis unit: volt) and (b) experimental waveforms for the BPM output voltages when V_{1-ref} is changed from 8V to 6V while V_{2-ref} is changed from 8V to 10V



(a)



(b)

Figure. 5.15: (a) Simulation model waveforms (top trace: V_2 ; bottom trace: V_1 ; horizontal axis unit: second; vertical axis unit: volt) and (b) experimental waveforms for the BPM output voltages when SOC_1 is suddenly changed from 80% to 85% under cell balanced condition where

$$SOC_1 = SOC_2 = 80\%$$

For the model and control verification during charging operation, similar test procedures are performed as for the discharge mode. The only difference in the testing condition is that for the charging operation, the SOC value of cell1 is manually varied/stepped in the opposite direction from 80% to 85% in order to create the fast transient condition of SOC for testing the dynamics of the SOC balancing control loop. The waveforms shown in Fig. 5.14 and Fig. 5.15 demonstrate the consistency between the simulation model and experimental results.

5.6 Summary

State-space averaging small-signal modeling and analysis is performed in this chapter in order to gain deeper insights into the dynamics of the energy sharing controlled distributed battery system and facilitate the design of the energy sharing controller. Based on the derived small-signal models and associated transfer functions, all of the control loops are compensated under each operation mode including discharge mode, constant current charging mode and constant

voltage charging mode by using rule-of-thumb frequency-domain design guidelines and criteria, such as control bandwidth and stability margins. The derived models and compensators design are validated by both simulations and experiments on a two-cell distributed battery system prototype.

CHAPTER 6

POWER MULTIPLEXED CONTROLLER FOR SIMO CONVERTERS

6.1 Introduction

Multiple independently regulated voltage rails are required in many increasingly complex yet reliable power distribution systems such as those used in battery-powered electronic devices, telecommunication and data communication equipments, system on-chip integrated circuits, and industrial infrastructures, among others [35-39, 98-112]. Especially in the past decade, a wide variety of portable devices, such as Smartphones, Tablets and Ultrabooks, have achieved widespread adoption worldwide. In such portable devices, a power management integrated circuit (PMIC) is usually employed to deliver different tightly regulated supply voltages from a single battery power source to various loads, including application/baseband processors, memory, WiFi/bluetooth modules, radio frequency (RF) power amplifiers and liquid crystal display (LCD) module, among others [35-39]. With more functional circuitries/modules being integrated into an increasingly smaller motherboard and System-On-Chips (SOCs), the performance specifications of the PMIC, including footprint, cost and efficiency, are becoming increasingly stringent. Improved PMIC performance can help extend the battery life in addition to saving more motherboard real estate which allows for using larger-size battery with higher capacity.

The PMIC is usually comprised of multiple switching DC-DC power converters that are driven by a single battery cell. These switching converters should operate independently without interference and cross regulation between one another. Single-inductor multiple-output (SIMO)

switching converter is a cost-effective alternative solution to the multiple individual switching converters architecture. By using only a single power inductor and/or less power switching devices, SIMO converter can potentially lead to reduced size, cost, component count in addition to eliminating mutual coupling between the power inductors which are closely integrated on a high-density board or chip [35-39]. However, due to the fact that the multiple output voltage rails are coupled to the same switching node in a SIMO converter, the cross regulation between the outputs can severely degrade the output voltage regulation performance during steady-state and dynamic operations and may even cause system instability in a worst case scenario.

This cross regulation effect has been extensively studied in the literature as in [35-39, 98-106] and a number of control schemes have been proposed aiming to address this issue. For example, in [35], a time-multiplexed control scheme is proposed to suppress the cross regulation between the outputs in boost or buck-boost derived SIMO converter operating in discontinuous conduction mode (DCM). This control scheme, however, is not well suited for the buck-derived SIMO converter where the switches are located at the input side instead of the output. Moreover, the controller presented in [35] is only suitable for DCM operation. When the SIMO converter enters continuous conduction mode (CCM) at heavy loads, this controller is no longer effective because the variation of the voltage/current in one output will directly affect the amount of energy delivered to other outputs, thus causing cross regulation. To suppress the cross regulation of the SIMO converter in CCM, a modified control scheme is proposed in [36] where a dc offset current is introduced in order to initialize the inductor current to the same value at the beginning of each switching cycle. This concept results in reduced cross regulation in CCM while maintaining low inductor current and output voltage ripples for higher efficiency and lower switching noise. The downside of this concept, however, is that it requires an extra freewheel

switch and current sensing circuitries in addition to a sophisticated technique to determine the optimal dc offset current value under different load current conditions. In [37], a predictive digital current mode controller is proposed, where the duty cycle value for each switch in the SIMO converter is calculated based on the current reference value and the estimated inductor current. While resulting in reduced cross regulation, this controller requires fairly high computational capabilities and resources. A state feedback control mechanism is presented in [38] where the state information of each output is fed to the control loops of other outputs. Although reduced cross regulation is achieved at small load transients, the complexity of the control architecture is expected to increase exponentially as the number of outputs increases. Also, the performance of the controller is sensitive to the variations of the converter parameters.

In summary, the main challenges associated with the SIMO converter still persist. Motivated by this fact, this work proposes a new control scheme called power-multiplexed control (PM control). By operating the output switches at a lower frequency than the power stage switches, each output is independently regulated when the corresponding output switch is turned on. This control scheme completely eliminates the cross regulation between the outputs under both steady-state and dynamic operations.

The remainder of this chapter is organized as follows: Section II describes the architecture of the SIMO topology and the basic operation principle of the PM control scheme. Section III presents the steady-state operation analysis of the PM controlled SIMO converter during both DCM and CCM operations. Experimental results are presented and discussed in Section IV. Section V summarizes this chapter.

6.2 SIMO Topology with The PM Control Scheme

While the proposed control scheme is applicable to different multi-output architectures that are derived from conventional converter topologies including buck, boost, and buck-boost converters [10-15], buck-derived SIMO converter is used in this work to illustrate and verify the proposed concept.

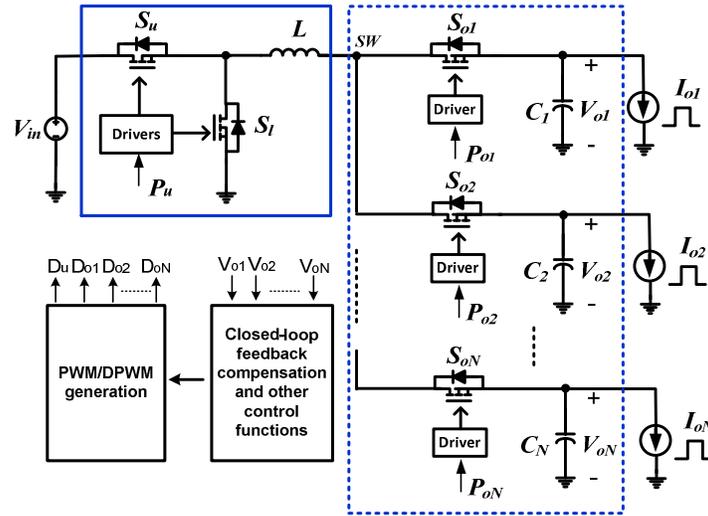


Figure. 6.1: Illustration of the N-output buck-derived SIMO converter

Fig. 6.1 illustrates the PM controlled N-output SIMO converter which consists of two stages. The front stage (input power stage), as highlighted in the solid box, is the same as the conventional buck converter with two switches (S_u and S_l) and one power inductor (L) but without the output capacitor. The output stage, as highlighted in the dotted box, is composed of N outputs coupled to the same switching node, SW , through N output switches (S_{o1} through S_{oN}) that can be turned on/off to enable/disable the corresponding output. Each channel can operate at different output voltage, different load current, different switching frequency and different modes of operation (CCM or DCM). The addition of an output would require only a switch with associated gate driver in addition to an output capacitor.

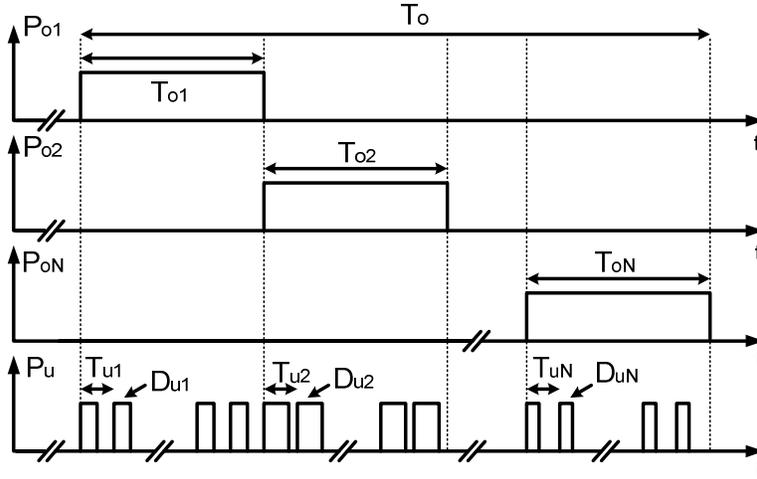


Figure. 6.2: Ideal timing diagram of the N -output SIMO converter with the proposed PM control scheme during steady-state operation

The main ideal timing diagram of the SIMO converter with the proposed PM control scheme is illustrated in Fig. 6.2. The switching frequency (f_s) of the input power stage switches, S_u and S_l , are equal and is set higher than the switching frequency (f_o) of the output switches, S_{o1} , S_{o2} , ..., S_{oN} . It is essential in the proposed PM control scheme to synchronize the rising edge of the gate driving signal for the output switches with that of the high-side input power switch, S_u , in order to completely decouple the operation of the multiple outputs. Output switches, S_{o1} , S_{o2} , ..., S_{oN} , are turned on one at a time for a certain period of time over a complete switching cycle of the output switches ($T_o=1/f_o$ in Fig. 6.2). During the on-time of each output switch (T_{o1} , T_{o2} , ... or T_{oN}), the power switch S_u has a distinct duty cycle value D_{ur} , where $r=1, 2, \dots, N$. In other words, when the output switch S_{o1} is turned on, the switch S_u operates with a duty cycle value D_{u1} , when the output switch S_{o2} is turned on, the switch S_u operates with a duty cycle value D_{u2} , and so on for other output switches. D_{u1} is set by the closed-loop feedback controller to achieve a regulated output voltage V_{o1} for load one, D_{u2} is set to achieve a regulated output voltage V_{o2} for load two, ..., and D_{uN} is set to achieve a regulated output voltage V_{oN} for load N . Switch S_u and S_l

operate in a complementary manner in CCM, while in DCM, S_l is turned on after S_u is turned off until the inductor current decreases to zero.

6.3 Steady-State Analysis of The SIMO Topology with PM Control Scheme Under Various Operation Modes

For simplicity, a two-output SIMO buck converter is utilized in this section to illustrate the operation of the PM control scheme. The principle of operation can easily be extended to SIMO converters with higher number of outputs ($N > 2$). Moreover, all the components of the SIMO converter are assumed to be ideal, which means all of the parasitic components, including DC resistance (DCR) of the inductor, equivalent series resistance (ESR) of the capacitor, and PCB traces parasitic resistance and inductance, are neglected. Based on the operation modes of the two channels, this section is divided into three subsections which respectively covers the operation of the PM controller when the two channels both operate in DCM, when the two channels both operate in CCM and when one channel operates in DCM while the other operates in CCM.

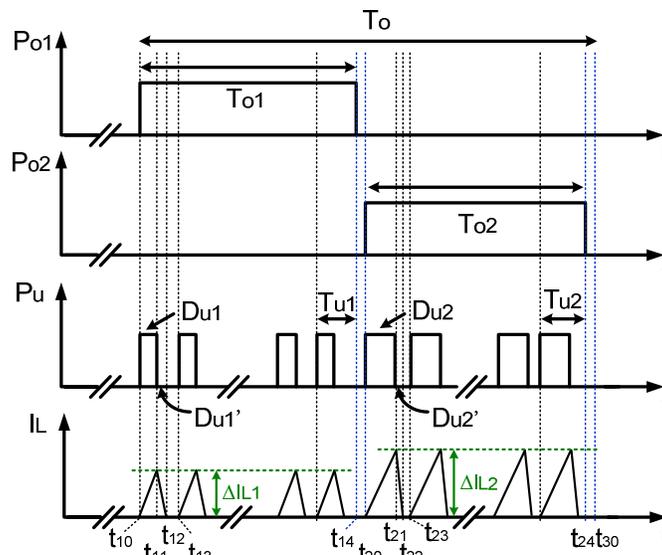


Figure. 6.3: Main theoretical operation waveforms of the PM controlled SIMO converter with the two channels both operating in DCM

A. Output Channels Both Operate in DCM

Fig. 6.3 illustrates the main theoretical operation waveforms of the PM controlled SIMO converter when the two channels both operate in DCM (when the output load current values are below a critical current value of the power inductor). To avoid shoot-through of the two outputs, a short period of dead time, T_d , (i.e., $t_{14}-t_{20}$ and $t_{24}-t_{30}$ in Fig. 6.3) is needed during the commutation of the two output switches. Therefore, a complete switching cycle (T_o) of the output switches is given by (6.1)

$$T_o = T_{o1} + T_{o2} + 2T_d \quad (6.1)$$

where T_{o1} and T_{o2} are the on-times of the output switch S_{o1} and S_{o2} during a complete switching cycle T_o , respectively.

As illustrated in Fig. 6.3, the inductor current is discharged to zero by the end of each switching cycle of the input switches (i.e., T_{u1} and T_{u2}) during DCM operation. The inductor current starts to increase from zero when the output switch S_{o1} and S_{o2} are turned on at $t = t_{10}$ and $t = t_{20}$, respectively. In other words, the inductor energy accumulated during the on-time of one output switch is fully released before the other output channel conducts, which leads to decoupled operations of the two channels. As a result, the PM controlled SIMO converter can be seen as equivalent to two independent single-output converters, and therefore, the conventional closed-loop feedback controller design guidelines for single-output converter can be applied to the closed-loop design of SIMO converter. Sophisticated control laws to decouple the operation of the outputs are not required.

Fig. 6.4 illustrates the equivalent circuits for the main intervals of operation of the PM controlled SIMO converter in different operation modes (CCM and/or DCM). The operation modes in which a specific equivalent circuit is valid are noted inside the bracket below the circuit.

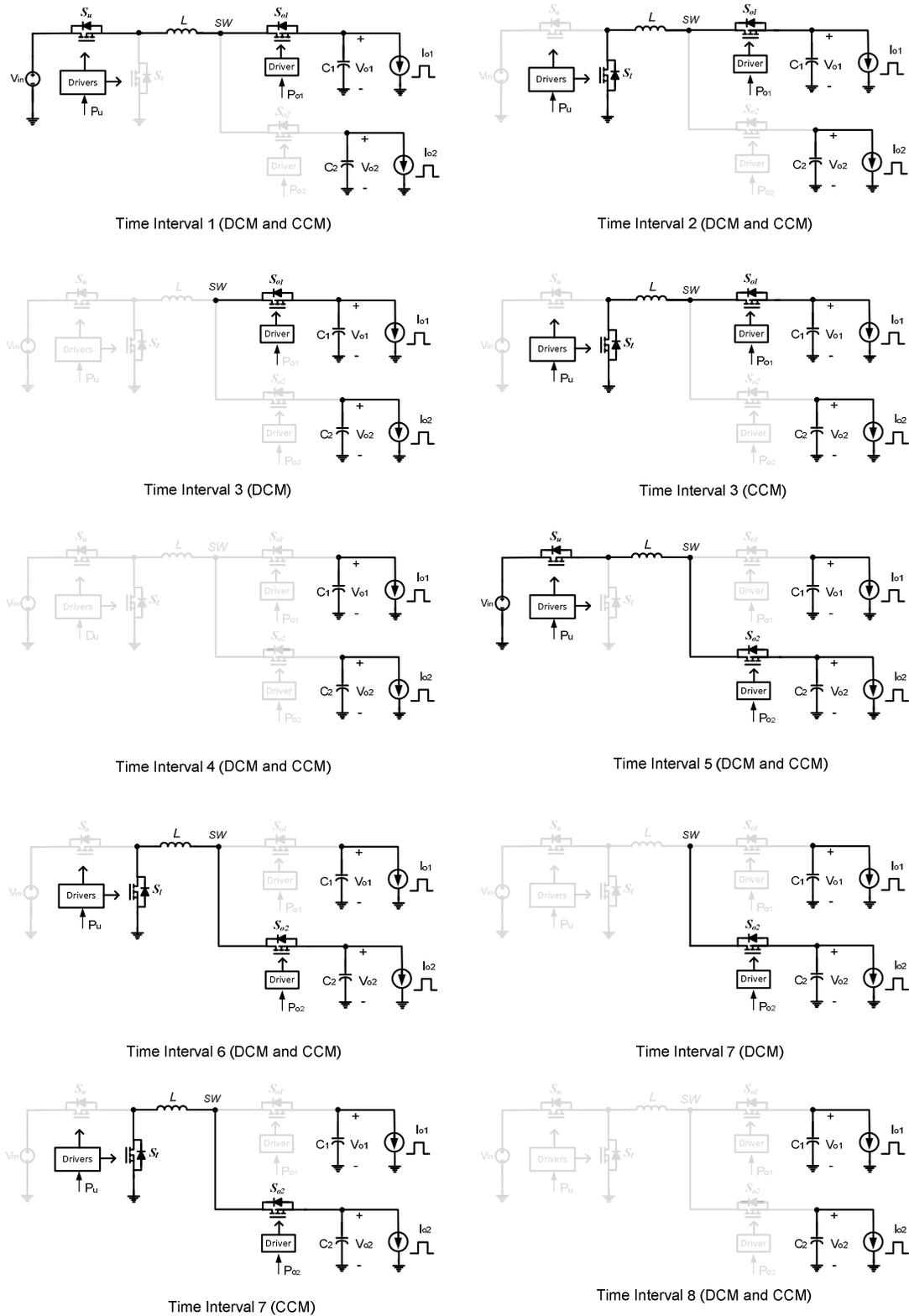


Figure.6.4: Equivalent circuits for the main intervals/modes of operation of the PM controlled SIMO under various operation modes

The description for each DCM interval of operation during a complete switching cycle (T_o) of the output switches are summarized as follows:

Time Interval 1 ($t_{10}\sim t_{11}$): during this time interval, the output switch S_{o1} is turned on while the output switch S_{o2} is turned off. Meanwhile, switch S_u is turned on while S_l is turned off. The input voltage source charges the inductor and causes the inductor current to increase. The relationship between the input voltage V_{in} , output voltage V_{o1} , the change in the inductor current ΔI_{L1} , and the charging time is given by (6.2). In the meantime, the output capacitor C_{o2} supplies energy to the load two.

$$\frac{\Delta I_{L1}}{t_{11} - t_{10}} = \frac{V_{in} - V_{o1}}{L} \quad (6.2)$$

Time Interval 2 ($t_{11}\sim t_{12}$): during this time interval, the output switch S_{o1} continues to be turned on while the output switch S_{o2} continues to be turned off. Meanwhile, switch S_u is turned off while S_l is turned on. The inductor is discharged to zero while delivering energy to the load one. The relationship between the output voltage V_{o1} , the change in the inductor current ΔI_{L1} , and the discharging time is given by (6.3). In the meantime, the output capacitor C_{o2} still supplies energy to the load two.

$$\frac{\Delta I_{L1}}{t_{12} - t_{11}} = \frac{V_{o1}}{L} \quad (6.3)$$

Time Interval 3 ($t_{12}\sim t_{13}$): during this time interval, the output switch S_{o1} continues to be turned on while the output switch S_{o2} continues to be turned off. Meanwhile, both switch S_u and S_l are turned off. The inductor current value remains at zero. The output capacitor C_{o1} supplies energy to the load one while the output capacitor C_{o2} supplies energy to the load two.

Applying the voltage-second balance theory to the inductor and capacitor charge balance theory to the output capacitor one yields (6.4) and (6.5), respectively.

$$\frac{V_{o1}}{V_{in}} = \frac{D_{u1}}{D_{u1} + D_{u1}'} \quad (6.4)$$

$$I_{L1} = \frac{D_{u1}(D_{u1} + D_{u1}')(V_{in} - V_o)D_{u1}T_{u1}}{2L} \quad (6.5)$$

where D_{u1}' is equal to the time the inductor current takes to discharge to zero divided by the switching cycle of switch S_u ; I_{L1} is the average inductor current during on-time of the output switch S_{o1} , and it is also given by (6.6) because the inductor current is effectively zero for channel one when the output switch S_{o1} is turned off while S_{o2} is turned on.

$$I_{L1} = \frac{I_{o1}T_o}{T_{o1}} = \frac{V_{o1}T_o}{R_{o1}T_{o1}} \quad (6.6)$$

where R_{o1} is the load resistance for output one and I_{o1} is the load current for output one. Based on (6.4), (6.5) and (6.6), the DC voltage gain for the channel one can be derived as given by

$$\frac{V_{o1}}{V_{in}} = \frac{2}{1 + \sqrt{1 + 4K_1/D_{u1}^2}} \quad (6.7)$$

where $K_1 = 2LT_o/(R_{o1}T_{u1}T_{o1})$, and D_{u1} is the duty cycle value of switch S_u when the output switch S_{o1} is turned on.

Time Interval 4 ($t_{14} \sim t_{20}$): during this short dead-time period, the input switches S_u and S_l are both turned off and the output switches S_{o1} and S_{o2} are turned off as well. Unlike the synchronous rectifier in the front power stage of the SIMO converter, the body diodes of the two output switches S_{o1} and S_{o2} cannot conduct during this dead-time period to provide a path for the inductor current to flow. Therefore, it is critical to ensure that the inductor current returns to zero before the dead-time period starts in order to avoid a voltage spike on the output switching node SW. DCM operation certainly meets this requirement as the inductor current returns to zero by

the end of each switching cycle of input switches. During this interval, output capacitor C_{o1} and output capacitor C_{o2} supply energy to the load one and the load two, respectively.

The operation of the PM controlled SIMO converter during *Time Interval 5* ($t_{20}\sim t_{21}$), *6* ($t_{21}\sim t_{22}$), *7* ($t_{22}\sim t_{23}$) and *8* ($t_{24}\sim t_{30}$) are similar to that during *Time Interval 1* ($t_{10}\sim t_{11}$), *2* ($t_{11}\sim t_{12}$), *3* ($t_{13}\sim t_{14}$) and *4* ($t_{14}\sim t_{20}$), respectively. Therefore, the DC voltage gain for the channel 2 in this case can similarly be derived as given by.

$$\frac{V_{o2}}{V_{in}} = \frac{2}{1 + \sqrt{1 + 4K_2/D_{u2}^2}} \quad (6.8)$$

where $K_2=2LT_o/(R_{o2}T_{u2}T_{o2})$, R_{o2} is the load resistance for output channel two, and D_{u2} is the duty cycle value of switch S_u when the output switch S_{o2} is turned on.

B. Output Channels Both Operate in CCM

Fig. 6.5 illustrates the main theoretical steady-state waveforms of the PM controlled SIMO converter when the two channels both operate in CCM. The basic PM control scheme discussed in Section III-A cannot directly be applied to CCM operation without modifications. Unlike in DCM, the inductor current during CCM operation is not discharged to zero by the end of each switching cycle of input switches. If the same PM control scheme used in DCM were applied in CCM, the output switching node, SW, would experience undesired voltage spikes during the dead-time periods (i.e., $t_{14}\sim t_{20}$ and $t_{24}\sim t_{30}$ in Fig. 6.5) because the inductor current has no path to flow and is forced to drop to zero abruptly (to be discontinued). Therefore, an inductor current reset technique is proposed and specifically employed in CCM to address this issue. The basic idea is to fully discharge the inductor current to zero during the inductor current reset time period T_{rs} (i.e., $t_{13}\sim t_{14}$ and $t_{23}\sim t_{24}$ in Fig. 6.5) before the other output channel conducts. By employing this inductor current reset technique, the operations of the two channels become

independent from one another. Consequently, the SIMO converter in CCM can also be seen as equivalent to two independent single-output converters.

Fig. 6.4 also includes the equivalent circuits for the main intervals of operation of the PM controlled SIMO converter when the two channels both operating in CCM. The description for each main interval of operation is summarized as follows:

Time Interval 1 (t_{10} – t_{11}): during this time interval, the output switch S_{o1} is turned on while the output switch S_{o2} is turned off. Meanwhile, switch S_u is turned on while S_l is turned off. The input voltage source is charging the inductor and causes the inductor current to ramp up. The relationship between the input voltage V_{in} , output voltage V_{o1} , the change in the inductor current ΔI_{L1} , and the charging time is given by (6.9). Meanwhile, the output capacitor C_{o2} supplies energy to the load two.

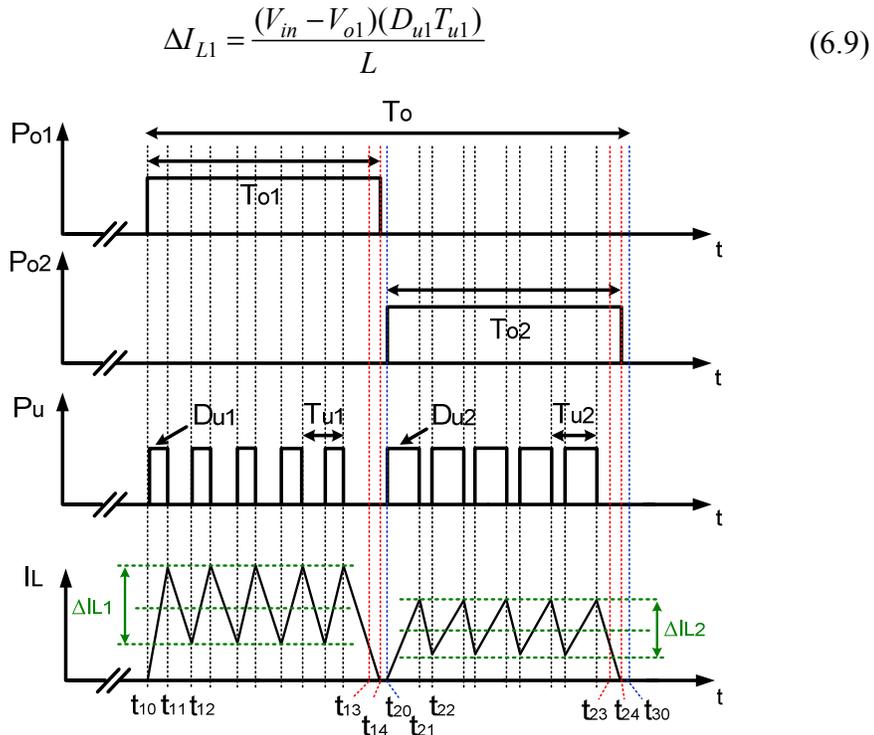


Figure.6. 5: Main theoretical operation waveforms of the PM controlled SIMO converter with the two channels both operating in CCM

Time Interval 2 ($t_{11}\sim t_{12}$): In this mode, the output switch S_{o1} continues to be turned on and the output switch S_{o2} continues to be turned off. Meanwhile, switch S_u is turned off while S_l is turned on. The inductor is discharged while delivering energy to the load one. The relationship between the output voltage V_{o1} , the change in the inductor current ΔI_{L1} , and the discharge time is given by (6.10). The output capacitor C_{o2} continues to supply energy to the load two. Based on (6.9) and (6.10), the DC voltage gain for the channel one is given by (6.11)

$$\Delta I_{L1} = \frac{V_{o1}(1-D_{u1})T_{u1}}{L} \quad (6.10)$$

$$\frac{V_{o1}}{V_{in}} = D_{u1} \quad (6.11)$$

Time Interval 3 ($t_{13}\sim t_{14}$): during this time interval, the inductor current is being reset. The output switch S_{o1} continues to be turned on while the output switch S_{o2} continues to be turned off. Switch S_u continues to be turned off and S_l continues to be turned on. Output capacitor C_{o2} continues to supply energy to the load two. The inductor continues to discharge with a slew rate of V_{o1}/L .

The optimal inductor current reset time for channel one $T_{rs_ch1_opt}$ occurs when the inductor current reaches zero right before the dead-time period starts at $t=t_{14}$, as shown in Fig. 6.5. Therefore, $T_{rs_ch1_opt}$ is given by

$$T_{rs_ch1_opt} = \frac{(I_{L1} - \Delta I_{L1}/2)L}{V_{o1}} \quad (6.12)$$

Substituting (6.6) and (6.10) into (6.12) yields

$$T_{rs_ch1_opt} = \frac{\left(\frac{V_{o1}T_o}{R_{o1}T_{o1}} - \frac{V_{o1}(1-D_{u1})T_{u1}}{2L}\right)L}{V_{o1}} \quad (6.13)$$

Generalizing (6.13) for any other channel yields

$$T_{rs_chr_opt} = \frac{\left(\frac{V_{or}T_o}{R_{or}T_{or}} - \frac{V_{or}(1-D_{ur})T_{ur}}{2L} \right) L}{V_{or}} \quad (6.14)$$

where $r = 1, 2, \dots, N$.

The inductor current reset time T_{rs} should satisfy $T_{rs} \geq T_{rs_chr_opt}$ in order to eliminate the voltage spike on the output switching node, SW, where multiple outputs are coupled.

Time Interval 4 ($t_{14} \sim t_{20}$): during this dead-time period, the input switches S_u and S_l are turned off while the output switches S_{o1} and S_{o2} are also turned off. Output capacitor C_{o1} and output capacitor C_{o2} supply energy to the load one and the load two, respectively.

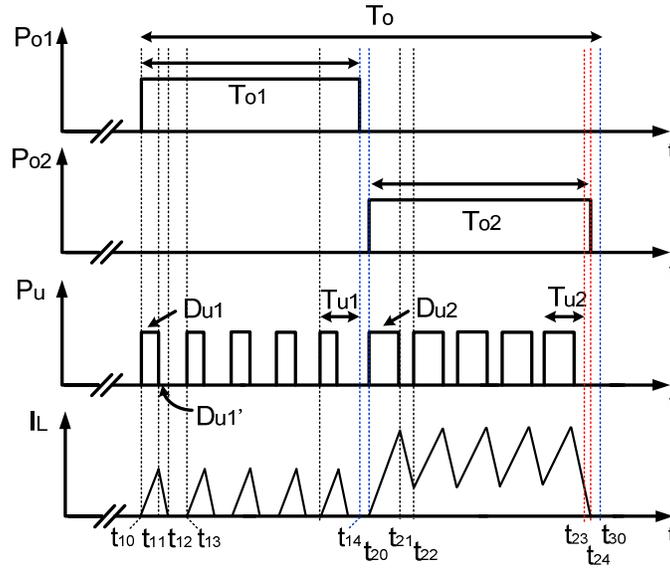


Figure. 6.6: Main theoretical operation waveforms of the PM controlled SIMO converter with the channel one operating in DCM and the channel two operating CCM

Time Interval 5 ($t_{20} \sim t_{21}$), 6 ($t_{21} \sim t_{22}$), 7 ($t_{23} \sim t_{24}$) and 8 ($t_{24} \sim t_{30}$): The operation of the PM controlled SIMO converter during these time intervals are similar to that during *Time Interval 5* ($t_{10} \sim t_{11}$), 6 ($t_{11} \sim t_{12}$), 7 ($t_{13} \sim t_{14}$) and 8 ($t_{14} \sim t_{20}$), respectively. Therefore, the DC voltage gain for the channel two can similarly be derived as given by

$$\frac{V_{o2}}{V_{in}} = D_{u2} \quad (6.15)$$

C. Output Channels Operate in Different Modes

The proposed PM controller and the inductor current reset technique are also effective when the two channels operate in different modes. Fig. 6.6 provides the main theoretical steady-state waveforms of the PM controlled SIMO converter with the channel one operating in DCM and the channel two operating in CCM. The operation of the channel one is the same as that discussed in Section III-A while the operation of the channel two is the same as discussed in Section III-B. It should be noted that T_{rs} is only required when a channel operates in CCM.

6.4 Proof-Of-Concept Experimental Prototype Results

A PM controlled two-output SIMO buck converter prototype is built in the laboratory in order to verify and evaluate the operation of the proposed concept. This proof-of-concept experimental prototype is designed with the specifications listed in Table 6.1. Based on the design specifications, the critical load current for channel one is calculated to be 1.094 A when $V_{o1} = 1.5$ V while the critical load current for channel two is calculated to be 0.833 A when $V_{o2} = 1$ V.

Table 6.1. Design Specifications of SIMO Converter

Parameter	Value
V_{in}	5 V
V_{o1}	1.5 V
V_{o2}	1 V
I_{o1}	2 A (max)
I_{o2}	2 A (max)
L	800 nH
f_s	300 kHz
f_o	15 kHz
T_d	120 ns
T_{rs}	3.33 μ s

A conventional digital Proportional-Integral (PI) compensator is used to regulate the output voltage of each channel. This PI compensator is designed to work well in both DCM and CCM based on the rule-of-thumb frequency-domain controller design guidelines. The digital PI compensator is implemented by using the microcontroller (TMS320F28335) from TI.

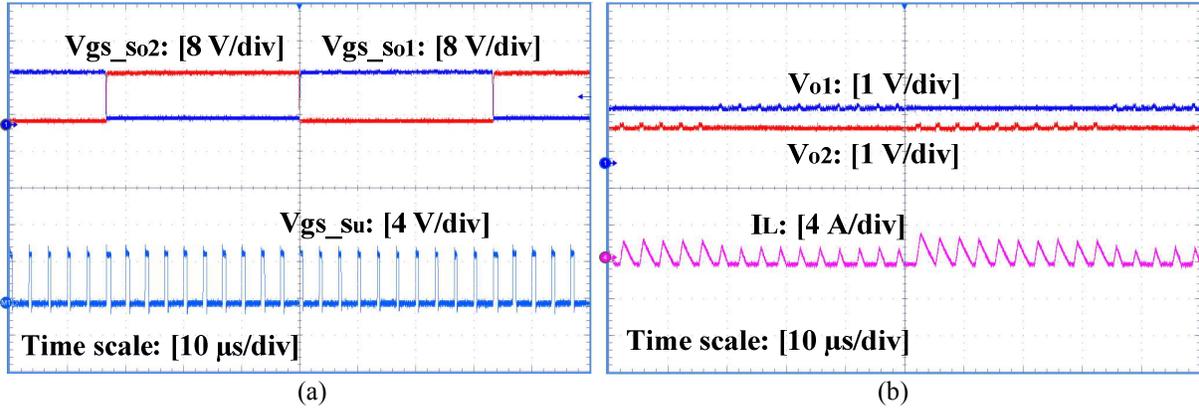


Figure. 6.7: Experimental waveforms of the two-output SIMO converter when the two channels both operate in DCM with $I_{o1}=200 \text{ mA}$ and $I_{o2}=500 \text{ mA}$. (a) Gate-to-source driving signals (V_{gs}) for the power switches; (b) output voltages and inductor current

A. Steady-State Operations

The performance of the PM controlled SIMO converter is first evaluated under steady-state conditions. The SIMO converter is tested under the same three different case scenarios as discussed in Section III. The first case is when the two channels both operate in DCM where T_r is not required. Fig. 6.7 shows the experimental waveforms when $V_{ref1} = 1.5 \text{ V}$, $I_{o1} = 200 \text{ mA}$ (DCM), $V_{ref2} = 1 \text{ V}$, and $I_{o2} = 500 \text{ mA}$ (DCM). Fig. 6.7 (a) shows the gate-to-source driving signals (V_{gs}) for S_{o1} , S_{o2} , and S_u . It can be observed from Fig. 6.7 (a) that the output switches S_{o1} and S_{o2} are turned on alternately for the same period of time. S_u has distinct duty cycle values during the on-times of each output switch in order to regulate the output voltages of the two channels at corresponding reference values. Fig. 6.7 (b) shows the output voltages and the

inductor current of the SIMO converter. It is shown in Fig. 6.7 (b) that the output voltages of the two channels are stable and regulated at their corresponding reference values, i.e., 1.5 V and 1 V, without any cross regulation between one another. In the meantime, the inductor current returns to zero by the end of each switching cycle of the input switches as the two channels both operate in DCM. No voltage spike is observed in either of the two output voltages.

For the second case scenario where the two channels both operate in CCM, the load current one is set to 2 A while the load current two is set to 1.5 A. Since the two channels both operate in CCM, the inductor current reset technique is applied for both channels to reset the inductor current before the other output channel conducts, as shown in Fig. 6.8. It is observed that the output voltages of the two channels are regulated at corresponding reference values ($V_{ref1}=1.5$ V and $V_{ref2}=1$ V) without any cross regulation in between. In addition, no voltage spike is observed in the output voltages thanks to the use of the proposed inductor current reset technique.

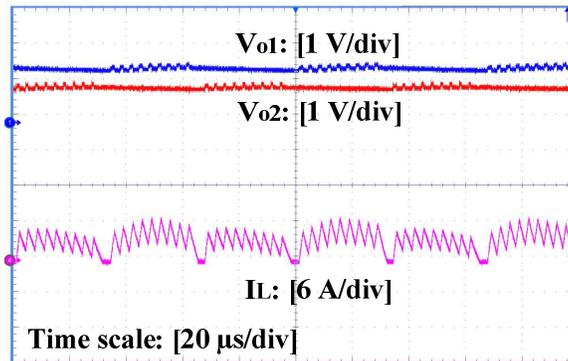


Figure. 6.8: Experimental waveforms of the two-output SIMO converter when the two channels both operate in CCM with $I_{o1}=2$ A and $I_{o2}=1.5$ A. Output voltages (top two traces) and inductor current (bottom trace)

To test the third case scenario where the two channels operate in different modes, load current one is set to 2 A (CCM) while load current two is set to 200 mA (DCM). The experimental waveforms for this case are shown in Fig. 6.9. It can be seen from Fig. 6.9 that

independent output voltage regulation are still achieved for both channels without any cross-regulation between one another.

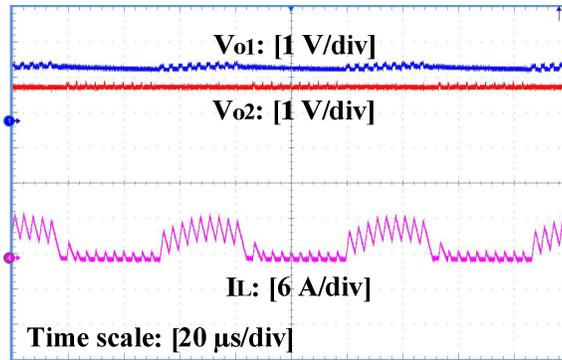


Figure. 6.9: Experimental waveforms of the two-output SIMO converter when the two channels operate in different modes with $I_{o1}=2\text{ A}$ (CCM), and $I_{o2}=200\text{ mA}$ (DCM). Output voltages (top two traces) and inductor current (bottom trace)

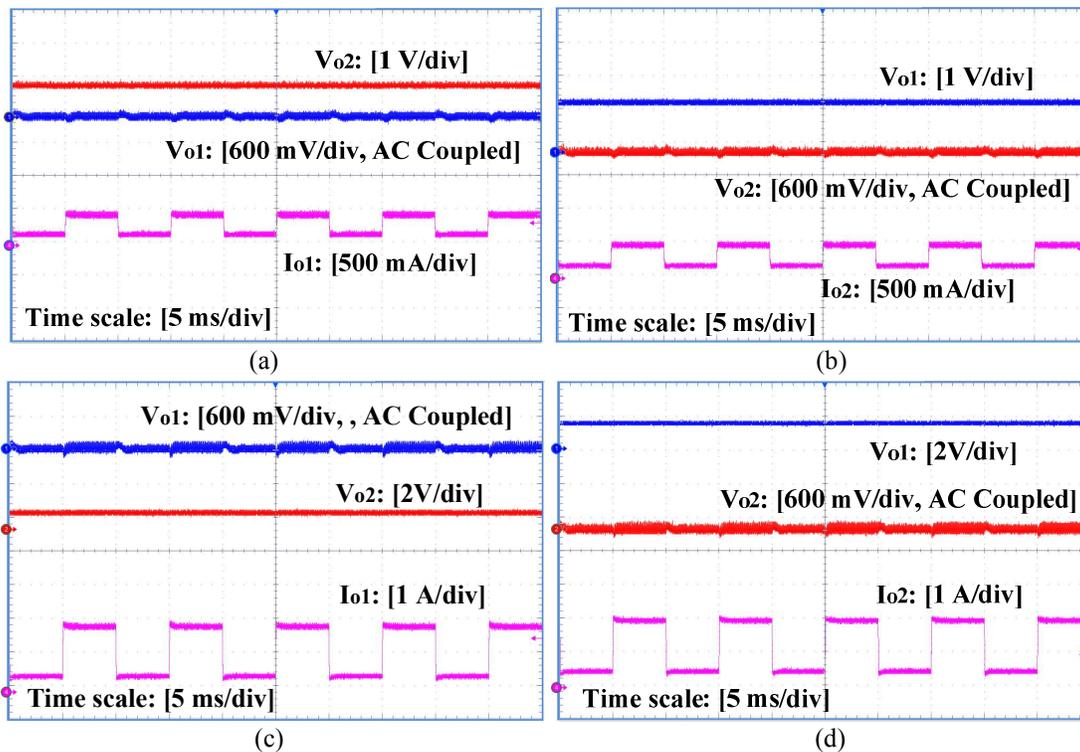


Figure. 6.10: Experimental waveforms for the two-output SIMO converter when one channel is under load transient condition while the other is under steady-state condition. Output voltages (top two traces) and inductor current (bottom trace). (a) $I_{o1}=200\text{ mA}-500\text{ mA}-200\text{ mA}$ and $I_{o2}=200\text{ mA}$, (b) $I_{o1}=200\text{ mA}$ and $I_{o2}=200\text{ mA}-500\text{ mA}-200\text{ mA}$, (c) $I_{o1}=500\text{ mA}-2\text{ A}-500\text{ mA}$ and $I_{o2}=2\text{ A}$, (d) $I_{o1}=2\text{ A}$ and $I_{o2}=500\text{ mA}-2\text{ A}-500\text{ mA}$

In summary, the operation of the two channels are completely decoupled from one another under steady-state conditions regardless of the operation modes of the two channels.

B. Dynamic Operations

In addition to steady-state operations, the performance of the proposed PM controller and inductor current reset technique is further tested and evaluated under load transient conditions. The output voltage for load one is still regulated at 1.5 V while the output voltage for load two is still regulated at 1 V. Fig. 6.10 shows the experimental waveforms when one output is under load transient condition while the other is under steady-state condition. Fig. 6.10 (a) and (b) show the waveforms when one output is under a load transient of 200 mA(DCM)-500 mA(DCM)-200 mA(DCM) while the other output is under a constant load current of 200 mA(DCM). No mode transitions occur in this case in either of the two channels. It can be observed from Fig. 6.10 (a) and (b) that the load transient of one output does not interfere with the steady-state operation of the other channel. Consistent results are obtained as shown in Fig. 6.10 (c) and (d) under the case scenario where one output is under a load transient of 500 mA (DCM)-2A(CCM)-500mA(DCM) that causes mode transitions while the other output is under a constant load current of 2A(CCM).

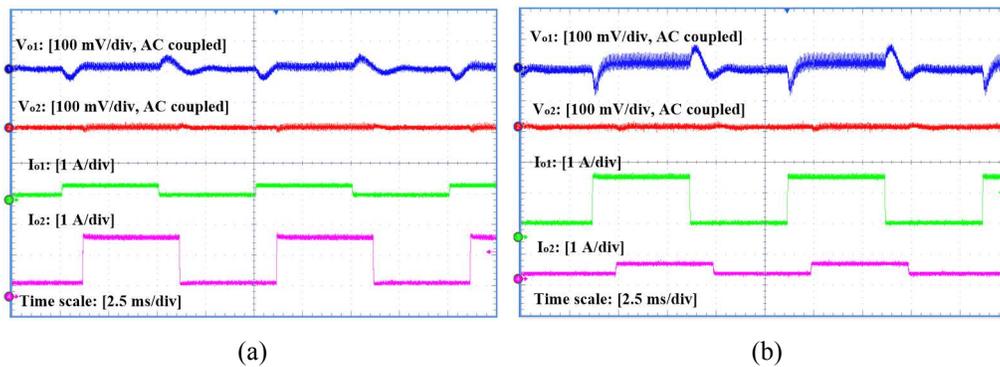
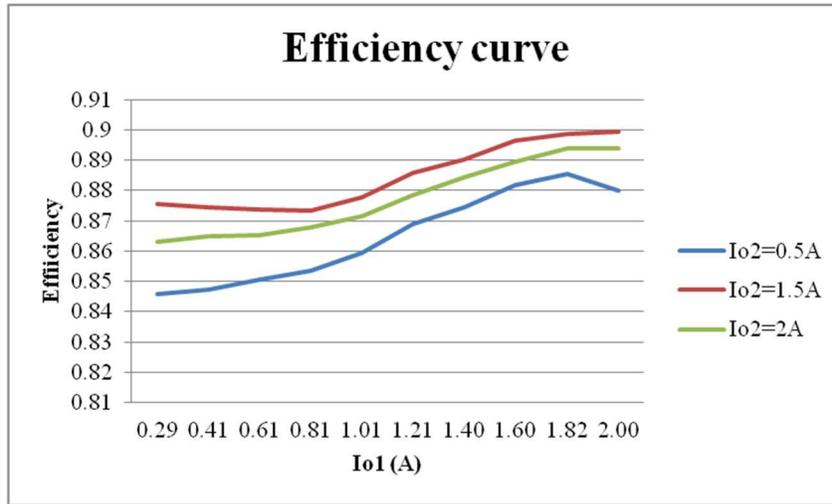
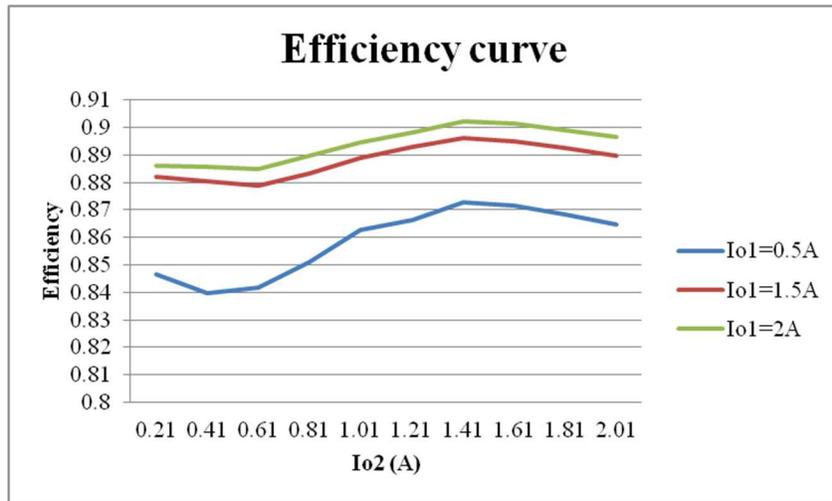


Figure 6.11: Experimental waveforms for the two-output SIMO converter when two outputs are both under load transient condition. Output voltages (top two traces) and load currents (bottom two traces). (a) $I_{o1}=200\text{ mA}-500\text{mA}-200\text{mA}$ and $I_{o2}=500\text{ mA}-2\text{A}-500\text{mA}$; (b) $I_{o1}=500\text{ mA}-2\text{A}-500\text{mA}$ and $I_{o2}=200\text{ mA}-500\text{mA}-200\text{mA}$

Fig. 6.11 shows the experimental waveforms obtained under the condition that the two outputs are both under load transient conditions of different magnitudes. It can be observed from Fig. 6.11 that the load transient only causes overshoot/undershoot in the corresponding output voltage and does not interfere with the dynamic operation of the other output.



(a)



(b)

Figure. 6.12: Efficiency curves of the two-output buck SIMO converter prototype with the proposed power multiplexed control at (a) fixed load current two; (b) fixed load current one

Fig. 6.12 shows the efficiency curves of the two-output buck SIMO converter prototype with the proposed PM controller under different operating conditions. It can be seen that the efficiency of the converter peaks at 90.2% when the load current one is 2A and load current two is 1.41A. Also, it can be noticed that the efficiency curves exhibit consistent trends at different load currents.

C. Three-Output SIMO Experimental Results

Sample experimental results obtained from a preliminary three-output SIMO converter prototype are shown in this section to further show the effectiveness of the proposed PM controller. Fig. 6.13 through Fig.6.15 show the steady state waveforms for the prototype with three outputs. Note that the input and output switches' frequencies are set at 300kHz and 30kHz, respectively. In other words, each output switch period contains 10 input switch periods. The duty cycle values for the three output switches are 40%, 30%, 30%. The reference output voltage and load current information for each channel are summarized below:

$$V_{\text{ref1}} = 1.5\text{V}, I_{\text{o1}} = 0.5\text{A}$$

$$V_{\text{ref2}} = 1.8\text{V}, I_{\text{o2}} = 0.7\text{A}$$

$$V_{\text{ref3}} = 1.5\text{V}, I_{\text{o3}} = 0.6\text{A}$$

It can be observed from Fig. 6.15 that the output voltage of each channel is regulated at its reference value without any cross regulation between the channels.

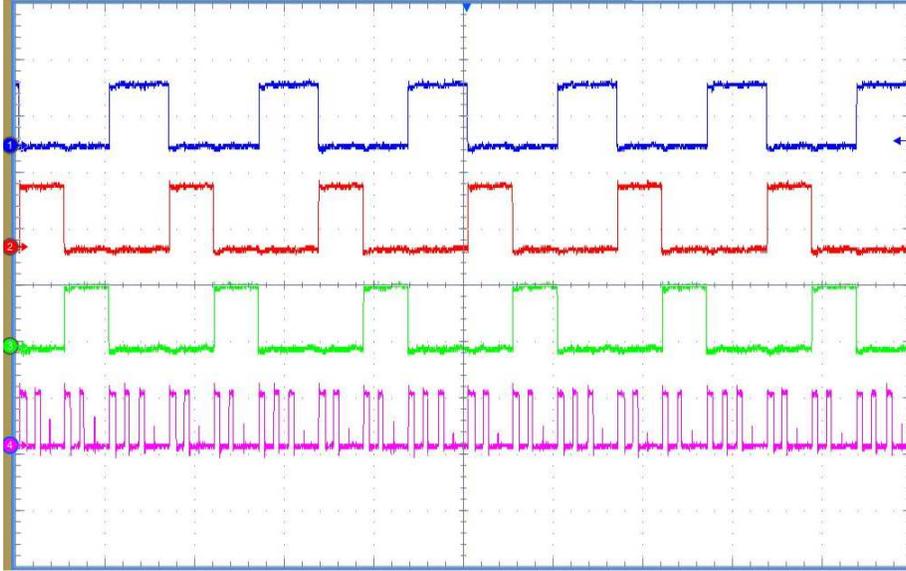


Figure. 6.13: PWM waveforms for the power switches of the SIMO converter prototype with three outputs. From top to bottom:
 Output switch 1 PWM: 3V/div, 20 μ s/div
 Output switch 2 PWM: 3V/div, 20 μ s/div
 Output switch 3 PWM: 3V/div, 20 μ s/div
 Input high-side switch PWM: 5V/div, 20 μ s/div

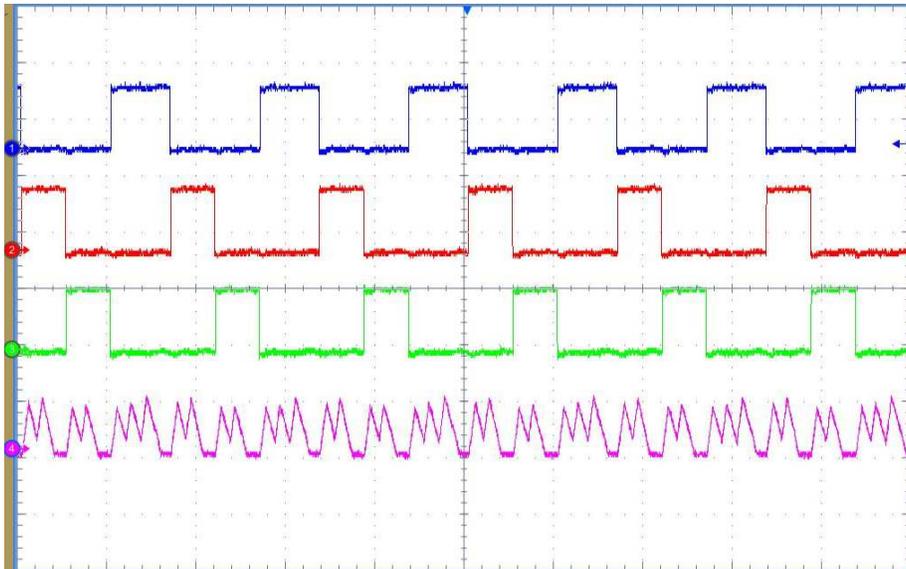


Figure. 6.14: Steady-state waveforms for the SIMO converter prototype with three outputs. From top to bottom:
 Output switch 1 PWM: 3V/div, 20 μ s/div
 Output switch 2 PWM: 3V/div, 20 μ s/div
 Output switch 3 PWM: 3V/div, 20 μ s/div
 Inductor current: 5A/div, 20 μ s/div

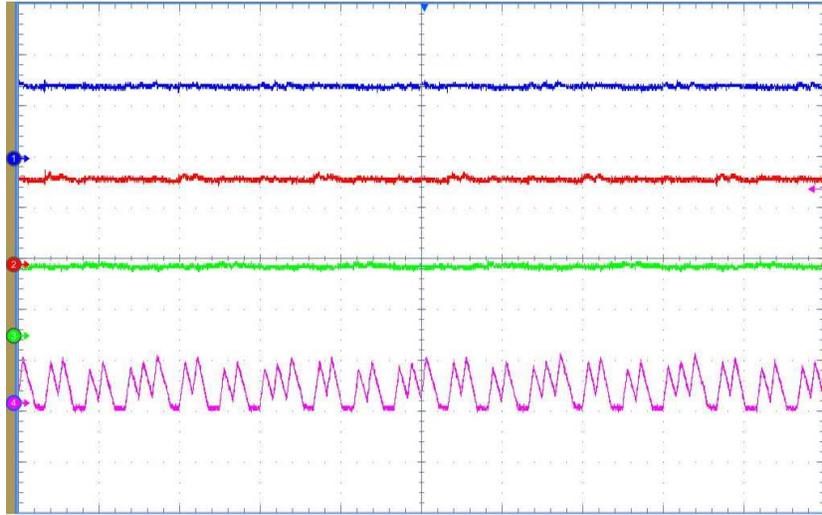


Figure. 6.15: Steady-state waveforms for the SIMO converter prototype with three outputs.

From top to bottom:

Channel 1 output voltage: 1V/div, 20 μ s/div

Channel 2 output voltage: 1V/div, 20 μ s/div

Channel 3 output voltage: 1V/div, 20 μ s/div

Inductor current: 5A/div, 20 μ s/div

Fig. 6.16 shows the waveforms of the three-output SIMO converter prototype during dynamic operation of load 3. The reference output voltage and load current information for each channel are summarized below:

$$V_{\text{ref}1}=1.5\text{V}, I_{o1}=0.5\text{A}$$

$$V_{\text{ref}2}=1.8\text{V}, I_{o2}=0.7\text{A}$$

$$V_{\text{ref}3}=1.5\text{V}, I_{o3}=0.6\text{A}-1.2\text{A}-0.6\text{A}$$

It can be observed that the dynamic operation of output channel 3 causes only overshoot/undershoot at output 3 but not at the other outputs (no cross regulation). The steady-state operation of channel 1 and channel 2 are well maintained without being interfered by the dynamic operation of channel 3.

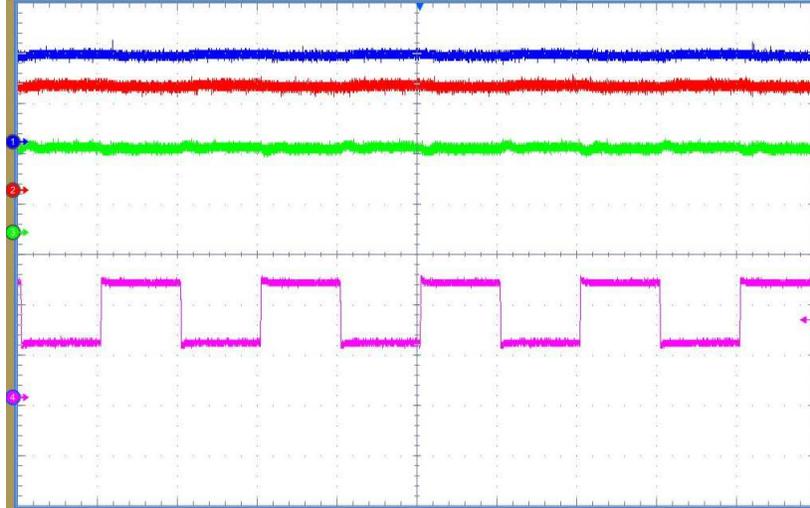


Figure. 6.16: Dynamic operation waveforms for the SIMO converter prototype with three outputs. From top to bottom:
 Channel 1 output voltage: 800mV/div, 5ms/div
 Channel 2 output voltage: 800mV/div, 5ms/div
 Channel 3 output voltage: 800mV/div, 5ms/div
 Channel 3 load current: 0.5A/div, 5ms/div

D. Additional Comments

- Low-frequency output voltage ripple

The low-frequency ripple at the output is a function of the output switches' frequency and output capacitance. Therefore, the low frequency output voltage ripple can be reduced by increasing the switching frequency of the output switches, by increasing the output capacitance, or by combination of both to yield an optimized design. Note that because of the proposed inductor current reset technique, the output switches are turned on and turned off at zero current which reduces the switching loss.

- Size/volume of PM controlled SIMO converter

With the proposed PM controller, the SIMO converter can lead to reduced footprint and volume in addition to weight compared to using multiple single-output converter solution even though it might require larger output capacitance to meet the same output voltage requirement.

This is because the footprint and volume reduction resulted from the power inductors, switches, drivers, and their corresponding traces/interconnections surpasses the added foot print and volume of the output capacitors. Note that the technological advances has resulted in increasing the capacitors' density at a faster rate than increasing the power inductors' density.

It can be shown that for an example SIMO converter design with three outputs, more than 14% net reduction in component's footprint and more than 20% net reduction in component's volume can be achieved when using commercially available components. For this SIMO converter with the proposed controller, it require one power inductor instead of three power inductors, five MOSFETs instead of six MOSFETs, and five gate drivers instead of six gate drivers, while requiring some additional output capacitors to meet the same ripple requirements when the SIMO converter's output switches operate at lower switching frequency than the switching frequency of three individual single output converters.

6.5 Summary

This chapter presents a power-multiplexed control scheme for a SIMO power switching converter. The PM control scheme results in eliminating the cross regulation between the multiple outputs while maintaining voltage regulation for each output during steady-state and dynamic operations. To eliminate the voltage spike on the output switching node during CCM operation, a simple inductor current reset technique is proposed. The PM controller can be implemented with a low-cost microcontroller or analog circuitries due to its simplicity. A two-output buck derived SIMO converter is utilized as an example in this work to illustrate and verify the operation of the proposed controller. Experimental results verify the effectiveness and performance of the proposed PM control scheme under different case scenarios.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Summary of Conclusions

Batteries have been widely used in many applications including portable electronics, EVs/HEVs, and distributed smart power grids. In addition to the advances of the battery technologies, the BMS plays a critical role in ensuring the efficient, reliable and safe operation of the battery pack and the system it powers. Among the functions of BMS, part of this dissertation work focus on addressing the issues related to online battery impedance measurement/monitoring and cell balancing for discharging and charging operation.

In addition to the BMS issues, this dissertation also addresses the common cross regulation issue related to the SIMO converters which have gain popularity in battery-powered applications due to the advantages including reduced number of components, size and cost as compared to multiple-converter solution. The cross regulation issue has been a key obstacle preventing the widespread adoption of the SIMO converter in broad range of applications.

To address the aforementioned issues, this dissertation proposes several advanced control and power management schemes utilizing the flexibility of digital controller. The contribution of this research work include the research and development of the following concepts: (1) Online battery impedance measurement method; (2) Energy sharing controller for cell balancing in battery discharge mode; (3) Battery charging controller with energy sharing for cell balancing during charging operation; (5) Small-signal modeling and analysis of the energy sharing controlled distributed battery system; (6) Power-multiplexed controller addressing the cross

regulation issue of the SIMO converters during both steady-state and dynamic operation regardless of the operating mode of each output channel, i.e., CCM or DCM. All of the proposed control and power management schemes have been validated and evaluated with proof-of-concept experimental prototype results.

7.1.1. Online Impedance Measurement Method

This dissertation first proposes an online impedance measurement method for electrochemical batteries. The battery impedance measurement is realized via the control and perturbation of the DC-DC power converter which interfaces the battery with the load. With the proposed method, the signal generation circuits/devices required by the existing impedance measurement methods are eliminated, which leads to reduced cost, design complexities and size of the overall system. This method can be performed either continuously or periodically without interrupting the normal operation of the battery system and power converter. The proposed method is well suited for real-time battery impedance monitoring.

In addition, a practical online SOC estimation method for lithium-ion batteries is provided in this dissertation based on the obtained impedance data. With the proposed method, there is no need to put the battery in rest/relaxation mode for a long period of time in order to reach electrochemical equilibrium prior to the OCV measurement. Experimental results have validated the effectiveness of the proposed online impedance measurement method and its utilization in the online SOC estimation.

7.1.2. Energy Sharing Controller for Cell Balancing in Battery Discharge Mode

An energy sharing controller is proposed in this dissertation based on a distributed battery system architecture. The DC-DC power converters with the proposed energy sharing controller are utilized to achieve SOC balancing between the battery cells while providing DC bus voltage

regulation to the rest of the system or load. As a result, there is no need for two independent converter systems for cell SOC balancing. This results in reduced design complexity of the battery energy storage system.

The proposed energy sharing controller addresses the battery cells' SOC imbalance issue from the root by adjusting the discharge rate of each cell while maintaining the total regulated DC bus voltage. The energy transfer between the battery cells which is usually required in the existing cell balancing solutions is no longer needed, thus eliminating the power losses caused by the energy transfer process.

The proof-of-concept experimental prototype results have validated the performance of the proposed energy sharing controller during discharging operation. The developed architecture and energy sharing controller is an attractive candidate for many battery energy storage applications including EVs/PHEVs (which utilize power distribution scheme that has a DC-DC power converter), DC microgrids, aerospace battery systems, laptop computers battery packs, and other portable devices with multi-cell battery energy storage.

7.1.3. Battery Charging Controller with Energy Sharing

The energy sharing controller proposed in the Chapter 3 is upgraded by integrating a battery charging control algorithm with the energy sharing concept in order to address the cell balancing issue during battery charging operation. The upgraded battery charging controller also addresses the battery cells' charge imbalance issue from the root by adjusting the charge rate of each battery cell while maintaining the average cell current to be regulated at a given level. The energy transfer between the battery cells is eliminated, thus leading to increased efficiency of the battery system. The experimental prototype results have validated the cell balancing performance of the upgraded battery charging controller with energy sharing during charging operation.

7.1.4. Small-Signal Modeling and Energy Sharing Controller Design

State-space averaging small-signal modeling and analysis is performed in Chapter 5 in order to gain deeper insights into the dynamics of the energy sharing controlled distributed battery system during both discharging and charging operation. Based on the derived small-signal models and associated transfer functions, the control loops are compensated for different operation mode, including discharge mode, constant current charging mode and constant voltage charging mode, based on the rule-of-thumb frequency-domain design guidelines and criteria. The simulation and experimental results obtained from a two-cell distributed battery system prototype have validated the derived small signal models and designed closed-loop compensators.

7.1.5. Power-Multiplexed Controller for SIMO Converters

In addition to addressing several BMS issues, this dissertation also proposes a power-multiplexed control scheme to address the cross regulation issue of SIMO switching converters which are increasingly used in portable applications where a battery powers multiple electronic loads. The PM control scheme completely decouples the operation of each output by multiplexing the conduction of each output switch. To eliminate the voltage spike on the output switching node during CCM operation, a simple inductor current reset technique is proposed. The PM controller can be implemented with a low-cost microcontroller or analog circuitries thanks to its simplicity. A two-output buck derived SIMO converter is utilized as an example in this work to illustrate and verify the operation of the proposed controller. Proof-of-concept experimental results are presented to verify the operation of the proposed PM control scheme under different case scenarios.

7.2 Future Research Directions

The following subsections give a brief outlook on some possible future research directions that are related to the work presented in this dissertation.

7.2.1. Accurate SOC Estimation

In Chapter 3 and 4, an energy sharing controller is proposed to achieve SOC balancing between the battery cells in a battery pack during discharging and charging operation, respectively. The accuracy of the SOC estimation directly impacts the performance and reliability of the proposed energy sharing controller as it is the case in other SOC balancing schemes. If the SOC estimation is not accurate, overdischarge or overcharge of the cells is likely to occur. The commonly used coulomb counting method is utilized in this work for the battery SOC estimation. As mentioned in Chapter 3 and 4, coulomb counting method has some downsides. For instance, it does not take into account factors that may change the usable capacity of the battery, such as temperature variation, discharge/charge rate, and aging effects, among others. Moreover, the coulomb counting method is highly sensitive to the initial SOC value and current measurement accuracy. The disadvantages of some other SOC estimation methods are summarized in Section 1.2.C of Chapter 1. Therefore, a more accurate and reliable SOC estimation method is needed in order to achieve desired cell balancing performance of the proposed energy sharing controller. In addition to the need for an accurate and fast current sensor (fast ADC is needed if digital control is used), the battery impedance information obtained by the method proposed in Chapter 2 has the potential to be used for providing insights into the health condition and capacity variation of the battery. This can lead to a more accurate SOC estimation results.

7.2.2. Online Battery SOH Estimation

Another important aspect of BMS is the SOH estimation of the battery cells during online operation for efficient power and energy management of the battery system. By modifying the single cell impedance measurement method proposed in Chapter 2, online multi-cell impedance measurement can be accomplished with the distributed battery system architecture used in Chapter 3 and 4. As the impedance of the battery itself reflects the variation of many factors such as temperature, capacity and electrochemical characteristics, the accuracy of the SOH estimation should be improved if the impedance data is utilized along with the approaches/techniques presented in the literature. For example, reference [30-31] reveal that the battery impedance growth at the trough frequency of the second semi-circle on the impedance spectrum highly correlates with the power fade, or SOH, of the battery cell. Other new techniques can also be explored to produce a more accurate and robust SOH estimation.

7.2.3. High Power Density Integration of The Distributed Battery System

In order to be applied in real-world applications, such as EVs/HEVs, the proposed energy sharing controlled distributed battery system architecture must be optimized in terms of power density, efficiency, cost, EMI, and thermal performance, among others. To achieve higher power density BPM design, other topologies can also be explored which feature lower count of magnetic components (such as switch-capacitor based converter topologies), fewer power switches, and reduced filter requirement, among others. Efficiency can be further improved by using power FETs with lower gate charge, less parasitics and lower on-resistance. In addition, the BPM efficiency is expected to be improved by using multi-layer PCB design with better component placement and trace routing.

From the battery system point of view, higher power density can be achieved through better integration of the BPMs and external functional blocks, such as thermal management and communication, among others.

7.2.4. Adaptive Optimization of The Inductor Current Reset Time

During the CCM operation of the PM controlled SIMO converter discussed in Chapter 6, the inductor current needs to be reset before another output channel conducts in order to prevent the cross regulation between the outputs. In this work, the inductor current reset time is set to a large value with sufficient margin allowing the inductor current to fully reset under all load and input voltage conditions. However, in order to achieve optimized efficiency and output voltage ripple, it is advantageous to dynamically optimize this inductor current reset time under different operating conditions. This could be achieved by calculating the time it takes for the inductor current to drop to zero under different V_{in} and I_o conditions at the beginning of the conduction period of a given output channel.

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