ON A FUTURE FOR SILICON CARBIDE IN POWER ELECTRONICS APPLICATIONS

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A THESIS

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ABSTRACT

Silicon-based MOSFETs and IGBTs have long been the premiere options for semiconductor switches in power converter applications. However, each of these Si based device structures has limitations that constrain the performance capabilities of their intended applications. The recently commercialized SiC MOSFET allows for optimized application designs that are not constrained by the limitations of Si semiconductor switches as in traditional designs.

This thesis will explore the device properties of SiC MOSFETs and compare them to the properties of Si MOSFETs and Si IGBTs. Device characterization methods for experimentally determining switching losses and conduction losses will be presented, along with special considerations to be made when dealing with wide band-gap devices.

In order to demonstrate SiC MOSFETs' system level optimization opportunities, this thesis will present a hard-switched 5 kW DC-to-DC converter that leverages the SiC devices in question to reach a system level efficiency of 99%. This converter will also be used as a platform to perform a head-to-head comparison of Si IGBTs and SiC MOSFETs in terms of overall system efficiency.

DEDICATION

This thesis is dedicated to everyone who stood behind me and offered assistance or encouragement not only throughout the process of developing this manuscript, but also during the entire course of my educational career.

LIST OF ABBREVIATIONS AND SYMBOLS

W	Watt
F	Farad
L	Inductance
C	Capacitance
H	Henry
Ω	Ohm
dt	Change in Time
dI	Change in Current
dv	Change in Voltage
J	Joule
AC	Alternating Current
DC	Direct Current

ACKNOWLEDGEMENTS

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Special thanks also go to Dr. Sujit Banerjee and Dr. Tim Haskew my other committee members. These gentlemen are first class electrical engineers but at the same time are easy going and a genuine delight to be around. Additional thanks should be given to Dr. Sujit Banerjee and the rest of Monolith Semiconductor Inc. for sponsoring the research associated with this thesis.

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Lastly, but certainly most important, I would like to thank my family. My sister, Maggie, is a constant reminder to be a good role model. My brother, Skyler, has been my best friend my entire life. We have grown up side-by-side and he has consistently pushed me to strive for the

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CHAPTER 1

INTRODUCTION & BACKGROUND

1.1 The Promise of Silicon Carbide

The electrical engineering sub-discipline of power electronics is an integral enabler of many modern day technologies that span an enormous range of power levels [1]. With world energy consumption reports trending upward each year [2], there is an increasing amount of economic and political pressure to improve the efficiency at every step of the energy consumption cycle, which of course includes power conversion as well. By leveraging cutting edge solid-state devices and advanced control techniques in their designs, power electronics engineers are pushing the performance envelope of power converters to new heights. The focus of this thesis is the emerging technology of wide band-gap (WBG) semiconductors, specifically SiC MOSFETs, and the system level optimization opportunities that they present. This paper will also present the design process of a concrete example application for the semiconductors in question, which takes the form of a DC-to-DC converter.

1.2 Device Landscape

The semiconductor switches traditionally used prior to the emergence of the WBG devices highlighted in this thesis significantly constrain the operating conditions and performance of the power conversion systems in which they are implemented.

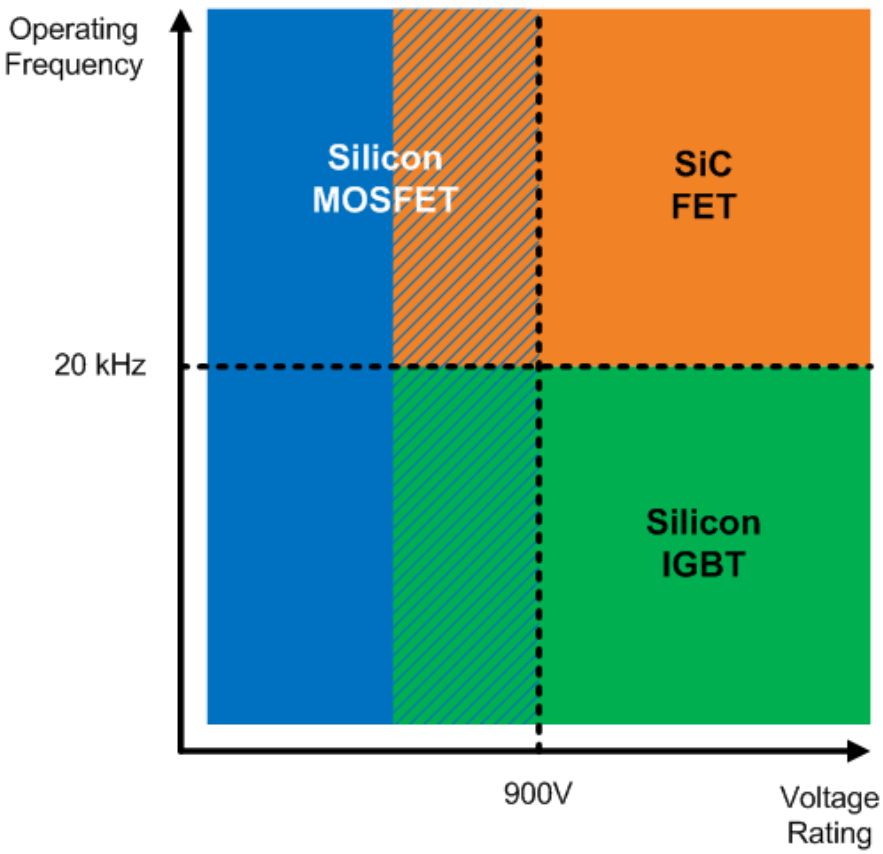

Figure 1 - System Level Application Device Landscape

Figure 1 illustrates the previously mentioned point by distinguishing regions of operating conditions predicated on voltage rating and operating frequency along with the devices traditionally used to satisfy those requirements. As the graphic indicates, Si IGBTs are suitable for voltage ranges in which a 1200V rated part is necessary, but they are limited to a maximum operating frequency of about 20 kHz. On the other hand, Si MOSFETs allow for operating frequencies well above 20 kHz. These devices however typically have an absolute maximum voltage rating of 900V which limits them to a usable operating voltage in the 600V range. Ultimately, SiC devices can accommodate both high voltage ratings and high operating

frequencies, which lead to an array of system level optimization opportunities which will be discussed in the following sections.

1.2.1 Efficiency

Efficiency, as mentioned in Section 1.1, is a priority when designing any power conversion system. When analyzing one of these systems, a majority of the power dissipation sources can easily be identified. Some losses can be attributed to the specific loss models for each circuit element, i.e. the equivalent series resistance (ESR) of the passive components, but these losses can be minimized by good fundamental circuit design techniques that will be discussed in Chapter 3. That leaves the semiconductor components, specifically the switches, as the primary contributor to power dissipation within a hard-switched converter. The losses associated with the semiconductor switches are classified into two categories, conduction losses and switching losses, which are explained in Figure 2.

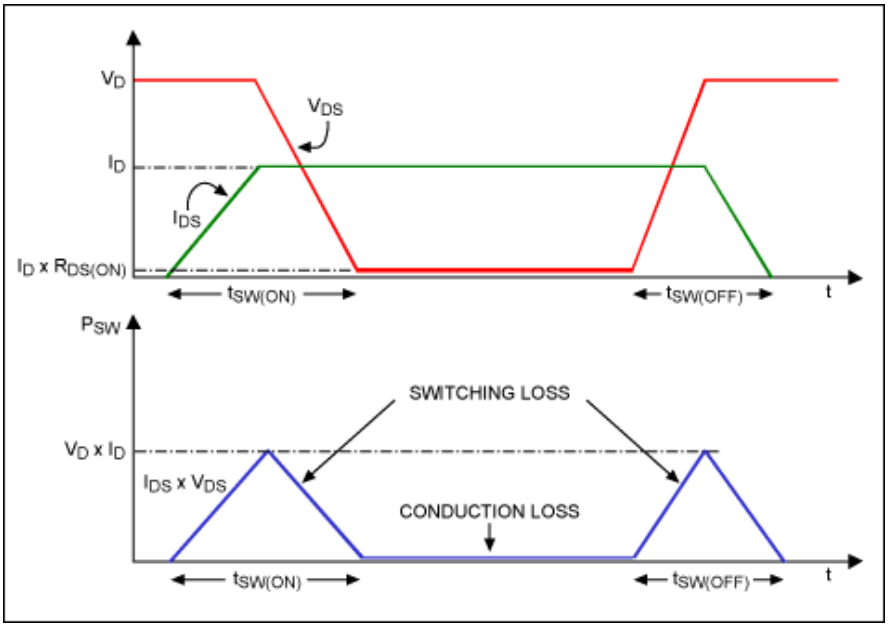

Figure 2 - Conduction and Switching Losses [3]

Figure 3 is presented in order to make a fair comparison in terms of conduction losses on the basis of specific on-resistance, which normalizes conduction performance by device active area. If Figure 1 were to be amended to include Si MOSFETs that were rated for 1200V, Figure 3 shows that these devices would have a specific on-resistance as much as 500 times greater than that of a comparable SiC device and thus much greater conduction losses [5].

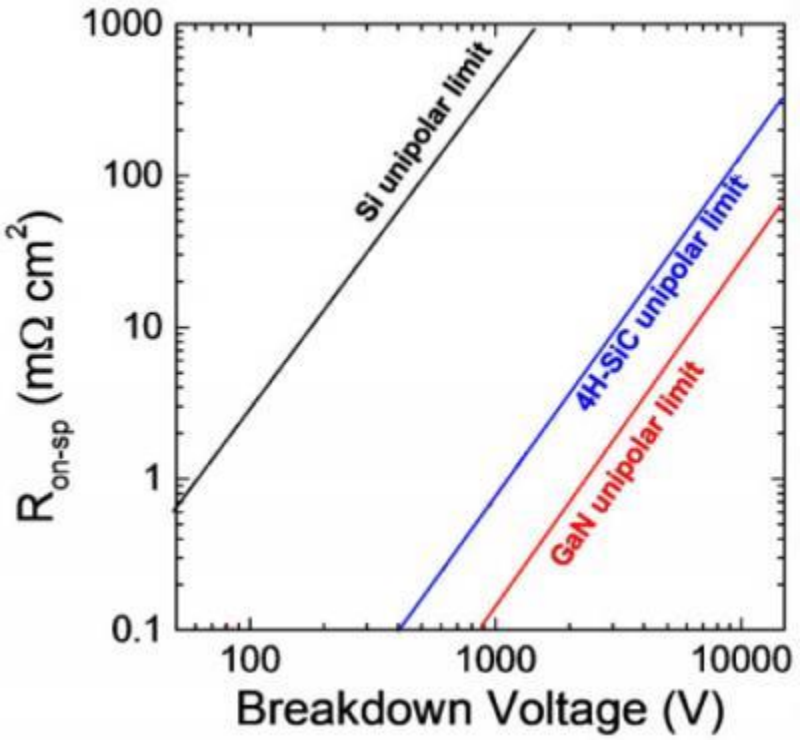

Figure 3 - Material Breakdown Voltage vs. Specific On-Resistance [4]

The bipolar nature of the Si IGBT device structure allows it to have extremely low conduction losses but it also limits the rate at which it can reach fully on and fully off states [6]. This quality causes the IGBT device structure to suffer significantly in the category of switching losses. By leveraging the MOSFET device structure and the semiconductor material of SiC, SiC MOSFETs

are able to excel at turn-on and turn-off rates as well as minimizing conduction losses, as will be demonstrated in Chapter 5.

1.2.2 Power Density

When discussing system-level optimization of power converters, efficiency is typically considered a first priority. Another metric that should not be ignored however is power density. The primary driver of power density in hard-switched converters is the filter component size. [7] Explains that the filter component size is directly related to the operational frequency of the converter. Since it has already been established in Figure 1 and Section 1.2.1 that a Si IGBT is incapable of accommodating switching frequencies greater than 20 kHz and a Si MOSFET is incapable of blocking voltages greater than 900V, the only option to improve power density of a ~1000V system is by implementing SiC devices.

1.2.3 Heat Dissipation

When considering power dissipation of power semiconductor switches, there are two major concerns. These concerns are overall system efficiency, which has been discussed in depth already, and thermal management. When a component dissipates power, it does so in the form of heat. Since the semiconductor components are typically responsible for a considerable portion of power dissipation within a converter, they also tend to dissipate considerable waste heat. In order to ensure the device remains operational, the device itself must maintain a junction temperature at or below its data sheet value, typically denoted as $T_{J,max}$. This is traditionally done by mounting some form of thermal management apparatus to the semiconductor devices. This could involve a heat sink with forced or natural air-cooling, the use of liquid cooled plates, or any

combination of these methods. Reducing the power consumption of the devices through improved conduction and switching losses directly reduces the heat load managed by this thermal system. Less heat dissipation means that smaller and less sophisticated cooling techniques can ultimately be used.

1.3 Objectives

The rest of this paper will serve as a composition of the cumulative knowledge gained by the author to this point concerning this specialized area of power electronics. The author will display a clear understanding of SiC semiconductor devices and how they compare to similar Si devices. A clear report will be provided that includes device level characterization as well as an application level design strategy that integrates and exploits advantageous properties of the devices under study.

1.4 Thesis Organization

The rest of this thesis is organized as follows.

Chapter 2 will discuss the characterization of discrete SiC MOSFETs. A method for conducting repeatable experiments that produce accurate and reliable empirical data will be presented. In addition, special metrology considerations that should be taken into account when characterizing SiC devices will be described.

Chapter 3 will demonstrate the power stage design process of a system-level application that allows the benefits of SiC devices to quantified. The author will present a start-to finish-design

process for a buck converter in which a paper design is developed into a tangible printed circuit board (PCB) that meets a set of design specifications.

Chapter 4 details the design process of the control stage of the application converter. Because SiC devices offer such versatility, digital control techniques are advantageous in order to fully exploit the capabilities of the devices.

Chapter 5 will detail the process for collecting empirical data from the converter. Efficiency data will be presented for a selection of comparable parts. The empirical data collected will also be compared to simulation data in order to verify that the design behaves as intended.

Chapter 6 will conclude and summarize the work presented in this paper and elaborate on future work to be done.

CHAPTER 2

CHARACTERIZATION

In Chapter 1, this thesis dissected a semiconductor switch's power dissipation characteristics into two categories, conduction losses and switching losses. Each of these sources of power dissipation was discussed and claims were made that a 1200V rated SiC MOSFET is able to offer comparable conduction losses to that of a similar Si IGBT while also being able to accommodate the high switching frequencies commonly associated with a Si MOSFET. This chapter will present methods for quantifying conduction loss and switching loss metrics associated with SiC MOSFETs.

2.1 Conduction Losses

Conduction losses in SiC MOSFETs are a function of a device property described in device data sheets as the on resistance ($R_{DS,on}$). Like the value suggests, conduction losses associated with a SiC MOSFET within a hard-switched buck converter can be represented by Equation (1).

$$P_{Cond}(W) = R_{DS,on} \times I_D \times D \times f_{SW} \quad (1)$$

Where:

I_D: device drain current

D: duty cycle

f_{SW}: switching frequency

2.1.1 Test Method

The $R_{DS,on}$ value for a SiC MOSFET can be experimentally extracted using a parametric curve tracing machine. This machine allows the user to insert a discrete part and sweep one parameter such as Gate-Source voltage (V_{GS}), Drain-Source voltage (V_{DS}), or Drain Current (I_D) while keeping other parameters constant. The machine is also equipped to monitor voltages and currents associated with the part during these parameter sweeps. This allows the test engineer to evaluate device characteristics such as breakdown voltage, leakage current, threshold voltage, or on-state resistance [15].

In the case where the user wants to evaluate the $R_{DS,on}$ value of a part, he or she would use the machine to generate a set of forward curves such as the ones shown in Figure 4.

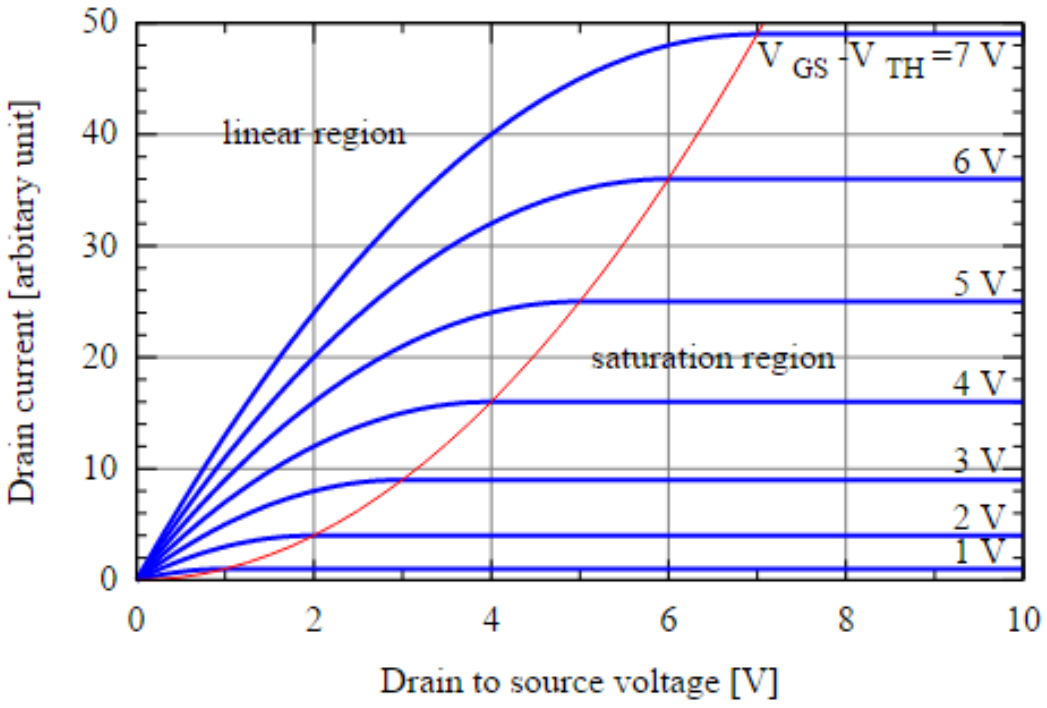

Figure 4 – Forward Curves Used for Determining $R_{DS,on}$ [26]

In order to extract a value for the DUT's on-state resistance from these forward curves, the test engineer would select the line that corresponds to the desired V_{GS} operating point (typically 20V for a SiC MOSFET). The inverse slope of this line in the linear region would be equal to that DUT's on-state resistance.

2.2 Switching Losses

Switching losses associated with any semiconductor switch are a function of how fast a device can reach its fully on or fully off state. SiC MOSFETs are unipolar devices with extremely low parasitic capacitances. As a result, they will generally have faster edge rates and higher dV/dt capabilities than similarly-rated IGBT's. This property means that the SiC MOSFETs will spend less time in the on/off transition states and as a result, dissipate less power during switching events. This claim can be confirmed via a test known as a double pulsed clamped inductive load (CIL) test [17]-[18].

2.2.1 CIL Test Circuit Theory

In order to perform CIL testing in support of this thesis, a dedicated test stand was designed, fabricated and assembled. Figure 5 demonstrates a high-level illustration of the test stand circuit schematic. The list of the test stand's pertinent elements and their description follows.

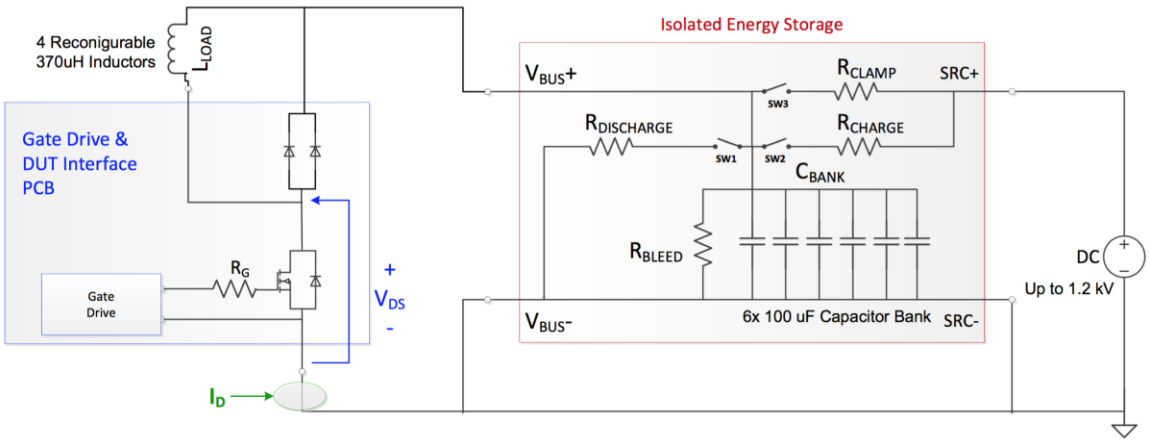

Figure 5 - Circuit Schematic of CIL Test Stand

From right to left:

- DC Power Supply – this supply is responsible for charging the isolated energy storage capacitor bank.
- Isolated Energy Storage – this network of capacitors, resistors and relays offers an added barrier of protection between the DUT and DC power supply in the event of a malfunction. A galvanically isolated user control box operates the relays responsible for charging and discharging the capacitor bank.
- Load Inductor – This inductor value is selected based on other test parameters.
- Gate Drive & DUT Interface PCB – by designing DUT interface boards in a modular fashion, like the one present in Figure 6, the CIL test apparatus can be used to test multiple device packages while maintaining optimal power flow. This PCB is responsible for measurement interface ports as well.

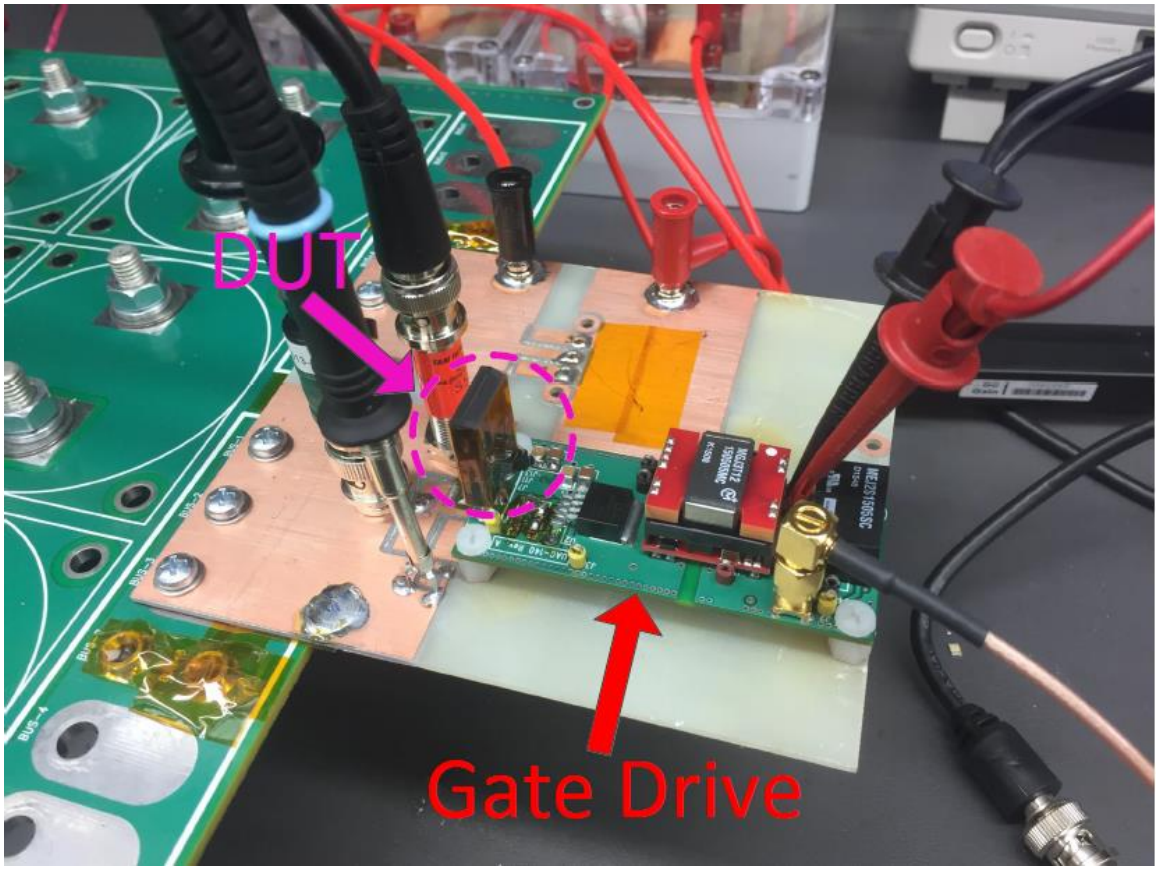

Figure 6 - DUT PCB

2.2.1.1 General CIL Operation

Figure 7, illustrates a simplified version of the circuit used to perform a CIL test. During a CIL test, the current will flow in one of two paths as denoted in Figure 7.

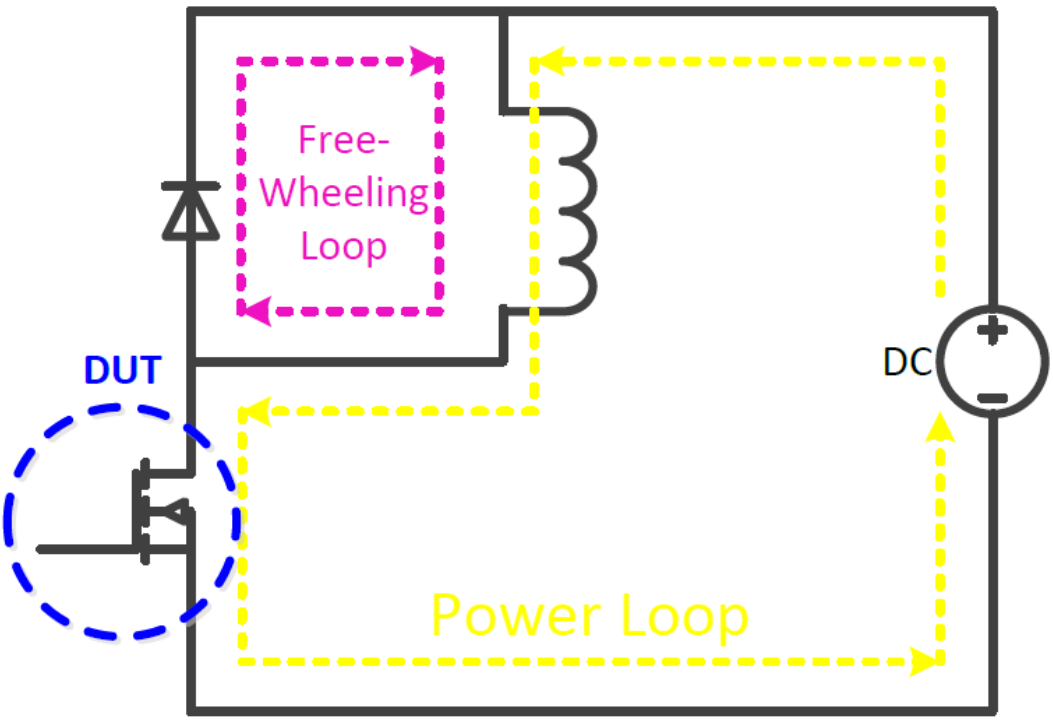

Figure 7 - General CIL Test Circuit Schematic

The objective of a CIL test is to turn the device under test (DUT) on and off under as similar V_{DS} and I_D conditions as possible [17]. By using an inductive load, this test also creates conditions which are very similar to those encountered in operation of an actual hard-switched converter. During the turn-on and turn-off events, a digital oscilloscope is used to capture the V_{DS} and I_D waveforms of the DUT. For the current effort, the DUT, as shown in Figure 5, is controlled via an arbitrary waveform generator and a custom gate drive circuit designed specifically for WBG devices similar to the one in [19].

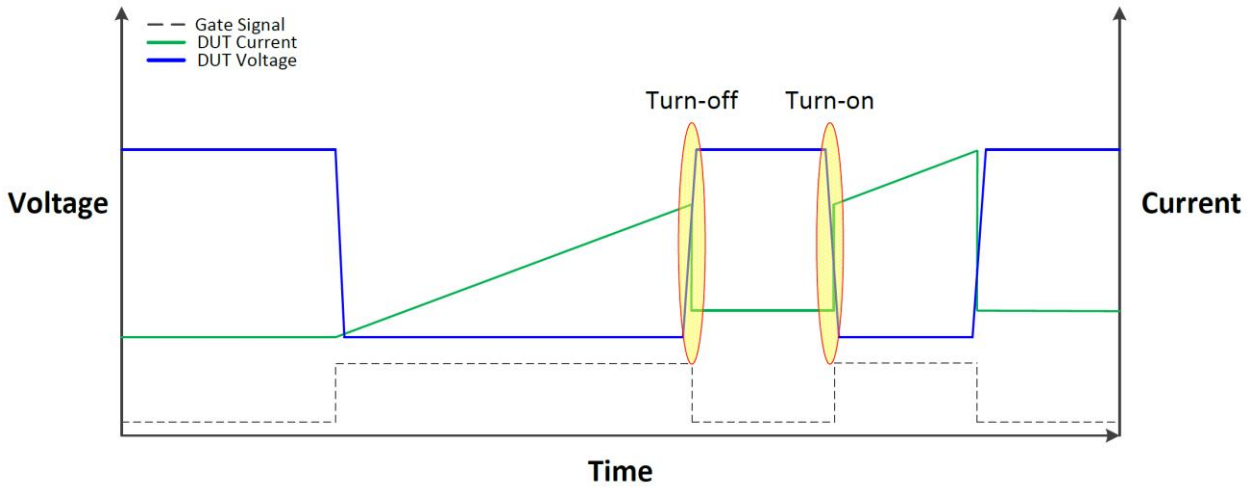

Figure 8 - CIL Test Waveforms

Figure 8 illustrates a high-level abstract diagram of a single CIL test in which the Gate Signal (V_{GS}) controls the state of the DUT and is active high. In this figure, it can be seen that the first pulse, or "charging pulse" is used to bring the load current up to the desired operating condition; and the second pulse is used to generate a pair of turn-off and turn-off events at this set-point. Not only does a CIL test allow the user to analyze DUT characteristics during turn-on and turn-off events (highlighted in yellow) at similar operating conditions as mentioned earlier, it also provides the user with the ability to precisely control these operating conditions as well.

Two primary variables not associated with the DUT itself strongly influence the switching energy dissipated during a CIL test. The first variable, V_{DS}, is simple enough to control. The DC supply is programmed to the desired V_{DS} value and then capacitor bank in the isolated energy storage unit is subsequently charged to that value before triggering the DUT. The second variable, the drain current magnitude, is only slightly more difficult to control. The principle of the CIL test circuit is based on the assumption that current through the load inductor remains nearly constant during the off-state of the switch due to low losses in the loop formed by the

inductor and freewheeling diode. Knowing that the current through the load inductor is equal to the current through the DUT during the device on-state, the user may predict the DUT drain current, $I_{D,}$ by applying the following equation to the charging pulse:

$$dI = \frac{V_L \times dt}{L} \tag{2}$$

In Equation (2), there are two degrees of freedom available to the user: the inductance value (L) and the pulse time (dt). The V_{DS} value chosen by the user will be substituted into the equation in place of V_L. By carefully choosing a pair of L and dt values, the use can precisely control the I_D magnitude of the DUT at the end of the charging pulse; and therefore during turn-on and turn-off events.

2.2.1.2 Operating Conditions

The operating conditions used for CIL tests are generally chosen based on relevance for a particular application. However, operating conditions must also be chosen for generalized head-to-head device comparison tests and also for quantifying switching loss data in manufacturer data sheets. As it currently stands, there is no universal standard for the operating conditions used in such generalized comparisons.

CREE, ROHM, and ST Microelectronics are three manufacturers commercially-available of SiC MOSFETs at the time of this writing. Table 1 offers an example of summarized data sheet information from these three manufacturers that clearly exhibits the lack of standardization in the SiC MOSFET testing community [20][21][22].

	Operating Conditions			Switching Loss Data		
Manufacturer (Part Number)	Gate Resistor (Ω)	VDS (V)	ID (A)	Turn-on (μJ)	Turn-off (μJ)	Total (μJ)
CREE (C2M0080120D)	2.5	800	20	265	135	400
ROHM (SCT2080KE)	0	600	10	174	51	225
ST Microelectronics (SCT30N120)	6.8	800	20	500	350	850

Table 1 - Manufacturer Device Data Sheet Switching Losses Comparison

Since there is not a standard for quantifying and reporting switching loss metrics in SiC device data sheets, it is difficult for a design engineer to quickly decipher data sheet information and make a component selection. Looking at strictly the total switching losses column of Table 1 would suggest that ROHM produces the best (lowest switching loss) part. However, this device was evaluated at lower operating conditions than the others; so it may actually perform worse that the other parts under identical operating conditions. Furthermore, one might assume that CREE offers a significantly better part than ST Microelectronics since the V_{DS} and I_D operating conditions are the same and the CREE part has much lower switching loss figures. While this assumption is likely true, it is not a guarantee due to the fact that the CREE part was tested with a lower gate resistor value than the ST Microelectronics part. Later in the thesis, the significant effect that the gate resistor can have on switching losses will be discussed in further detail.

2.3 Special Considerations for WBG Devices

To this point, Chapter 2 has focused primarily on the theory for characterizing SiC MOSFET devices. Section 2.3 will shift the focus more toward the hardware considerations that the test engineer must observe in order to produce accurate and reliable data.

As the operating frequency of WBG devices enters the "Near RF" Domain as indicated in Figure 9, it becomes increasingly important for engineers to be conscious of side-effects associated with the fast-switching behavior of WBG devices [8][27][28]. Traditional devices such as the Si IGBT have switching times on the order of 1 us; whereas SiC MOSFET's can commutate an inductive load in as little as 10-20 ns. This implies a significant difference in the spectral content of the waveforms inherent in these two categories of systems. This difference means that all aspects of a WBG-based system must be designed with consideration for increased high-frequency spectral content, which usually extends into the VHF range, as shown in Figure 9. The implications of this paradigm shift have to be considered not only during component and system design, but also during the selection of metrology to instrument these systems, as will be discussed in the following sections of this thesis.

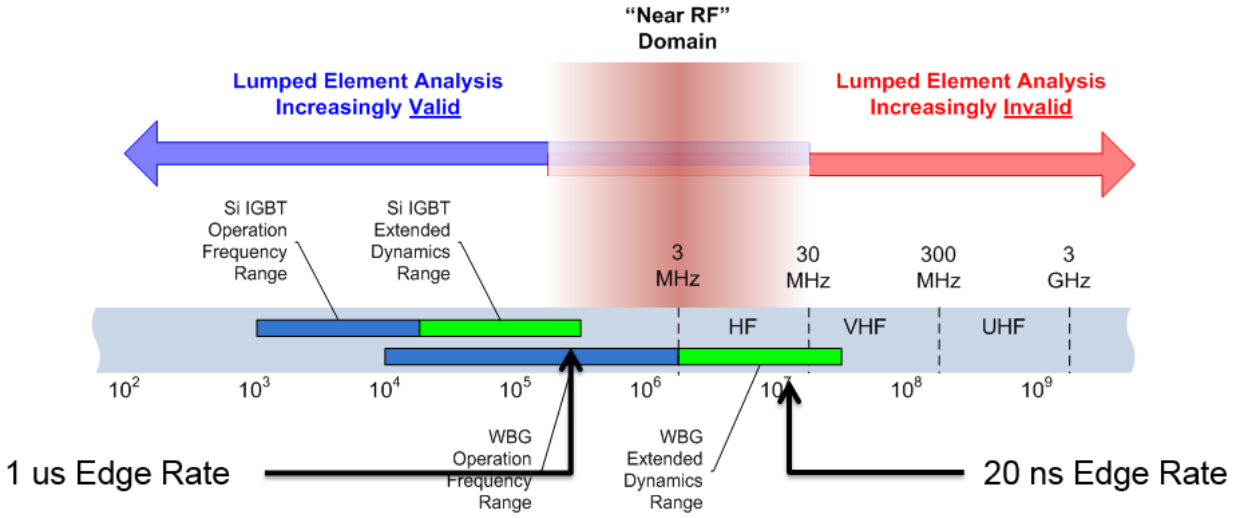

Figure 9 - WBG Operating Frequency Considerations

2.3.1 Test Circuit PCB Layout

The test circuit PCB is the foundation for obtaining valid testing results. It is responsible not only for the power flow but also the orientation and arrangement for the connection of measurement probes. Figure 10, which is a PCB layout view of the DUT adapter PCB featured in Figure 6 illustrates a streamlined PCB layout in which optimized power flow is achieved through wide power pours while also providing strategically placed measurement ports.

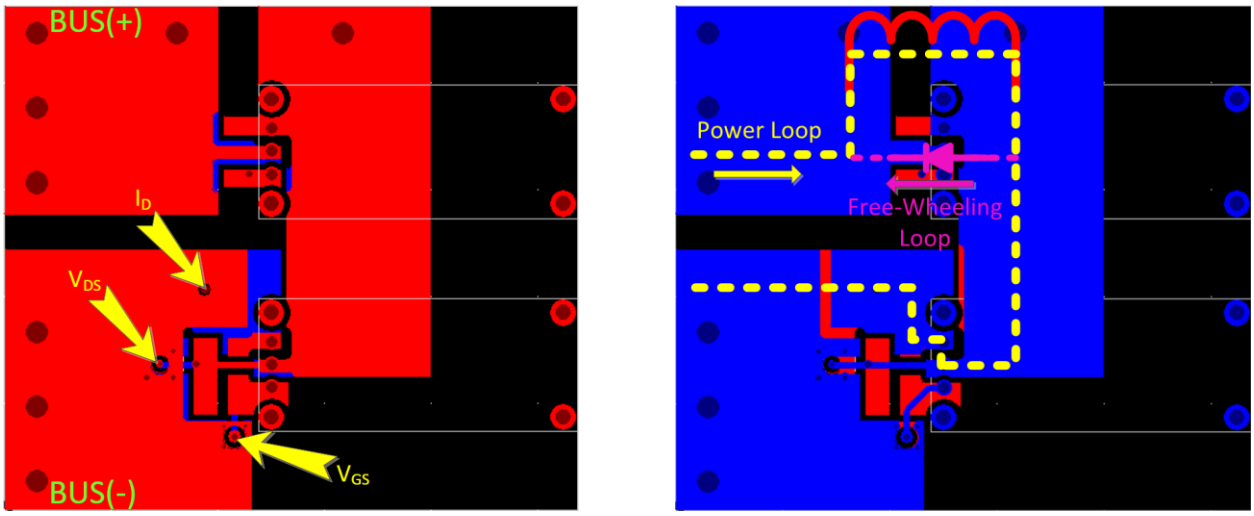

Figure 10 - DUT Adapter PCB Layout (Top and Bottom View)

When designing a DUT interface board of this nature, it is important to consider the spectral content of the signals which will be present in the CIL test circuit. As indicated in Section 2.3, the very fast signal edge rates produced by SiC MOSFET's result in "near-RF" spectral content which can easily excite resonances in parasitic elements of the test circuit and associated metrology. In order to mitigate this challenge, the interconnections between the DUT and other critical circuit elements should have as low equivalent series inductance (ESL) as possible. Ultra-low inductance connections are achieved by utilizing copper pours that are short and wide rather than narrow traces [23].

The PCB designer should also consider the proximity of signal traces to nodes that are subject to high dv/dt. Close proximity will result capacitive coupling which may be large enough to conduct substantial AC displacement currents across these unintended pathways. The magnitude of displacement current through any capacitor is proportional to the voltage rate-of-change across that capacitor ($I_C = C \cdot dV/dt$). Accordingly, the fast edge rates associated with SiC

MOSFET operation can cause even small parasitic PCB capacitances to conduct substantial displacement current.

By understanding this concept, it can be determined that traces in close proximity to nodes with high dv/dt can be subject to current perturbations on the signal trace. These current impulses can result in undesired noise on the signal traces that can affect measurement quality as well as circuit performance. To overcome this issue, the designer should strive to spatially isolate signal traces associated with the gate drive circuitry and measurement traces from the power loop of the DUT interface board.

2.3.2 Instrumentation

Now that proper PCB layout techniques have been discussed, this thesis will transition into the instrumentation requirements necessary to record accurate data during CIL tests. This section will focus on probe specifications, such as probe bandwidth, which an engineer should consider when selecting probes for a CIL test.

2.3.2.1 Voltage Probes

Figure 5 shows the CIL test circuit topology operating similar to a half bridge converter with the DUT in the lower position. Having the DUT in the lower position is an intentional design decision that allows the pertinent DUT voltage measurements, V_{GS} and V_{DS}, to be ground referenced measurement made by single-ended probes.

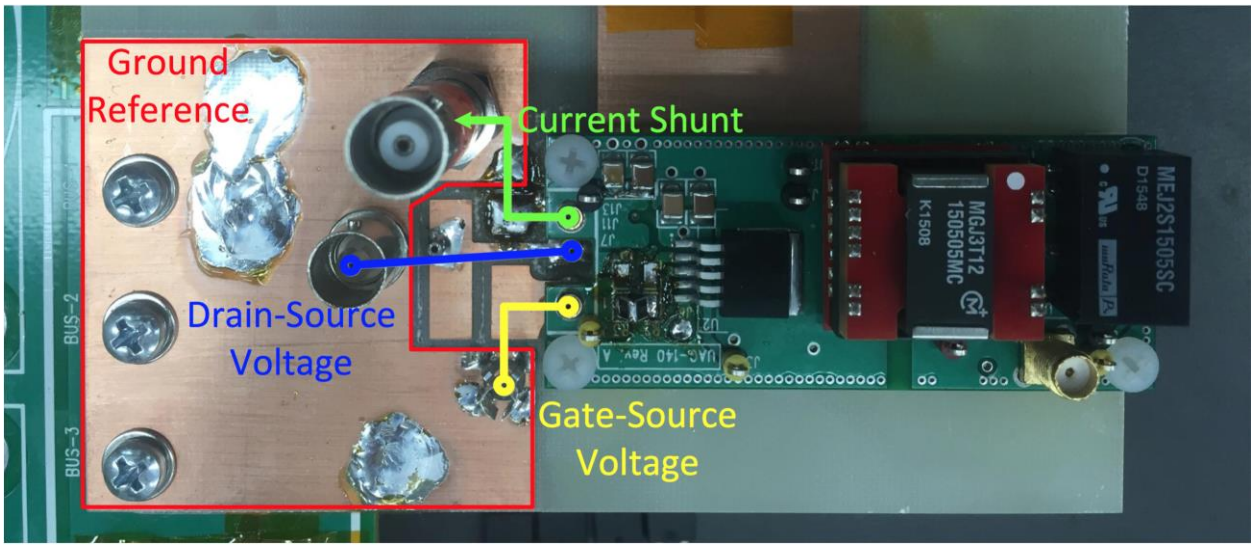

Figure 11 - PCB Mounted Ground Referenced Probe Interface Ports

This is a very important consideration, as it allows for the tightest probe connection possible whether it is a BNC connector for the V_{DS} measurement or probe-tip adapter for the V_{GS} measurement. Introducing additional loop inductance into the method for attaching the voltage probes, whether it is by a standard alligator clip ground wire or by the long leads on differential probes, is known to produce unreliable results with high-speed switching circuits [23]. The best method for mitigating this issue is to provide tight, low-inductance connections to the signals being monitored, by use of on-board connectors which are designed to mate with oscilloscope probes, as shown in Figure 12.

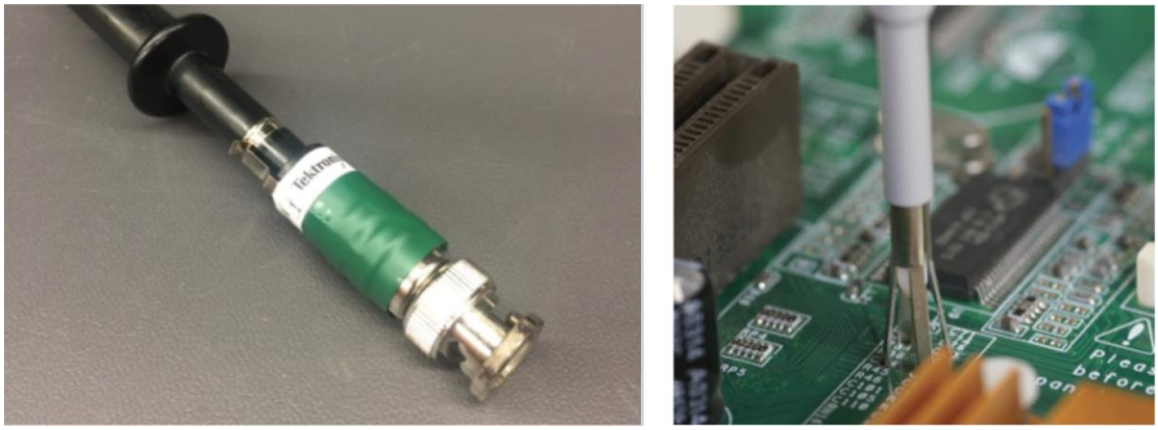

Figure 12 - Low Inductance Voltage Probe Attachment Methods

Another important consideration to make when dealing with SiC devices, which have extremely, fast rise and fall times, is adequate instrumentation bandwidth (BW). A common rule of thumb states that instrumentations BW in GHz should exceed $0.25/T_R$, where T_R refers to the rise time of the monitored signal in nanoseconds. However, researchers have shown that up to five or ten times this baseline requirement is necessary in order to adequately preserve the amplitude and phase of the measured signal, respectively [24]. Thus, for a SiC MOSFET with a 5 ns voltage rise-time, a minimum instrumentation BW of 500 MHz is needed.

2.3.2.2 Current Probes

Unlike voltage probes, current probes involve an intrusive technique to monitoring the DUT. This paper will consider two different approaches to measuring the drain current, I_D, during a CIL test.

2.3.2.2.1 Current Transformer

Today, high-bandwidth, instrumentation-grade Current transformers (CTs) are available which allow for pulse-current monitoring during CIL tests. The circuit branch under test is passed

through the aperture of the CT, and the measurement port is attached to the input of an oscilloscope. The oscilloscope measures the voltage potential across the internal CT terminating resistance and then the voltage measurement is converted back to a current value mathematically and displayed by the oscilloscope. This method for obtaining device drain current waveforms is common in practice [25] and offers the advantage of galvanic isolation, which leads to the ability to monitor currents anywhere in the CIL test circuit. This feature is particularly useful when load inductor or free-wheeling diode current monitoring is desired. However, there are two disadvantages to this approach. The first is that this type of current probe is incapable of measuring DC currents (which is generally not a problem for CIL testing, provided that the pulse sequence is sufficiently short). The second and more important disadvantage that this probe presents is the choke point in the DC bus that must be implemented in order to pass the current through aperture of the device.

2.3.2.2.2 Current Viewing Resistor

Another popular technique for monitoring the drain current of the DUT during a CIL test utilizes a current viewing resistor (CVR) in the form of a coaxial shunt. The method for inserting this device into the CIL test circuit involves splitting the Bus(-) node from the source node of the DUT. The device is then inserted in series to connect the two previously mentioned nodes back together via a small, high precision resistance. This technique allows for a high BW ground-referenced voltage probe to be used to measure the voltage across the resistive shunt. That voltage is then mathematically converted to a current by the oscilloscope.

Like the current transformer discussed in the previous section, this technique offers a few disadvantages as well. Because this device must be inserted in series with the DUT, it adds a small amount of extra parasitic impedance that otherwise would not be present in the circuit. These devices also have a limited capacity for absorbing pulsed energy. Also, similar to current transformers, this method involves inserting a choke point for the current flow in the circuit.

2.3.2.2.3 Current Probe Summary

Figure 13 shows a side-by-side implementation of the two current measurement techniques discussed in this chapter. Both methods require the test circuit to be altered for measurement. However, note that the current transformer requires an additional wire loop to be inserted into the circuit and through the aperture of the CT. This wire loop is a significant source of parasitic inductance, which is undesirable for the reasons already stated.

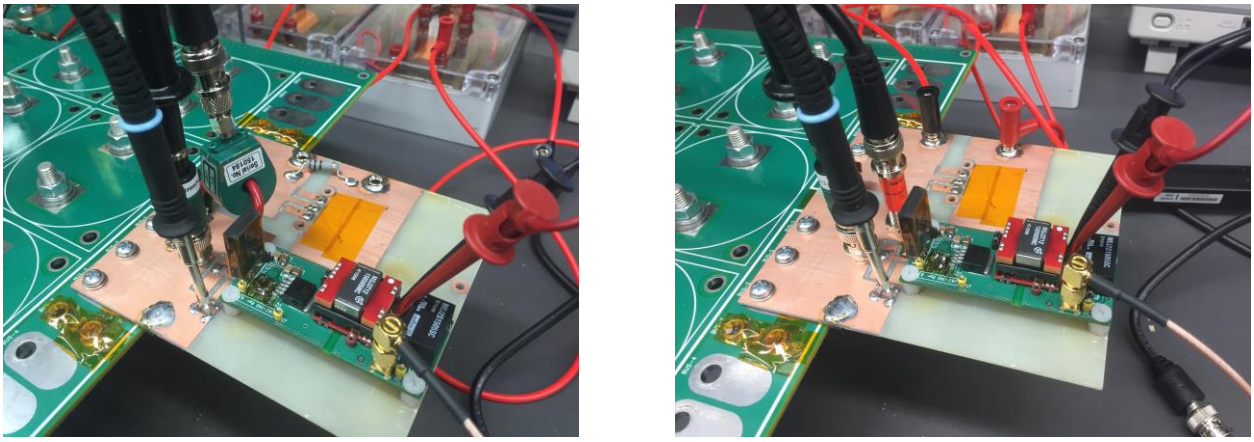

Figure 13 - Current Transformer (left) and Coaxial Shunt (right) Implemented on DUT Adapter PCB

2.3.3 Proper De-skew

Now that the instrumentation to produce adequate CIL test results with SiC devices has been established, this thesis will discuss an important software configuration that must be accounted

for in order to accurately separate turn-on and turn-off switching losses. The term de-skew refers to the alignment of the V_{DS} and I_D waveforms such that their relationship on the oscilloscope depicts their relationship in the circuit. Often times, there exists an amount of latency on one oscilloscope channel or another that causes the waveforms to be misaligned. This misalignment leads to a shift in switching losses from turn-on to turn-off or vice versa depending on the misalignment direction.

Figure 14 presents the circuit used to perform the de-skew procedure. This circuit, including the DUT adapter PCB, is identical to the circuit and adapter PCB used for CIL testing (Figure 5 and Figure 10) with the only exception being the resistor that is substituted into the circuit in place of the inductive load bank and free-wheeling diode.

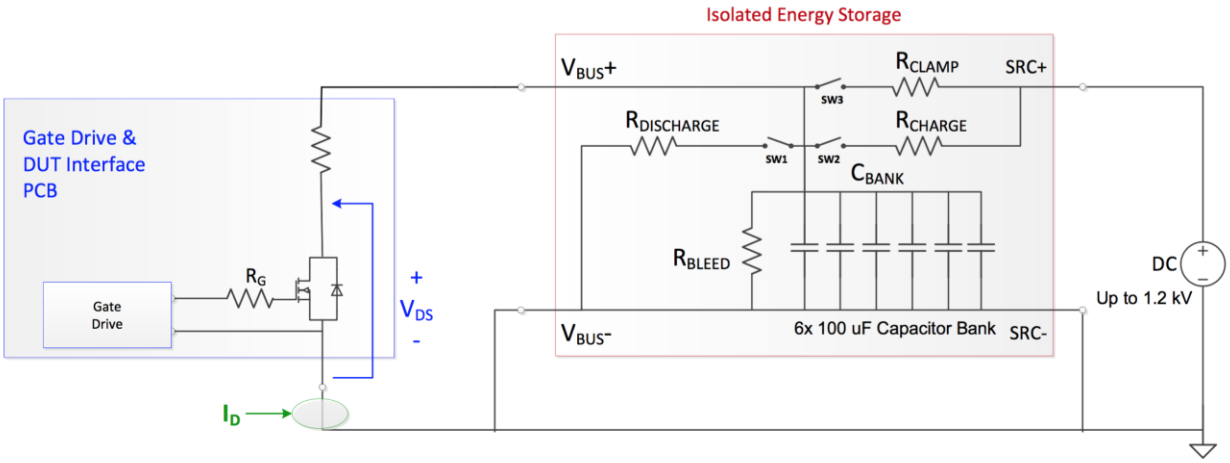

Figure 14 - CIL Test Deskew Circuit

To perform the de-skew procedure, the test engineer triggers the DUT exactly the same as he or she would in a normal CIL test. The same DUT measurements, V_{DS} and I_D, are taken and projected on the oscilloscope. Next, the test engineer creates a math function into the

oscilloscope to represent the "ideal" current waveform, which is predicted based on the voltage across the load resistor used. This math function implements the following expression:

$$I_{Deskew} = \frac{V_{BUS} - V_{DS}}{R} \quad (3)$$

Where:

R: the resistor value used (typically ~10Ω)

V_{BUS}: the bus voltage at which the test was performed (typically ~200V)

The resulting "ideal" current waveform, representing I_D, is in perfect phase alignment with the measured V_{DS} waveform. The measured current, I_D, should then be shifted in phase until it matches as closely as possible the "ideal" current waveform. At this point, the measured I_D should be in time-agreement with the V_{DS} waveform.

Figure 15 depicts a comparison between each of the previously mentioned current measurement techniques. From the image, it can be determined that the coaxial shunt measurement technique produces a "sharper" current edge which is more suitable for alignment with the "ideal" or reference current waveform. This will allow more accurate tuning of the de-skew parameter, and will ultimately provide improved reliability and accuracy of the subsequent switching loss measurements.

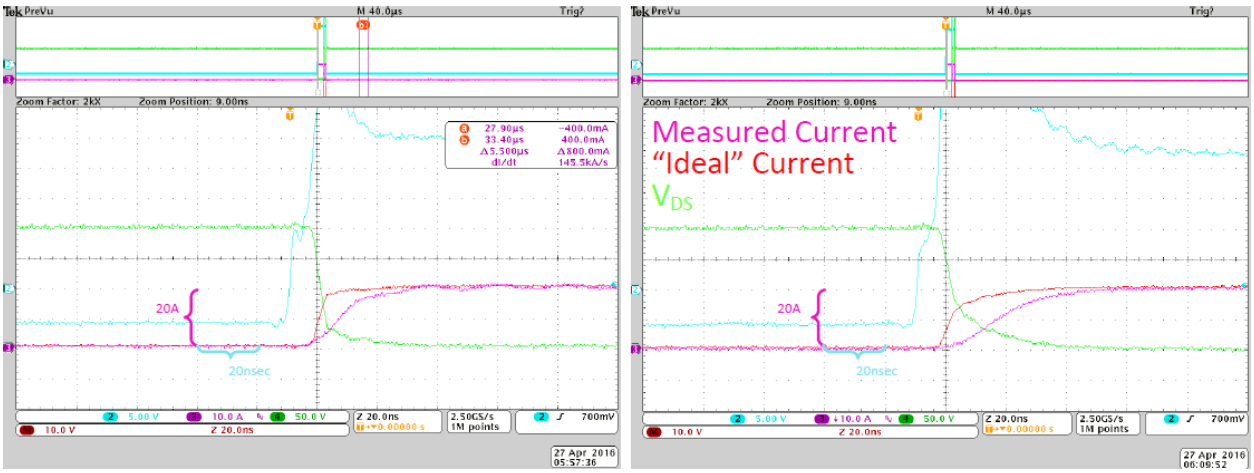

Figure 15 – Coaxial Shunt (left) and Current Transformer (right) Deskew Comparison

2.4 Processing Results

After all measures discussed in the previous sections of this chapter have been accounted for, the test engineer can be confident in the data that is collected during a CIL test. The raw data collected during these tests can be processed in a number of ways. One method involves using MATLAB to extract the data, plot the waveforms, and calculate the switching losses.

2.4.1 Effect of Gate Resistor Value on Switching Losses

Earlier in this thesis it was mentioned that the external gate resistance employed in the gate-drive circuit plays a significant role in determining the switching performance of the DUT. A large gate resistance will limit the current into the gate of the part and will limit the rate at which the gate capacitance will charge. The effect that variation in the gate resistance has on the switching performance of a DUT can be seen in the following figures. The conditions for these test procedures were: V_{BUS} = 800V and I_D = 20A.

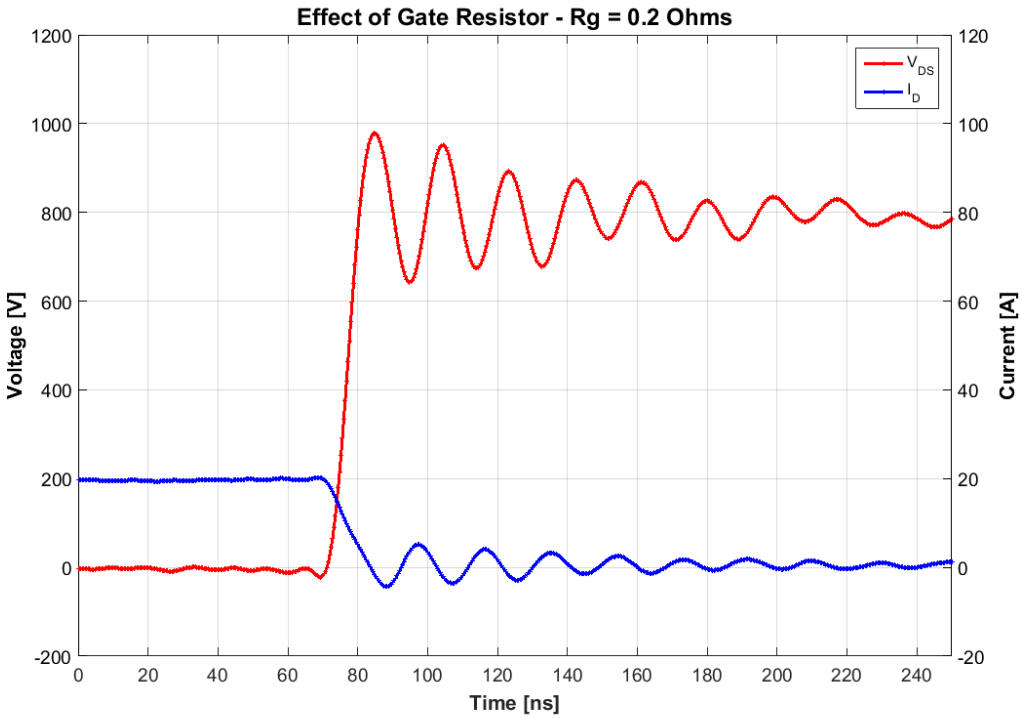

Figure 16 -Effect of 0.2Ω Gate Resistor during Turn-Off

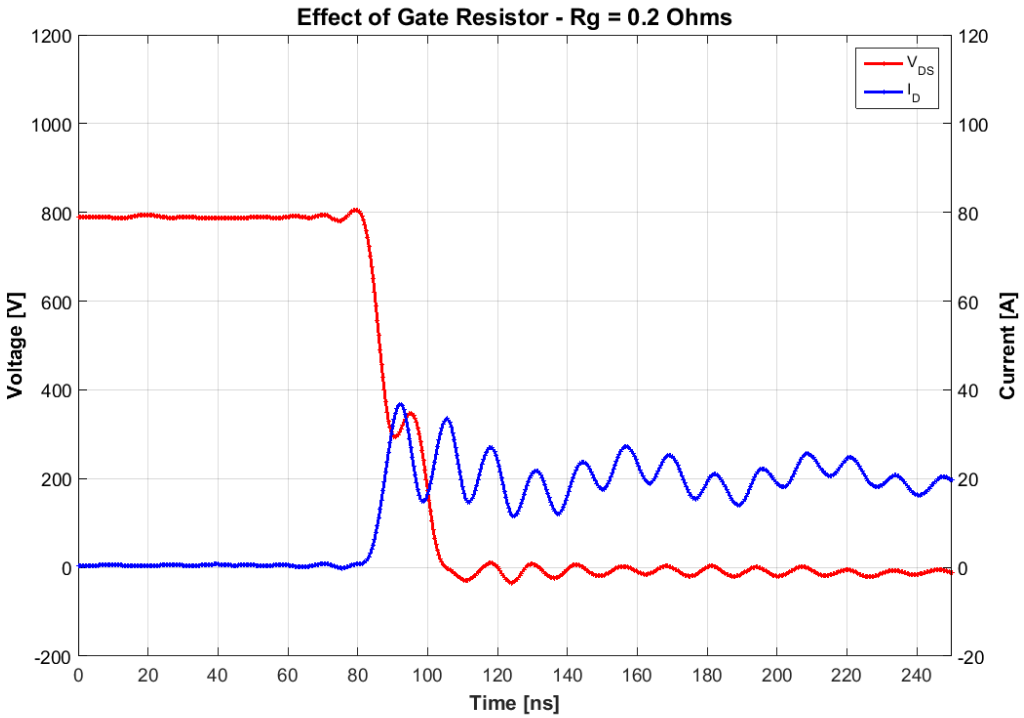

Figure 17 - Effect of 0.2Ω Gate Resistor during Turn-On

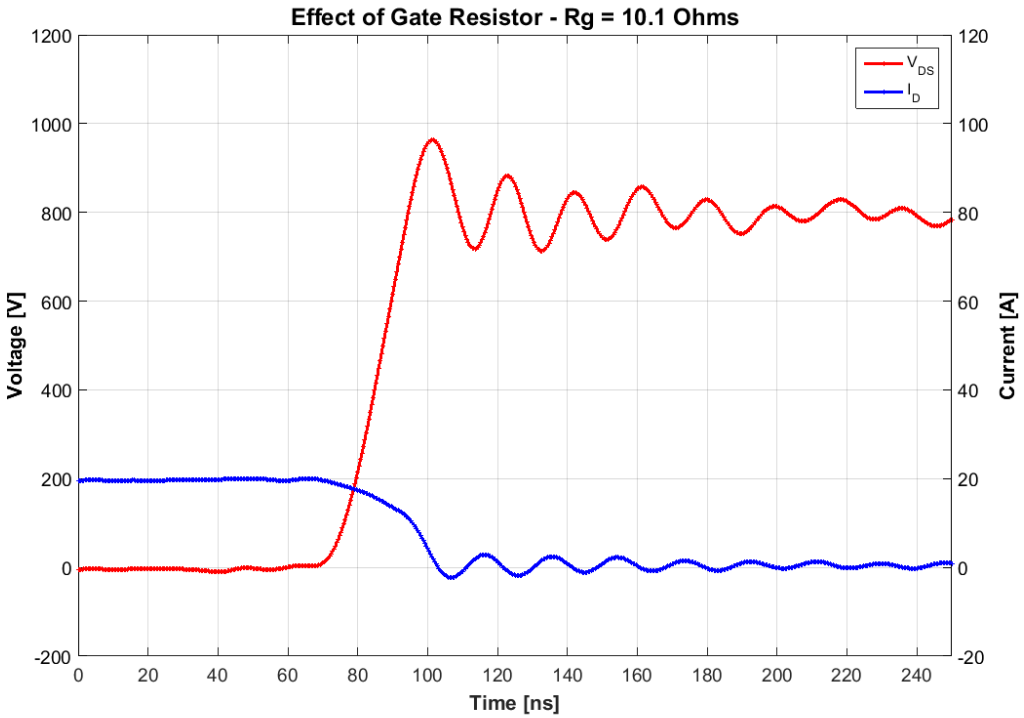

Figure 18 - Effect of 10.1Ω Gate Resistor during Turn-Off

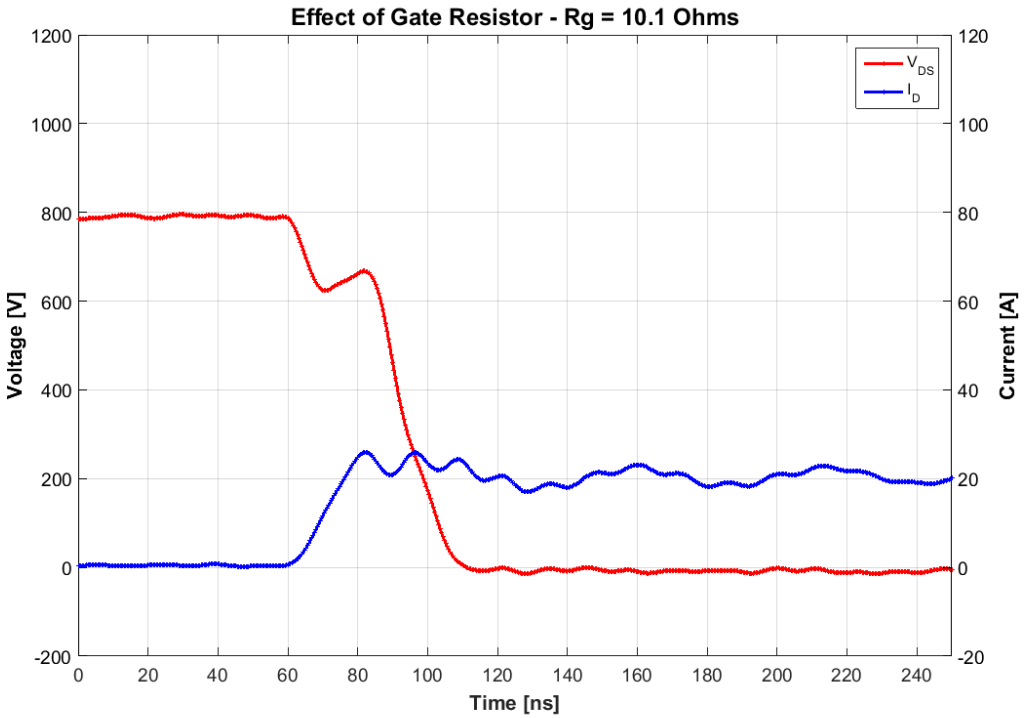

Figure 19 - Effect of 10.1Ω Gate Resistor during Turn-On

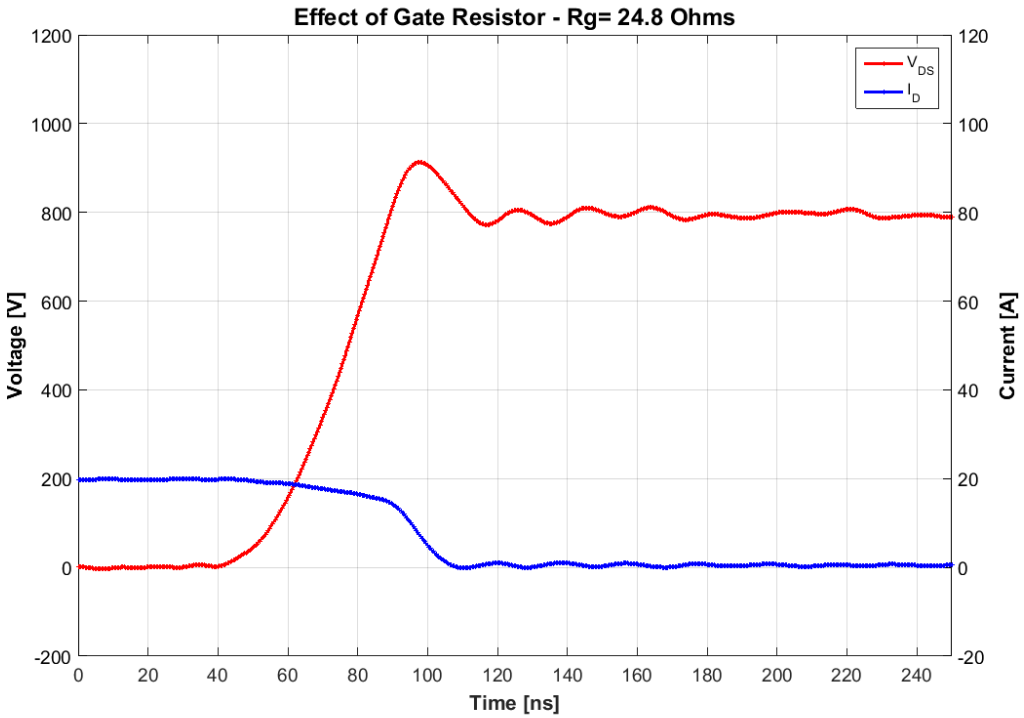

Figure 20 - Effect of 24.8Ω Gate Resistor during Turn-Off

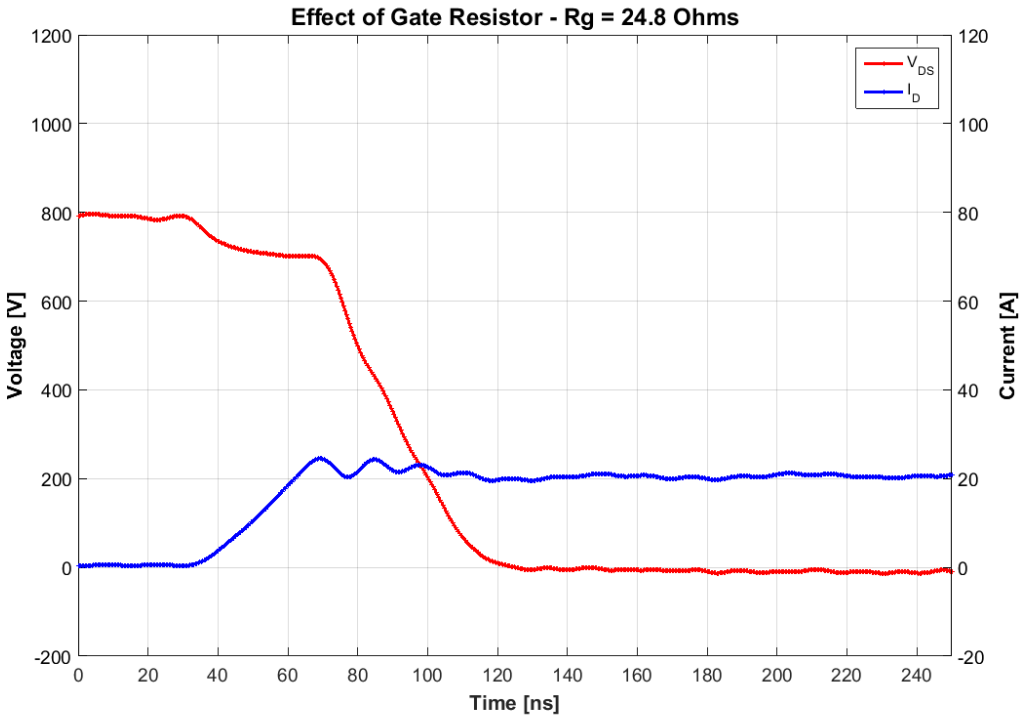

Figure 21 - Effect of 24.8Ω Gate Resistor during Turn-On

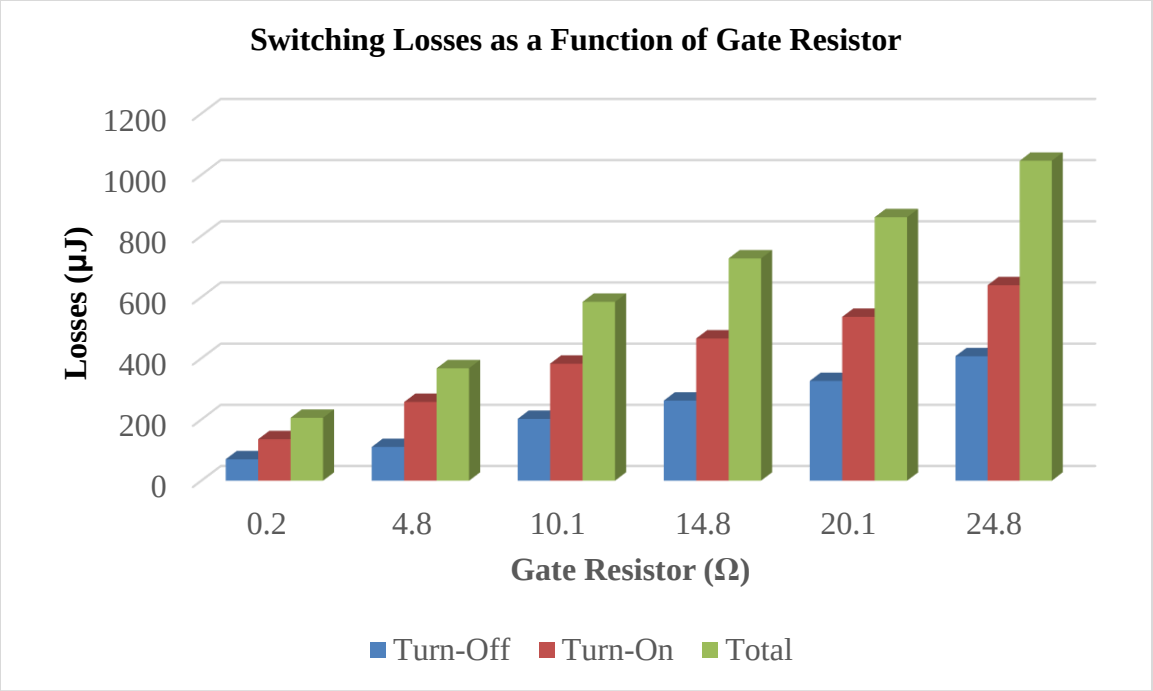

Figure 22 – Switching Losses as a Function of Gate Resistor Values

2.4.2 Limits of Integration

One topic that is a subject for debate when quantifying switching losses in a CIL test is the method for setting the limits of integration for which the losses are calculated. There is no universal standard for setting these limits. Some researchers set the limit at the first zero crossing, while others set the limit at the first rising-edge zero crossing. For the current work, the limit of integration was set to a wider timeframe, when both waveforms have reached steady state. This was done to ensure that the switching loss estimates do not include the contribution of any energy temporarily stored in the bus inductance or switch output capacitance, as discussed in [29]. An example of how the limits of integration can influence switching loss results can be seen in Figure 23. For this test the waveforms for the 10.1 Ω gate resistor in Figure 18 and Figure 19 were considered. In this case, the point at which the waveforms exhibited the peak instantaneous energy was taken as a point of reference. From this point the starting limit of

integration was fixed at constant time period before the reference point. The stopping limit of integration was then altered in terms of time after the reference point to reflect the data shown below in Figure 23. As the figure indicates, varying the limits of integration by as little as 50 nsec can influence the switching losses on the order of 10 μJ.

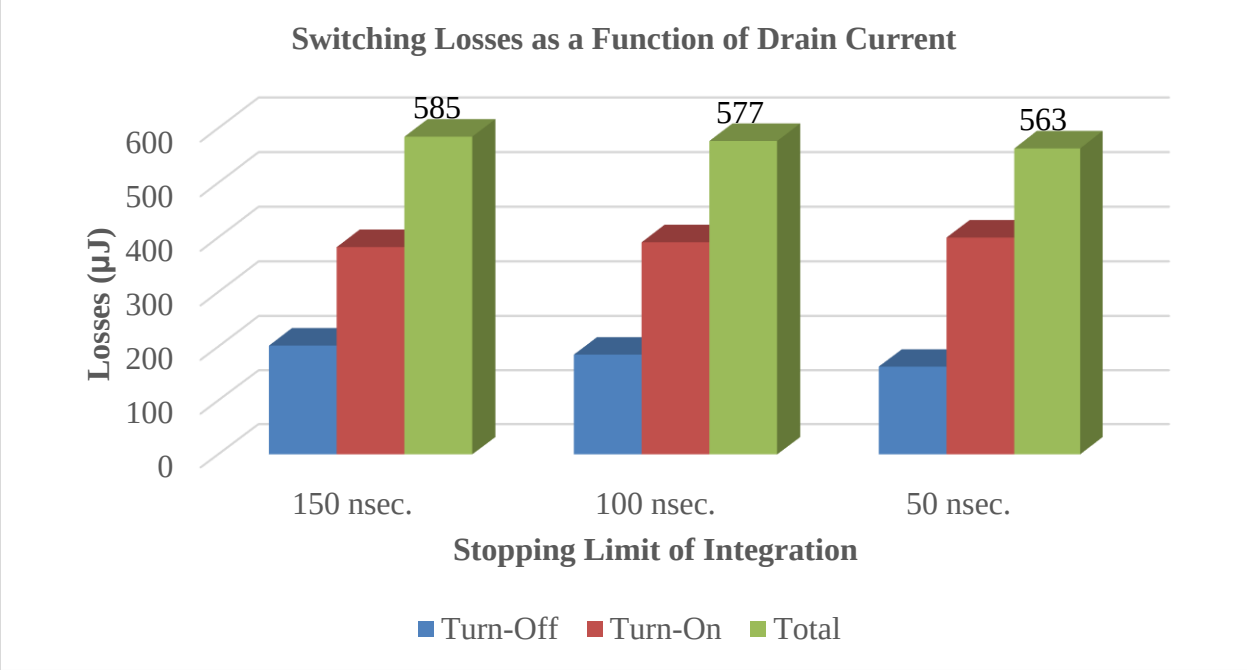

Figure 23 - Effect of Integration Limits on Switching Loss Quantification

CHAPTER 3

CONVERTER DESIGN

This thesis has discussed SiC MOSFETs as a higher performance alternative to comparable Si devices. Theoretical comparisons have been made based on intrinsic device properties inherited from the semiconductor material used to construct them and the structure of the devices. Static and switching measurements were then presented in order to support these comparisons. In order to further validate claims that SiC devices are superior to Si devices in terms of performance, this thesis will present an application design in which the devices are interchanged within a DC-to-DC converter under identical operating conditions.

3.1 Power Stage Design

This section will discuss the motivation for certain design decisions made with respect to the power stage of the converter under consideration. The topology selection of the converter will be discussed as well as a set of specifications that allow the converter to be envisioned in a real world application. A method for selecting converter components based on design specifications will be presented along with the considerations to be noted when implementing these components in a PCB design.

3.1.1 Topology Selection

The topology selected for the DC-to-DC converter presented in this thesis is a hard-switched non-isolated buck converter, as shown in Figure 24.

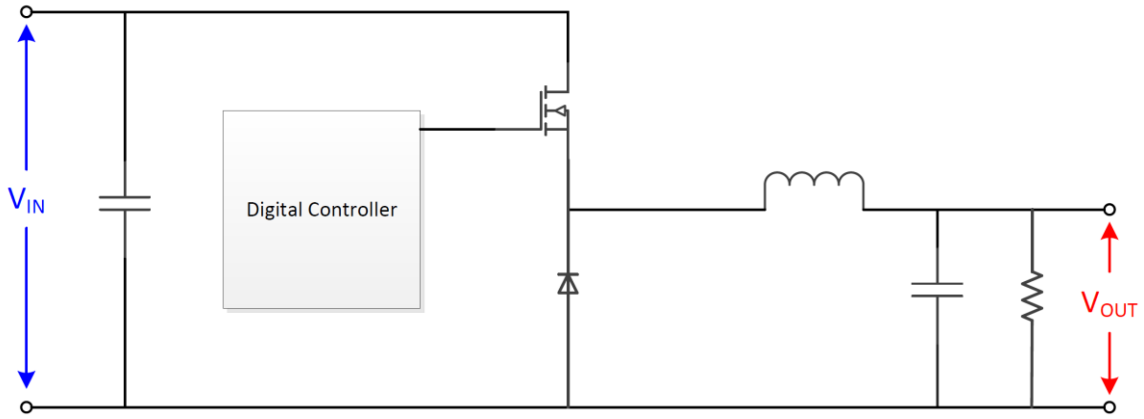

Figure 24 - Hard Switched Non-Isolated Buck Converter Topology

This topology was selected for two primary reasons. First, a power stage of this type is inherently stable due to the absence of any right half plane zeros. As a result, it is typically easier to design a control stage for a buck converter than any other converter topology. This converter will explore the use digital control techniques in an attempt to elevate converter performance under specific operating conditions; consequently, any simplification based on plant selection is desired. Secondly, the converter was designed to demonstrate the performance of the SiC semiconductor devices under consideration. Limiting the number of components and striving for circuit simplicity allowed for the DUT performance metrics to be more easily quantified.

3.1.1.1 Application Example

High-level design and performance specifications for the DC-DC converter under consideration are presented in Table 2. Note that the combination of input voltage and switching frequency operating conditions for this converter place it squarely in the SiC MOSFET quadrant according to Figure 1.

Condition	Value
Input Voltage ($V_{In,Nominal}$)	675V
Output Voltage ($V_{Out,Nominal}$)	350V
Power Range	1kW-5kW
Switching Frequency (f_{SW})	100kHz-200kHz
Dynamic Response	Near Critically Damped

Table 2 - DC-to-DC Buck Converter Specifications

The chosen converter topology and operating specifications for this application design were not arbitrary. This converter was designed to emulate a real world application that is in common use in data centers. According to the Natural Resources Defense Council (NRDA), in 2013, U.S. data centers consumed an estimated 91 billion kilowatt-hours of electricity, equivalent to the annual output of 34 large (500-megawatt) coal-fired power plants [16]. Improving power conversion processes in data centers by increasing converter efficiency will lead to lower overall power consumption and lower operating cost, not to mention the positive environmental impact.

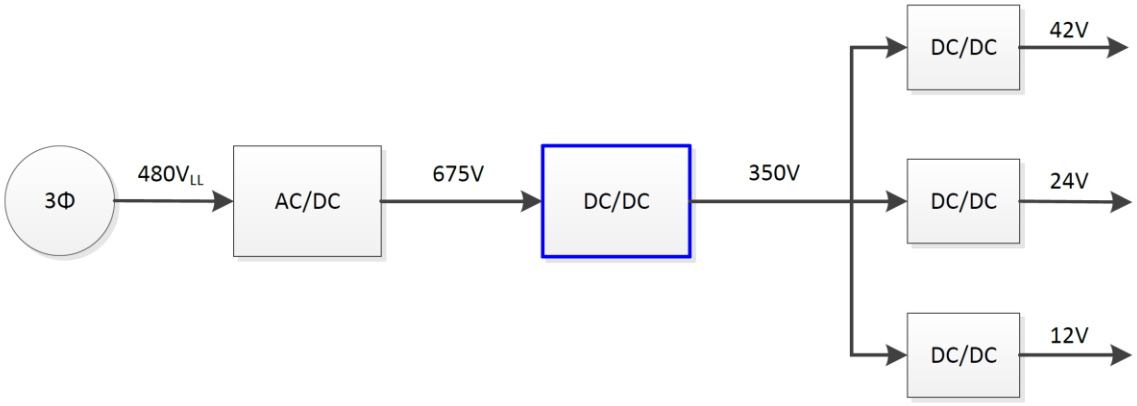

Figure 25 – Notional Data Center Power Conversion Process

Figure 25 offers a high level view of a notional data center power distribution network. In this network, an AC/DC converter converts the 3-phase 480V_{LL} input to a regulated 675V DC output. The DC/DC converter that is being designed for this application, highlighted with a blue outline, then converts the 675V DC input into a 350V DC output, which is a standard DC distribution voltage used to supply power to cabinets containing point-of-load DC-DC converters and the server hardware itself.

3.1.2 Component Selection

There are many resources containing step-by-step instructions for selecting component values for the basic buck converter topology shown in Figure 24 [12]. This section will provide the detailed approach that the author took in selecting components for the converter under discussion.

3.1.2.1 Inductor Selection

It is well known that the design of hard-switched DC-DC converters typically begins with the selection of the inductor [9]. As such, it is appropriate that the inductor selection process should be discussed first. When selecting any component, the designer should ensure the component

would operate as intended at both extremes of the operating spectrum during steady state. In this design, there are two parameters that have associated operating ranges, the power range (1kW-5kW) and the switching frequency (100 kHz-200 kHz). The maximum average current rating of the inductor should be determined using Equation (4). The minimum inductance value necessary to keep the converter in CCM can be determined using Equation (5).

$$I_{Max,Avg} = \frac{P_{Pou,Max}}{V_{Out,Nominal}} \tag{4}$$

$$L_{Min} = \frac{\left(V_{In,Nominal} - V_{Out,Nominal}\right) \times \frac{1}{f_{SW,Min}} \times D}{2 \times \frac{P_{Out,Min}}{V_{Out,Nominal}}} \tag{5}$$

Using the values supplied by the specifications within Table 2, the maximum average current that the inductor in this design should be able to accommodate is approximately 14.3A. Following a similar procedure, the minimum inductance value needed for this design is determined to be approximately 295µH. A custom-wound 350µH was chosen as the inductor for this design. The inductor was wound using 12AWG magnet wire and a toroid shaped distributed air gap core based on a high-frequency-capable ferrite material from Magnetics Inc. [11]. The 12AWG wire is suitable for current up to 20A with a maximum temperature rise of 60 ºC [1]. The core's material properties specify that this material will begin to saturate at a flux density of 600-700 mT; the converter design in question will operate the core at a maximum flux excursion of approximately 393 mT, which is well within the capabilities of this inductor. This will allow for the converter to operate at rated current without risk of inductor saturation.

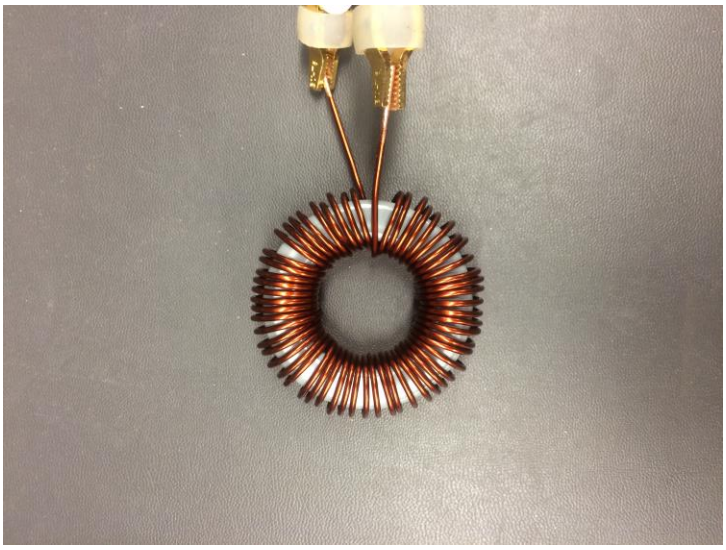

Figure 26 - Custom Wound 350 μH Inductor

3.1.2.2 Output Capacitor Selection

Output capacitor selection is based on the peak-to-peak ripple current produced by the previously selected filter inductor as well as the desired maximum output voltage ripple. The current through the inductor can be visualized as a combination of a DC component and an AC component. The DC component is the average value of the current waveform and what is ultimately delivered to the load. The function of the output filter capacitor is to filter off the small signal (AC) component of the inductor current so that only the DC component remains. Equation (6), taken from [12], represents the minimum output capacitance needed to satisfy the specified output voltage ripple.

$$C_{out(\min)} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{out}} \tag{6}$$

ΔI_L, as previously discussed, is a function of the voltage being applied across the inductor as well as the time period that it is being applied. The largest applicable value for ΔI_L should be used in this equation in order to appropriately size the output capacitor. For this case, the resulting value for ΔI_L is approximately 5.5A. Substituting this value into Equation (6) along with a switching frequency of 100 kHz and a maximum output ripple voltage of 1V yields a minimum output capacitance of 6.89µF. In order to mitigate any additional output voltage ripple caused by the output capacitor ESR and to ensure adequate overhead, this design implemented a 10µF output capacitor network comprised or ten individual 1µF capacitors in parallel, each having a 10mΩ ESR. Assuming that all the paralleled capacitors are nearly equal in capacitance value, the AC current should divide equally between them, resulting in an effective output capacitor ESR of approximately 1 mΩ.

3.1.2.3 Input Capacitor Selection

The function of the input capacitor network is to supply energy to the system in short bursts, as demanded by the converter as energy is added to the output filter during the switch-on interval of each switching period. This prevents the need for the input power supply to source these high-frequency current pulses through a long conductor, which can result in substantial ringing and oscillation of the input voltage. In order to prevent this and to alleviate some of the stress to the input voltage supply, a reservoir of energy is created by the input capacitors, which is drawn from during the switch-on intervals. The energy reservoir is subsequently refilled during the off period of each switching cycle, such that the "average" power component is provided by the input source, while the "ripple" component is provided by the input filter. While the output capacitor network is typically comprised of low ESR ceramic capacitors, the demands of input

capacitor network typically require a different component type. Due to the need for high-voltage rating and substantial energy storage in a small volume, this filter is ideally comprised of metal film capacitors, which when compared to electrolytic capacitors have much lower ESR.

As has already been mentioned, the primary function of the input capacitor network is to supply extra power to the system during times of need. Therefore, the precise values of the input capacitors are not critical so long as they have the capacity to store an adequate amount of energy. In the case of this design, two 5μF film capacitors were used in parallel to create a 10μF input capacitor network.

3.1.3 Board Layout

When laying out a PCB such as that required for the implementation of the converter considered here, there are several design principles that should be adhered to in order to ensure optimal operation. These practices include but are not limited to:

i. Large area pours for power flow instead of traces.
ii. Linear power loop design.
iii. Mirrored power pours to optimize current flow.
iv. Feedback voltage dividers sampled for control purposes should be secluded from high dv/dt areas of the PCB.

3.1.4 PCB Implementation of Power Stage

By adhering to the design specifications presented earlier in this chapter and carefully following proper component selection and PCB layout techniques, the author was able to take a paper

design for the converter in question and develop this design into a fully functioning power stage prototype, as shown in Figure 27 and Figure 28. Note the low inductance copper pour interconnections for each node. These pours optimize power flow on both sides of the PCB by utilizing cross stitching vias around their borders. Furthermore, the PCB is also arranged such linear power flow is achieved by component organization that allows power to enter the PCB on one end and exit on the opposite end.

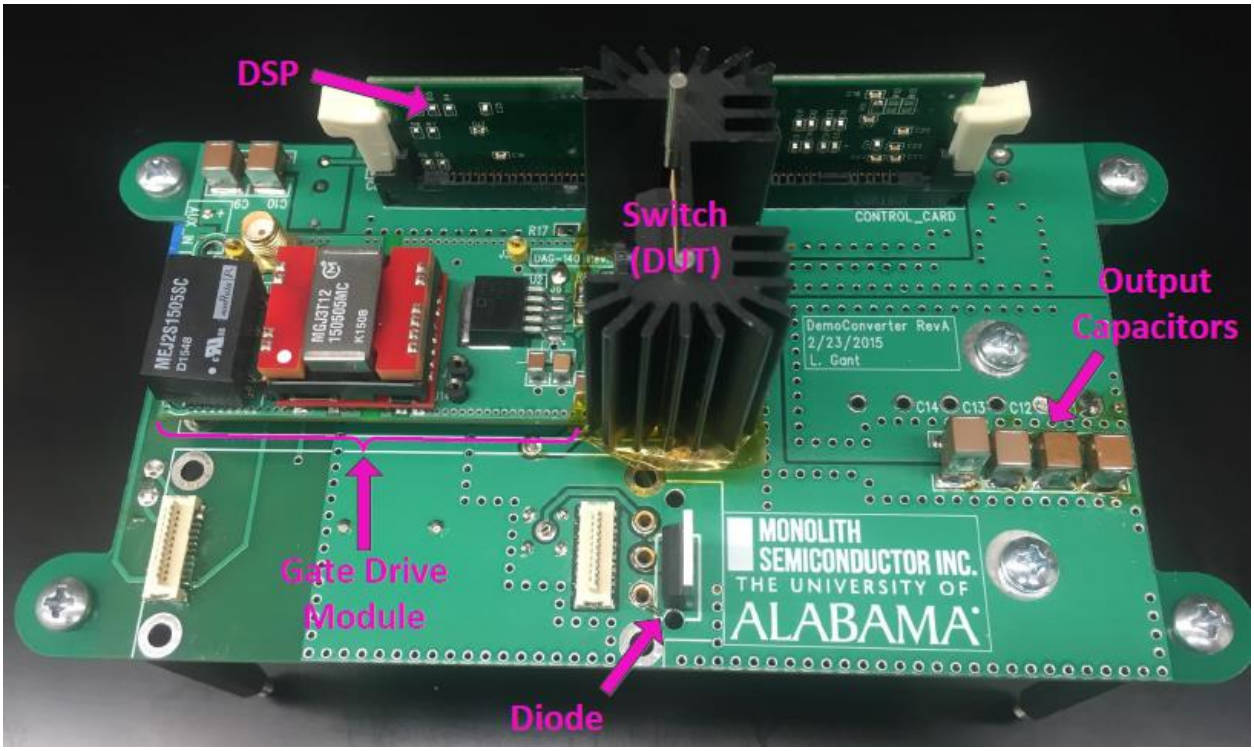

Figure 27 - Fabricated Power Stage PCB (Top)

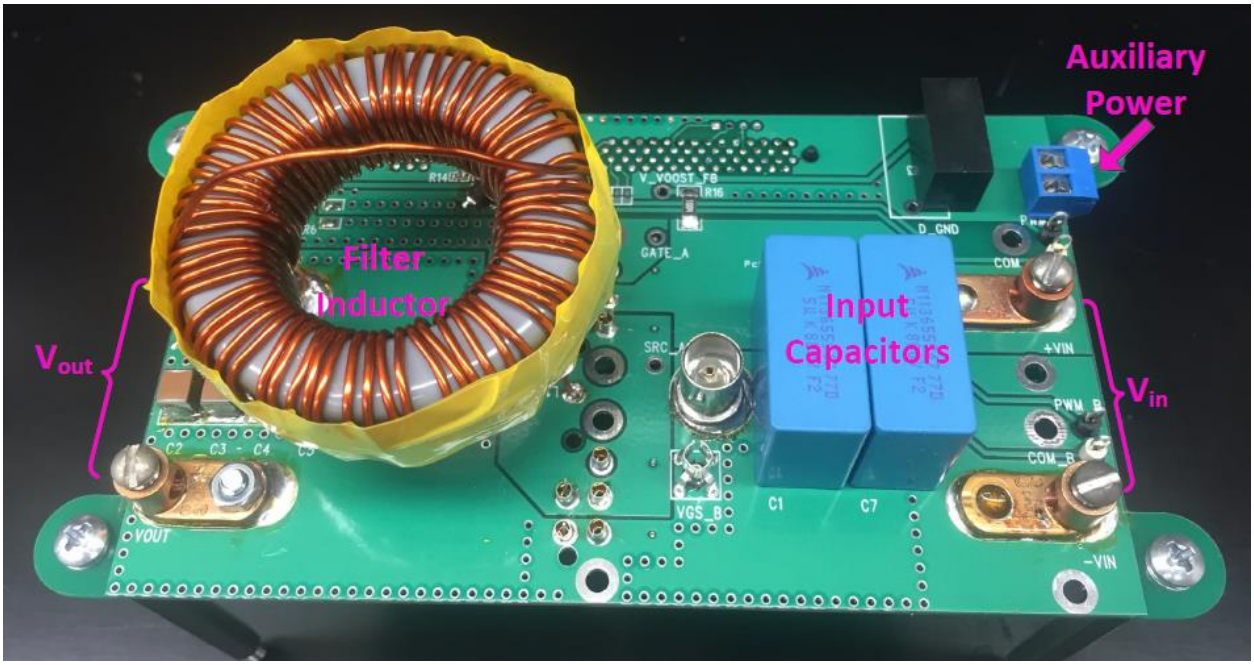

Figure 28 - Fabricated Power Stage PCB (Bottom)

CHAPTER 4

CONVERTER CONTROLLER DESIGN

Because this converter was designed not only to show the stark contrast between Si and SiC devices, but also to show the versatility of the SiC devices, a digital controller was deemed necessary. This section will demonstrate the procedure for designing a digital compensator based on the type-three analog compensator presented in [13].

4.1 Open-Loop Transfer Function

In order to begin the design process for the compensator, the system for which the compensator is being designed should first be modeled appropriately. To do this, a system level block diagram, shown in Figure 29, was constructed to represent each element considered in the design process. Each of the components in this system diagram will be explained in the following sections.

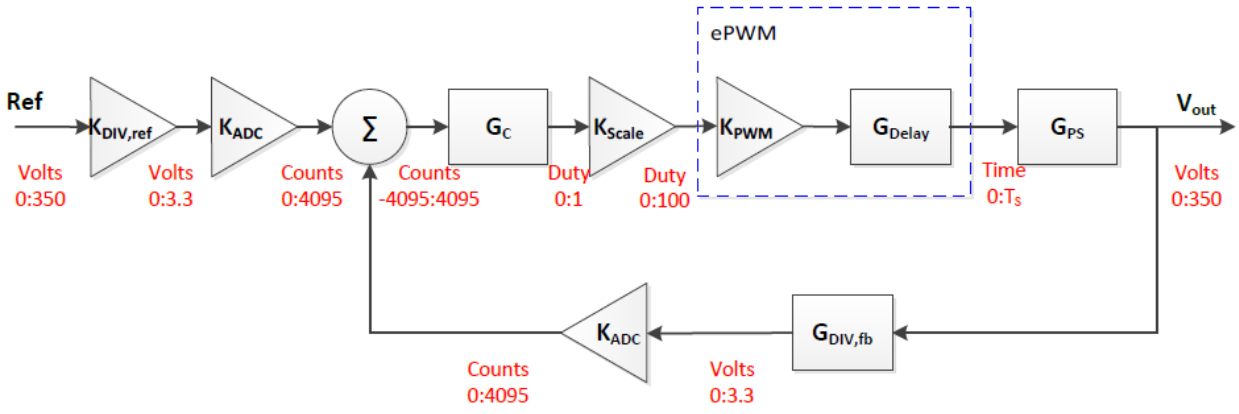

Figure 29 - System Level Block Diagram of DC-to-DC Buck Converter

The next step in the compensator design process involves breaking the closed-loop system in order to create one open-loop linear transfer function that this thesis will refer to as $G(s)_{OL}$.

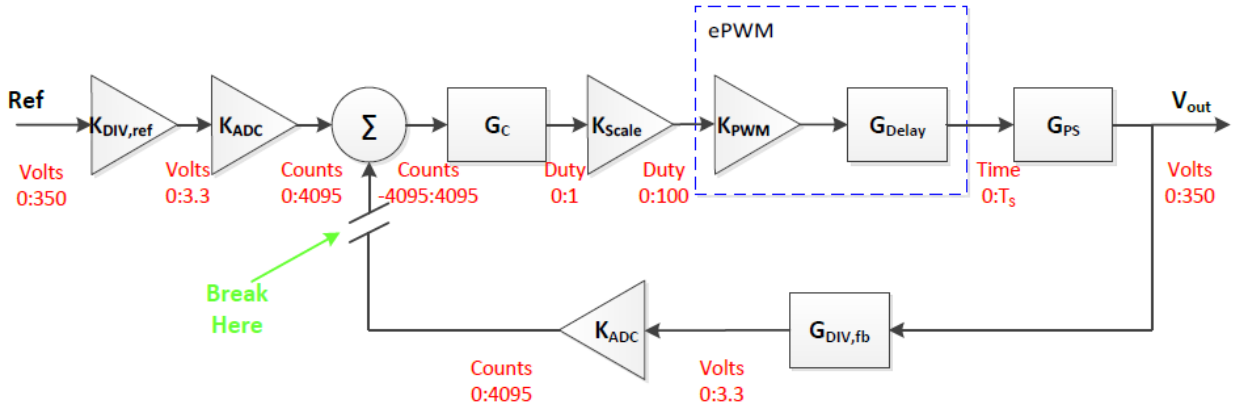

Figure 30 - System Level Block Diagram with Closed-Loop Break Location

Figure 30 denotes the location in which the closed-loop system should be broken. Equation (7) represents the transfer function of the open-loop system that will be used to design the type-three compensator.

$$G(s)_{OL} = G(s)_C \times K_{Scale} \times K_{PWM} \times G(s)_{Delay} \times G(s)_{PS} \times G(s)_{DIV,fb} \times K_{ADC} \qquad (7)$$

It should be noted that the reference branch gain blocks ($K_{DIV,ref}$ and K_{ADC}) are pre-scale values used to simplify the programming of the reference value for the user. Thus, these gain values are not included in the open-loop transfer function since they are not part of the "loop gain" presented to the controller.

Now that an open-loop transfer function has been established, the next step is to assign values to each of the blocks represented in the Equation (7).

4.1.1 Plant Transfer Function

The plant transfer function, $G(s)_{PS}$, is defined by the power stage elements of the converter. This transfer function, taken from the literature [9], was determined to be:

$$G(s)_P = \frac{V_{in}}{LC} \frac{1 + srC}{s^2 + s\left(\frac{1}{RC} + \frac{r}{L}\right) + \frac{1}{LC}} \tag{8}$$

Where:

R: Load Resistance (122.5Ω for 1kW and 24.5Ω for 5kW)

C: Output Capacitor Value

L: Inductor Value

r: Output Capacitor ESR

It should be noted that the ESR of the output capacitor is a significant contribution to the overall system behavior, since it introduces a high-frequency zero into the plant transfer function.

4.1.2 Scale Gain

The Scale Gain, K_{Scale}, is necessary in this design in order to properly condition the input to the ePWM function block used in the programming integrated development environment (IDE) for the digital signal processor (DSP). When designing a compensator of this nature, the output of the compensator transfer function is typically in the range of 0 to unity (0-1). However, the input of the ePWM block requires an input of 0-100. In order accommodate an internal gain of 100 within the ePWM block, a gain block of 0.01 was factored into the open-loop transfer function.

$$K_{Scale} = 0.01 \tag{9}$$

4.1.3 PWM Delay

The PWM Delay, $G(s)_{Delay}$, refers to the delay introduced by the PWM modulator, which can be described as the amount of time from the DSP sampling instant until the instant when the duration of the output pulse is completely determined. For this design $G(s)_{Delay}$ was modeled as a half cycle Padé Approximation [14]. This value, although it is an over estimate, is commonly used in this situation for a PWM delay element. Further investigation to determine the precise delay value based on controller characteristics may improve the system performance but this estimate will serve as a reasonable starting point.

$$G(s)_{Delay} = \frac{1 - s\frac{T_S}{4}}{1 + s\frac{T_S}{4}} \tag{10}$$

4.1.4 Feedback Divider

The purpose of the Feedback Divider, $G(s)_{DIV,fb}$, is to step down the output voltage to a suitable level for the DSP analog to digital converter (ADC) to sample. The ADC used in this work has a sampling voltage range of 0-3.3V. The output voltage of the converter is nominally 350V. A 1 MΩ and a 4.7 kΩ resistor were used to form the resistor divider network for this application. A 1 nF capacitor was also used in parallel with the 4.7 kΩ resistor in order to suppress high-frequency noise which appears at the node from which the ADC voltage is sampled. Equation (11) represents the resulting feedback divider transfer function, including the contribution of this low-pass filter and the scaling of the voltage divider, as shown in Figure 31.

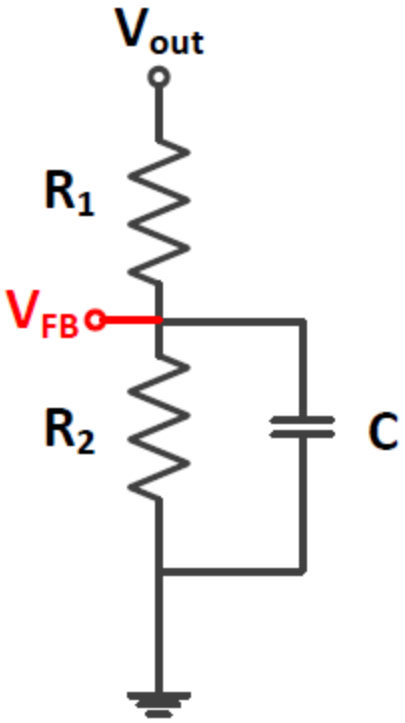

Figure 31 - Feedback Voltage Divider Network

$$G(s)_{DIV,fb} = \frac{R_2}{R_1 + R_2 + R_1 R_2 C s} \tag{11}$$

Where:

R1: 1 MΩ

R2: 4.7 kΩ

C: 1 nF

4.1.5 ADC Gain

The ADC Gain, K_{ADC}, is inversely related to the ADC resolution of the DSP. The DSP ADC in this application has a resolution of 12-bits. Applying this resolution to the ADC range, 0-3.3V, results in a static gain block represented by Equation (12).

$$K_{ADC} = \frac{1}{V_{ADC,Res}} = \frac{1}{805.8\mu V} = 1241 \tag{12}$$

4.1.6 PWM Gain

The PWM Gain, K_{PWM}, is specific to the particular DSP being used. In a digital controller based on a DSP, this value can usually be determined by inspecting the range of values established by the timer structure which underlies the PWM function. However, in the case of this design, the value for the PWM gain was unknown due to the high-level of abstraction associated with the MATLAB interface used to program the DSP, as discussed later. In order to determine this value, an experimental procedure was performed. Figure 32 illustrates the foundation on which the experimental theory was based.

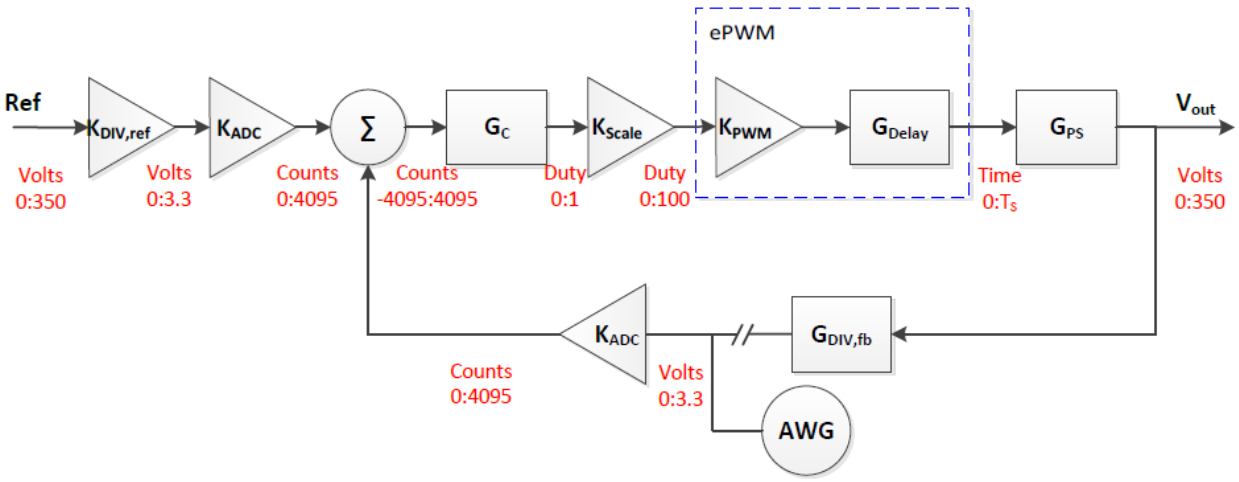

Figure 32 - System Level Block Diagram with AWG Feedback Signal

In this experiment, the feedback path for the ADC was physically broken. In its place, an arbitrary waveform generator was inserted in order to simulate the feedback voltage with a superimposed small signal fluctuation. By monitoring the small-signal perturbation present in the output voltage created by this small-signal perturbation in the feedback voltage during this experiment, it was possible to empirically estimate the transfer function $\frac{\widetilde{V_{OUT}}}{\widetilde{V_{FB}}}$. For this experiment, the controller transfer function, $G(s)_C$, was chosen to be unity. By doing this, all blocks in the system level diagram shown in Figure 32 were known with the only exception being K_{PWM}. (Note K_{Scale} was chosen to be 1 for this experiment)

For the next step in the experiment, the converter was given an input voltage of 50V and the AWG was set to supply the DSP ADC an average value equal to that of the programmed reference. Superimposed on the AWG signal was a small signal perturbation. The frequency of this perturbation was adjusted in finite steps ranging from 100 Hz to 10 kHz. The AWG waveform was observed along with the output waveform, V_{out}, using two separate oscilloscope

channels. From these waveforms, the overall system gain and phase delay, at each perturbation frequency, could be determined. The gain was estimated by dividing the output waveform peak-to-peak value by the AWG waveform peak-to-peak value. The phase was estimated by measuring the time delay between the input signal (AWG perturbation) and the output signal (V_{OUT}) and converting the result to units of degrees. An example of the waveforms described above that were collected using an oscilloscope can be seen below in Figure 33, where the AWG waveform is represented in green and the output waveform is represented in blue.

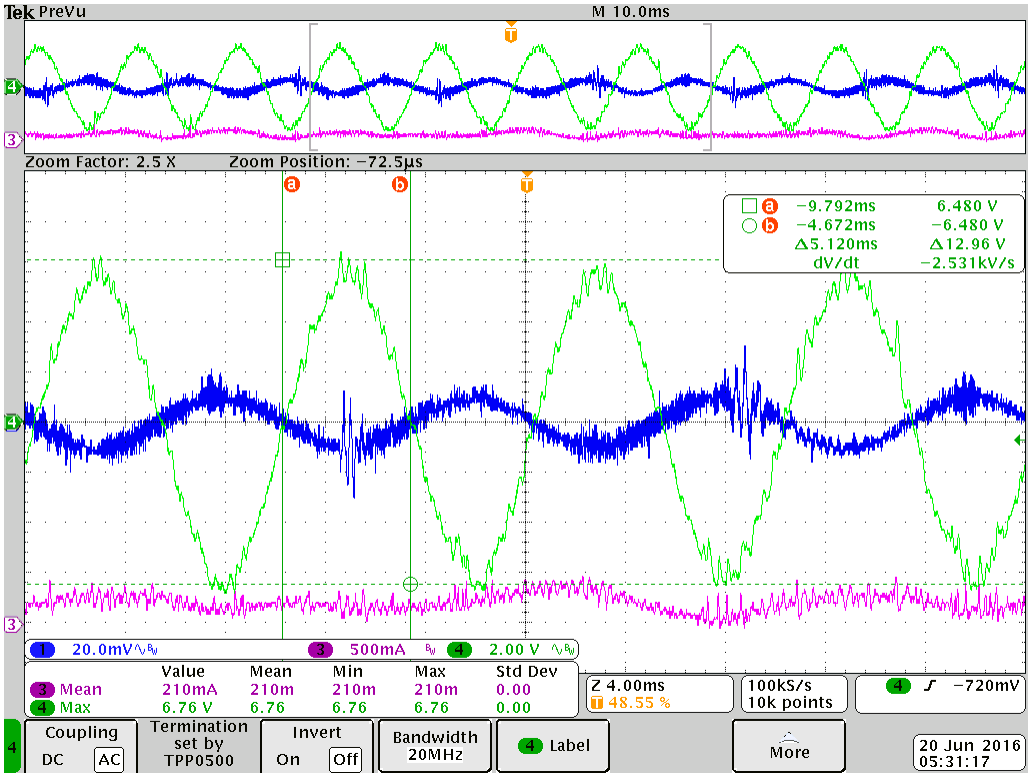

Figure 33 - K_{PWM} Experimental Waveforms for 100 Hz Perturbation

Next, the system gain values collected through experimentation were compared to the system gain values produced through simulation assuming the PWM gain value was unity. A Bode magnitude plot was created using MATLAB as a method for visual comparison, shown here as Figure 34.

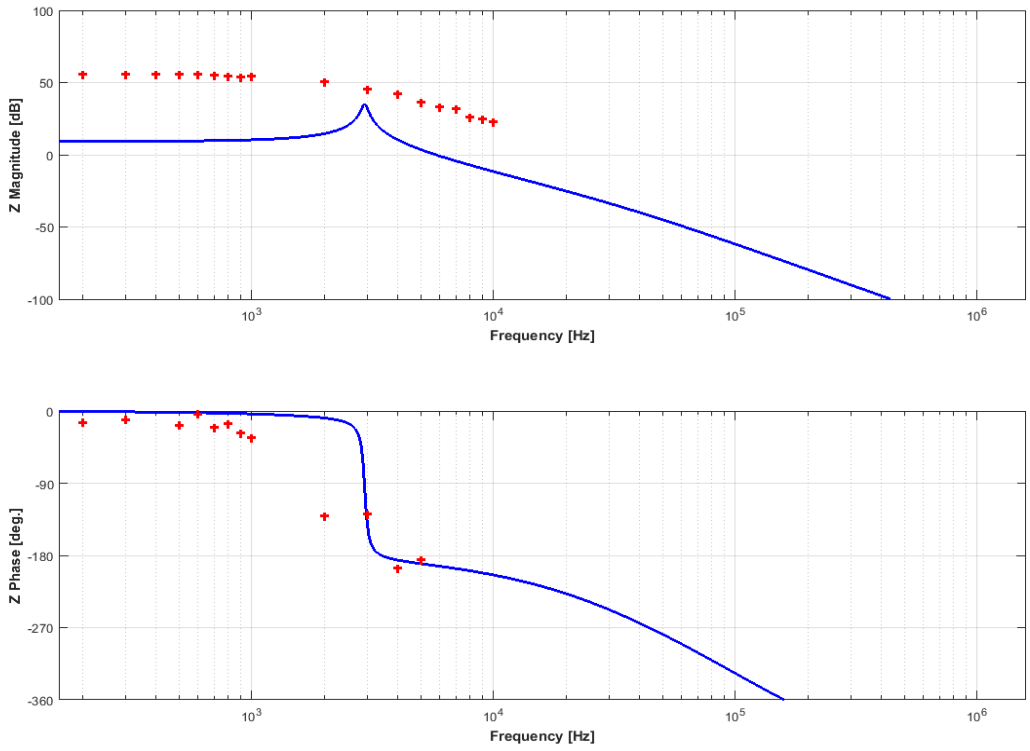

Figure 34 - Bode Magnitude Plot of Experimental vs. Simulation Results

By knowing all block values represented in Equation (7) other than K_{PWM}, the next step in the experiment was to adjust the value for K_{PWM} in the simulation until the simulation Bode magnitude plot was aligned with the experimental Bode magnitude plot. The result of assigning K_{PWM} a value of 0.0098 is visible in Figure 35.

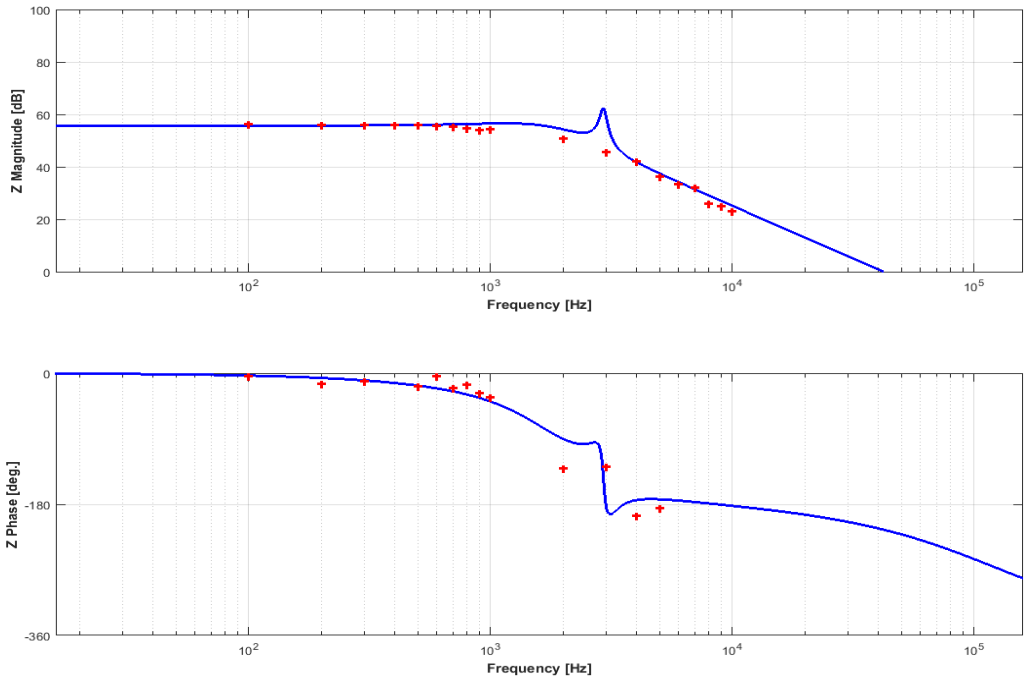

Figure 35 - Bode Magnitude Plot of Experimental vs. Simulation Results after Modification of K_{PWM} Value

Thus, the value of K_{PWM} was experimentally determined to be:

$$K_{PWM} = 0.0098 \tag{13}$$

4.2 Open-Loop frequency Response

Now that Equation (7) has been populated with the values discussed above, the next step in the controller design process begins by plotting the complete open loop transfer function, $G(s)_{OL}$. Figure 36 depicts the frequency response of the system via a Bode magnitude and phase plot for the system's open loop transfer function. In the next few sections of this thesis, this figure will be used as the basis for designing a compensator suitable for this application.

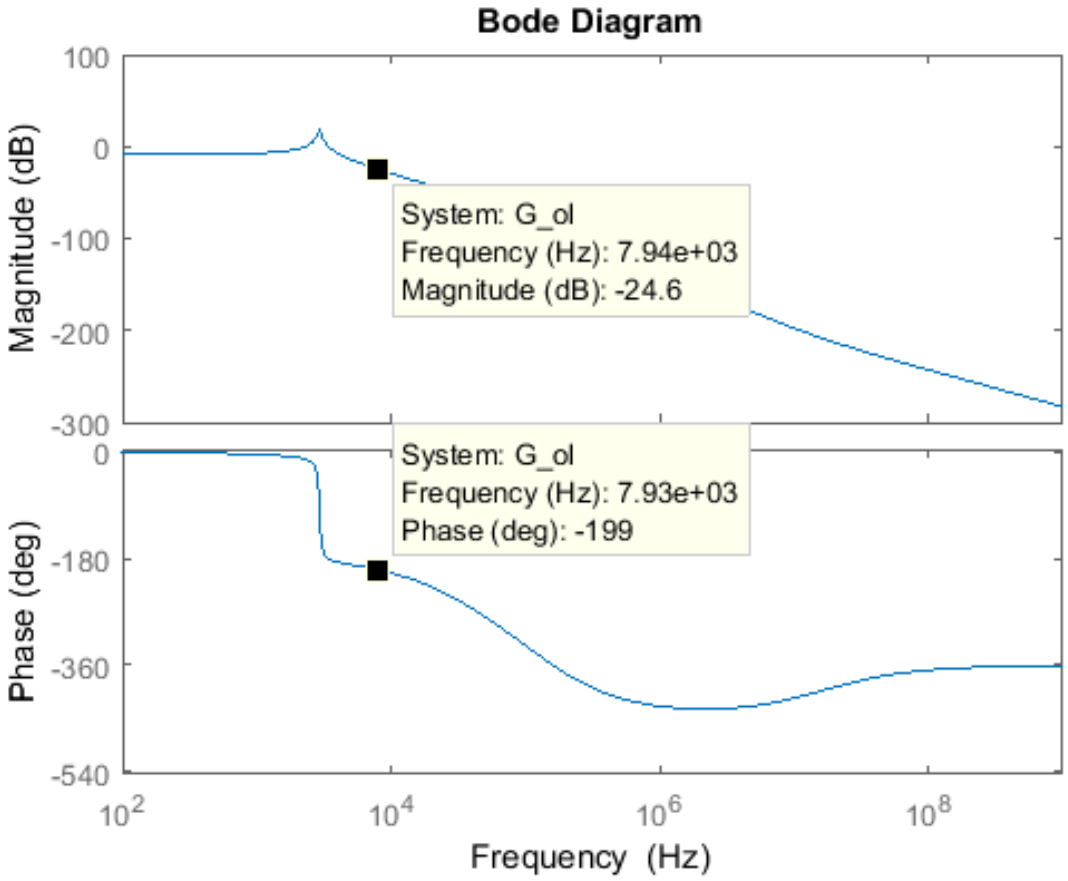

Figure 36 - Open-Loop Bode Plot Before Compensation

4.3 Compensator Design

There are many different types of compensators which can be employed in feedback control systems (i.e. PID, lead, lag, etc.). Each type of compensator has unique characteristics that may make it the most suitable for a particular application. In this example, a type-three compensator was chosen and designed using the k-factor approach [13]. This analytical design approach allows the designer to specify a crossover frequency and desired phase margin, and the K-factor method calculates the location for a paired set of poles and zeros in order to establish the desired system characteristics. This thesis will give a high-level explanation for the design process of the

controller for this system. A more detailed explanation for the continuous time type-three compensator design process and the equations involved can be found in [9].

4.3.1 Design in Continuous-Time

It was established previously that this system will implement a DSP as means of feedback control. One common method for designing a digital controller is to first design the controller in the continuous time domain and then convert the resulting s-domain transfer function into a z-domain transfer function using one of severable available discretization methods.

When designing a compensator for DC-to-DC converters, three system characteristics described by the Bode plot should be observed to ensure bounded-input, bounded-output (BIBO) stability and reasonable dynamic performance:

1) The crossover frequency should be selected at a frequency such that it has adequate bandwidth to manage the LC resonance of the system while also remaining unaffected by the switching frequency of the converter. A common rule of thumb used in this application is to ensure the crossover frequency is at least five times lower than the switching frequency (i.e. for a converter with a 200 kHz switching frequency, a crossover frequency less than 40 kHz should be selected).
2) The phase of the system should have adequate margin at the selected crossover frequency so as to provide a properly damped response during the dynamic events.
3) The phase angle of the system should not pass below -180° at any frequency below the selected crossover frequency.

A type three compensator has the general form represented by Equation (14).

$$G(s)_C = \frac{k_c}{s}\frac{\left(1 + {}^{s}/_{\omega_z}\right)^2}{\left(1 + {}^{s}/_{\omega_p}\right)^2} \tag{14}$$

The Bode plot presented in Figure 36 suggests that the LC resonance of the system occurs at approximately 3 kHz. Accordingly, 8 kHz was chosen as a desired crossover frequency. This crossover frequency allows for a timely dynamic response while also satisfying the requirements in the list above. The desired phase margin targeted in this design exercise was 50º. After using the k-factor design approach for a type-three compensator presented in [9] to obtain the values for k_c, ω_z, and ω_p, the resulting compensator transfer function is represented by Equation (15).

$$G(s)_C = \frac{0.7841}{s}\frac{\left(1 + {}^{s}/_{4450.5}\right)^2}{\left(1 + {}^{s}/_{718520}\right)^2} \tag{15}$$

4.3.2 Conversion to Discrete-Time

Since this converter is implemented via a digital control strategy, the compensator transfer function was converted into its equivalent discrete time transfer function. For the exercise, this conversion was performed by hand utilizing the Backward Euler technique. This techniques involves replacing the 's' variables in the compensator transfer function with the expression shown in Equation (16).

$$s = \frac{z - 1}{zT_S} \tag{16}$$

Where:

s: continuous-time transfer function variable

z: discrete-time transfer function variable

T_S: sampling period

In this case, the author made use of MATLAB's $c2d()$ function with a sampling period, T_S, of 5µs to create the equivalent discrete time transfer function, $G(z)_C$. The output of this process is presented in Equation (17).

$$G(z)_C = \frac{36z^2 - 69.16z + 33.19}{z^3 - 1.13z^2 + 0.1342z - 0.00421} \tag{17}$$

The resulting complete open-loop transfer function after the implementation of the designed controller is presented in Figure 37 with markers denoting the selected crossover of 8 kHz. Note that the gain value and phase margin represented in this figure correspond to the target values presented earlier in this chapter.

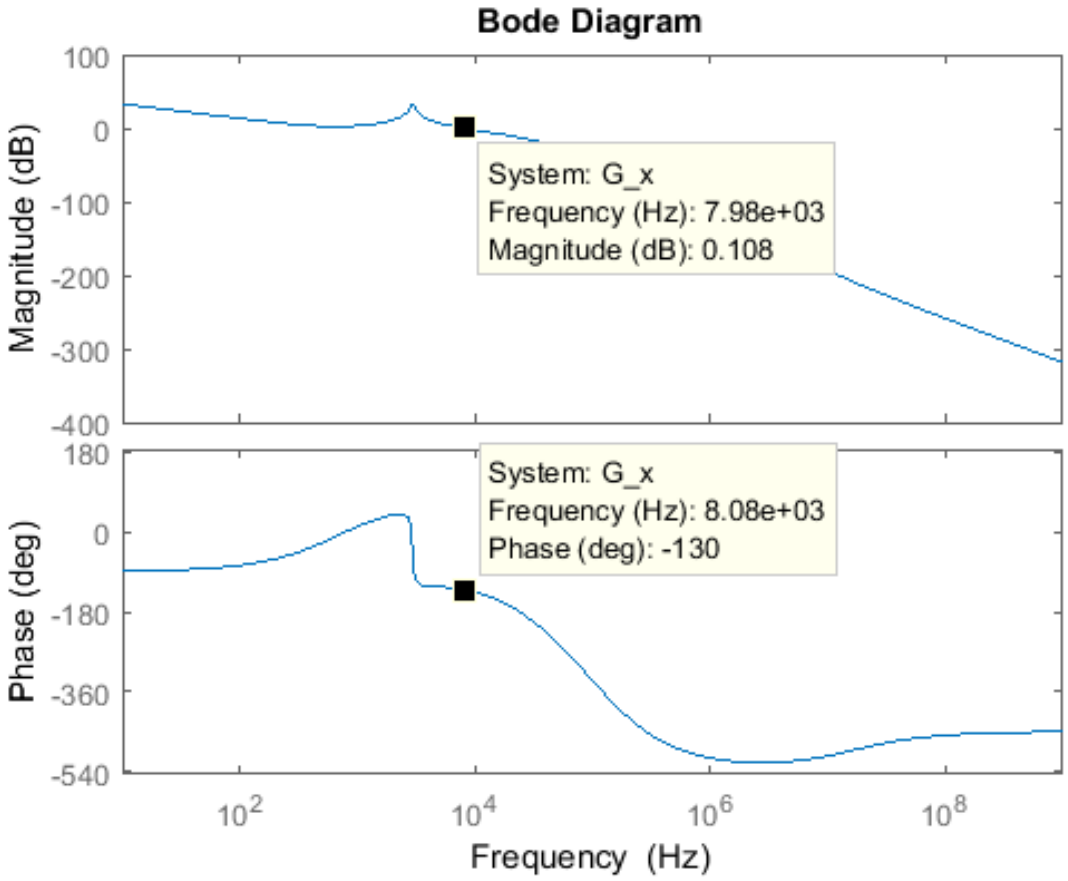

Figure 37 - Complete Open-Loop Bode Plot after Compensation

4.4 Closed-Loop Simulation

In order to test the designed compensator, MATLAB's Simulink was used to model the complete closed-loop system as seen in Figure 38. A Z-transform block with the coefficients listed in Equation (17) was used to model the custom-designed discrete-time compensator in this simulation.

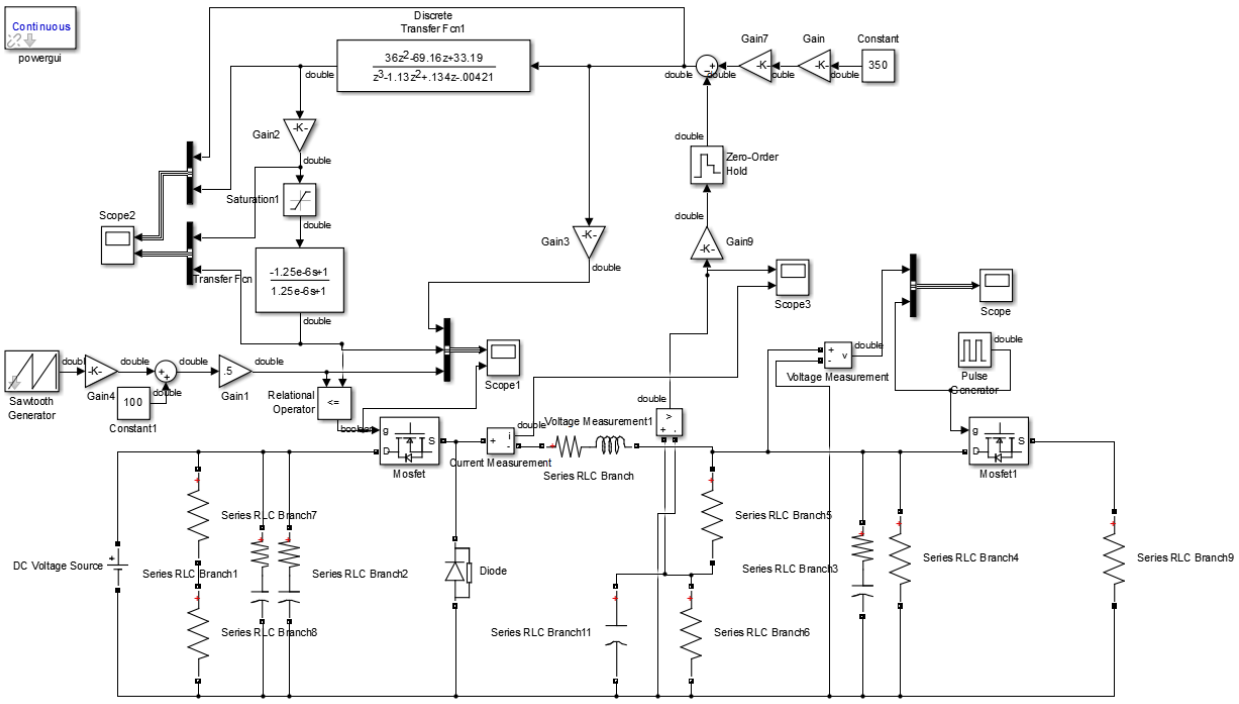

Figure 38 - Simulink Closed-Loop Simulation

This system was supplied with a 675V DC input and a voltage reference of 350V was established, as described previously in this chapter. At a certain point, the system was subject to a load step change, which caused the load current to change from its minimum value to its maximum value, and then back to its minimum value. This was done in order to observe the system's response to a dynamic load change. The results of this simulation are presented in Figure 39 and Figure 40 where the red line represents the output voltage and the blue line represents the dynamic load step trigger. These plots confirm that the system controller provides adequate steady state tracking as well as a sufficient response to a dynamic event.

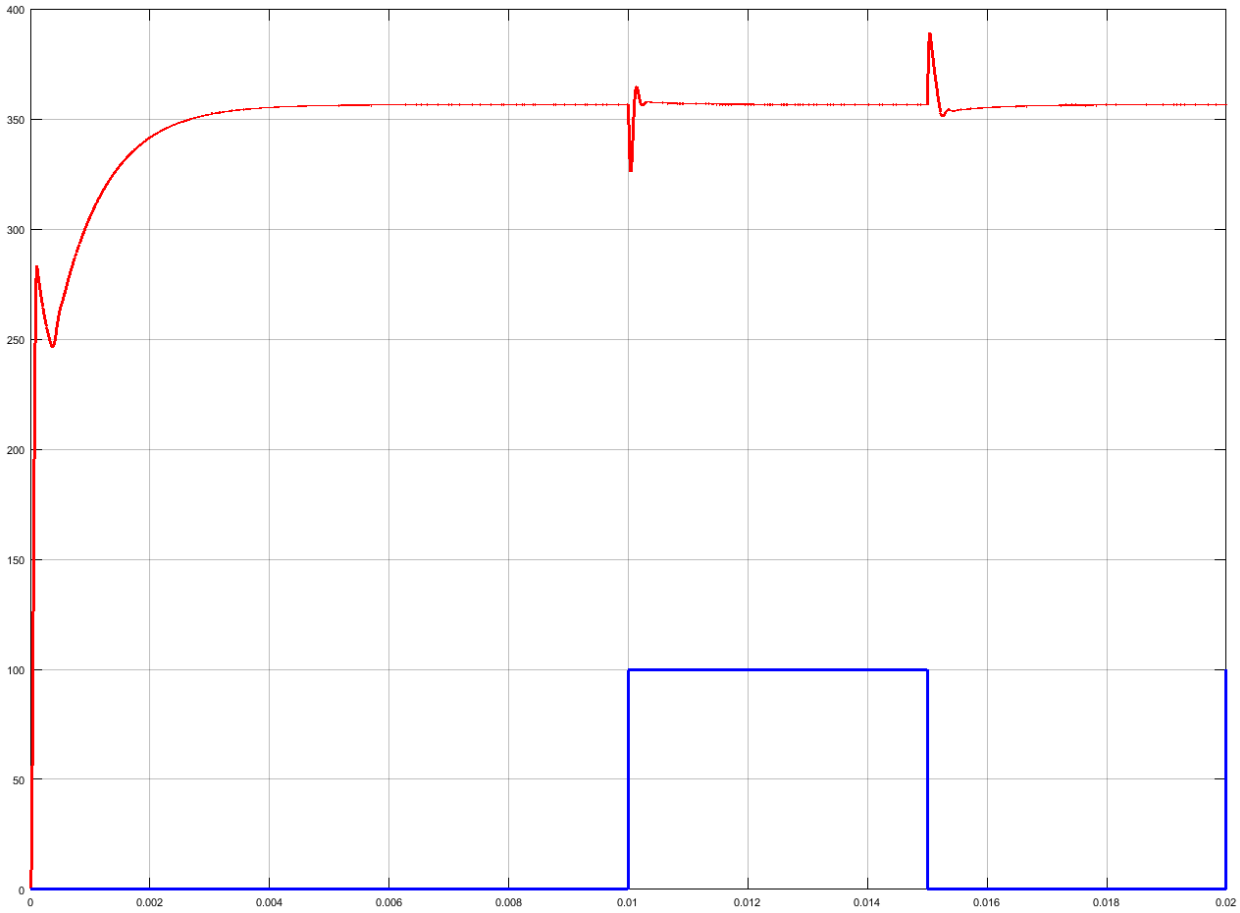

Figure 39 - Simulink Simulation Overview; red waveform is output voltage [50 V/div]; time scale is [2 ms/div].

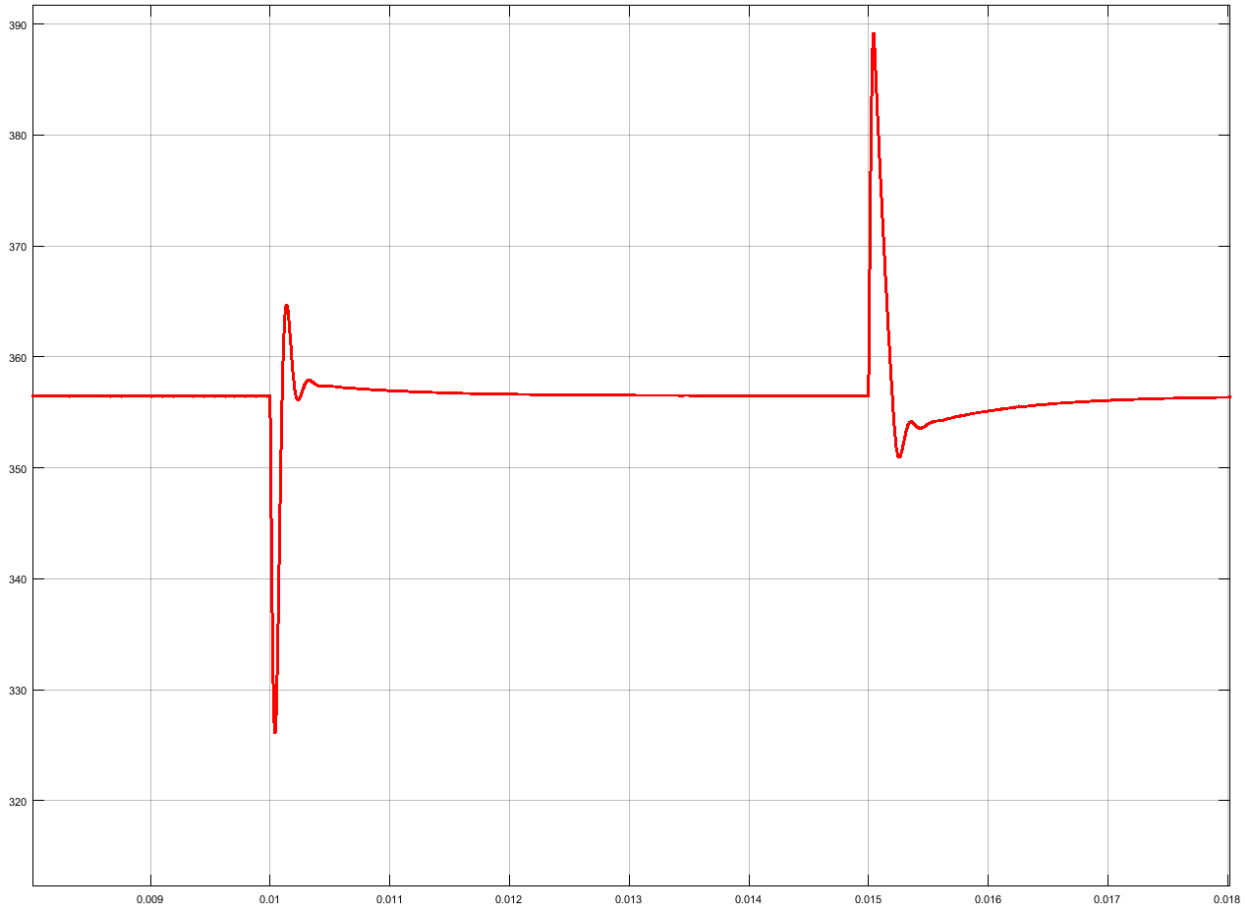

Figure 40 - Zoomed in View of Output Voltage Waveform during Load Step Change; red waveform is output voltage [10 V/div]

4.5 Controller Hardware

To implement the digital controller in this design, a TI TMS320F28027 control card was used. This control card was selected because it was believed to provide adequate sampling rates as well as CPU clock speed among other qualities for performing the necessary calculations for this application. This control card was also packaged as an evaluation kit such that it could be easily interfaced with a PC via a docking station and USB cable. This feature allowed for convenient programming and debugging of the controller during development.

4.5.1 Method for Programming DSP

The primary reason that this controller was selected was its support for MATLAB's Simulink Embedded Coder toolbox to auto-generate source code. This MATLAB toolbox enables the use of the Simulink environment as the system IDE. Thus, by designing a system diagram and configuring a small set of hardware-specific dialog boxes, hours of manual software design can be accomplished in mere minutes. Figure 41 illustrates the implementation of the previously designed type-three compensator in Simulink. From this diagram, Simulink can be used to auto-generate code specifically tailored for the target hardware platform. This code can then be uploaded to the control card using TI's Code Composer Studio software package.

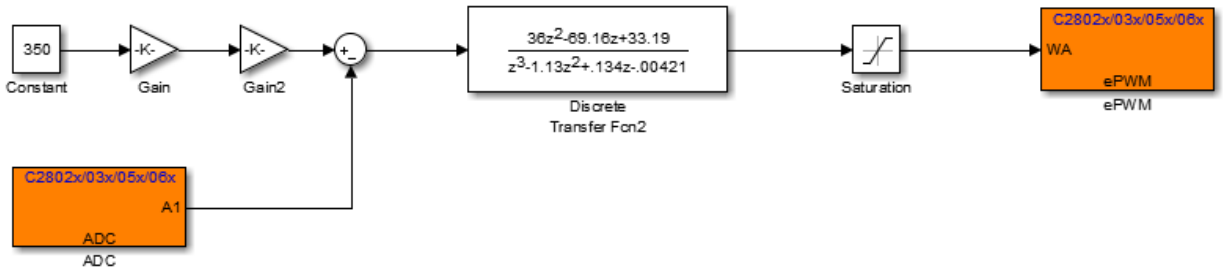

Figure 41 - Simulink Embedded Coder Type-Three Compensator Implementation

4.6 Validation Testing

During the commissioning of the digital controller implementation described in this thesis, several challenges were encountered with the auto-generation of code for the DSP using Simulink. While this feature provides a powerful interface to the DSP hardware, which permits an engineer to design a controller at a high-level of abstraction, some flexibility and determinism is lost in the ability to configure the DSP for high-performance operation. In this case, it was found that the control law implemented via the diagram shown in Figure 41 was not able to

execute properly in real-time on the control card used for the implementation. It is believed that this limitation is due to the floating-point math used to implement the Z-transform block in this diagram when Simulink converts this control algorithm to DSP-specific code. Further work is ongoing to further isolate this problem and implement a work-around, as will be discussed in the future work section of this thesis.

CHAPTER 5

CONVERTER PERFORMANCE WHEN CONSIDERING SIC VS. SI DEVICES

5.1 Testing Environment

This thesis has discussed the performance advantages of SiC MOSFET devices when compared to "legacy" devices such as the Silicon IGBT. Methods for confirming the claims made about the single cycle characteristics of SiC MOSFET devices have been previously presented in terms of static characteristics and CIL test results. A practical design application for these devices has also been presented in the form of a DC-to-DC buck converter. This chapter will detail the results of operating these high-performance SiC MOSFET devices within the custom-designed converter described previously.

5.1.1 Enclosure

In order to ensure safe operation of the high-voltage converter under consideration, a safety enclosure was constructed. This enclosure, seen in Figure 42, was fabricated using 1” aluminum extrusions and ¼” thick clear polycarbonate panels. This enclosure served many purposes that included acting as a blast shield in the event of DUT failure, and an added buffer of insulation between the test engineer and high voltage electrical connections present in this system. The enclosure also provided a sturdy mechanical platform on which the converter could be elevated in order to optimize air-flow and cooling.

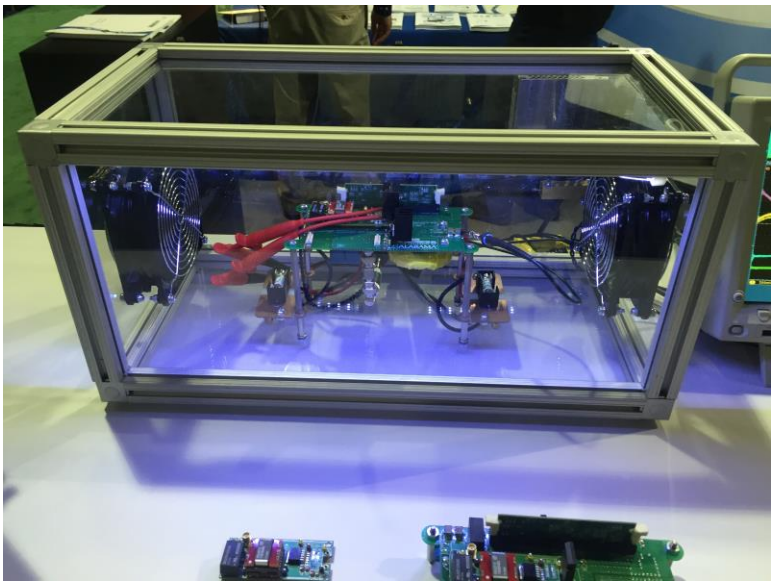

Figure 42 - Converter Enclosure on Display at the 2016 Applied Power Electronics Conference (APEC) in Los Angeles, California

5.1.2 Cooling

The DUTs and all other components prone to elevated heat dissipation were cooled utilizing heat sinks and forced air cooling. Figure 43 gives an example of how the heat sinks were mounted to the DUT and diode in the buck converter. These heat sinks were mounted with an insulated sil-pad gasket and tightened to 0.6779 Nm with a high quality micro-torque wrench. Using a specific torque value for the heat-sink mounting helped to ensure that the following device-to-device comparisons were made on equal terms, since small variations in thermal resistance can considerably affect the performance of switching devices when operating at high temperatures and high frequencies.

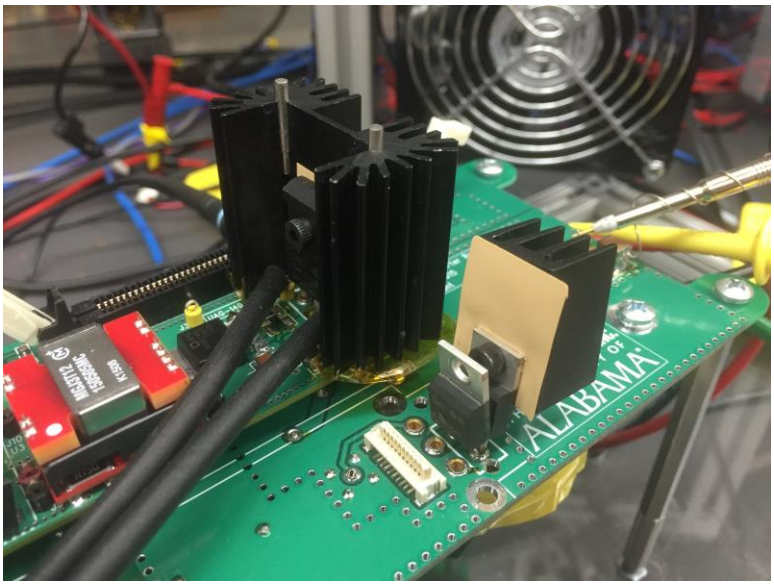

Figure 43 - Heat Sinks Mounted on DUT and Diode

5.1.3 Power Supply & Load

During testing, this converter was supplied power via 10 kW DC supply and was loaded by a reconfigurable resistive load bank. This supply and load allowed for testing across the entire 1 kW to 5 kW load range.

5.2 Instrumentation

In order to monitor the operating characteristics of the converter, several types of instruments were used. A 500 MHz oscilloscope was used to monitor the gate source voltage (V_{GS}) of the DUT, the switch node voltage (V_{SW}), and the inductor current (I_L). A power quality analyzer was also used to monitor the converter efficiency in real-time, and a thermal camera was used to monitor the temperature of the DUT. An example oscilloscope screenshot captured during the converter evaluation is presented in Figure 44.

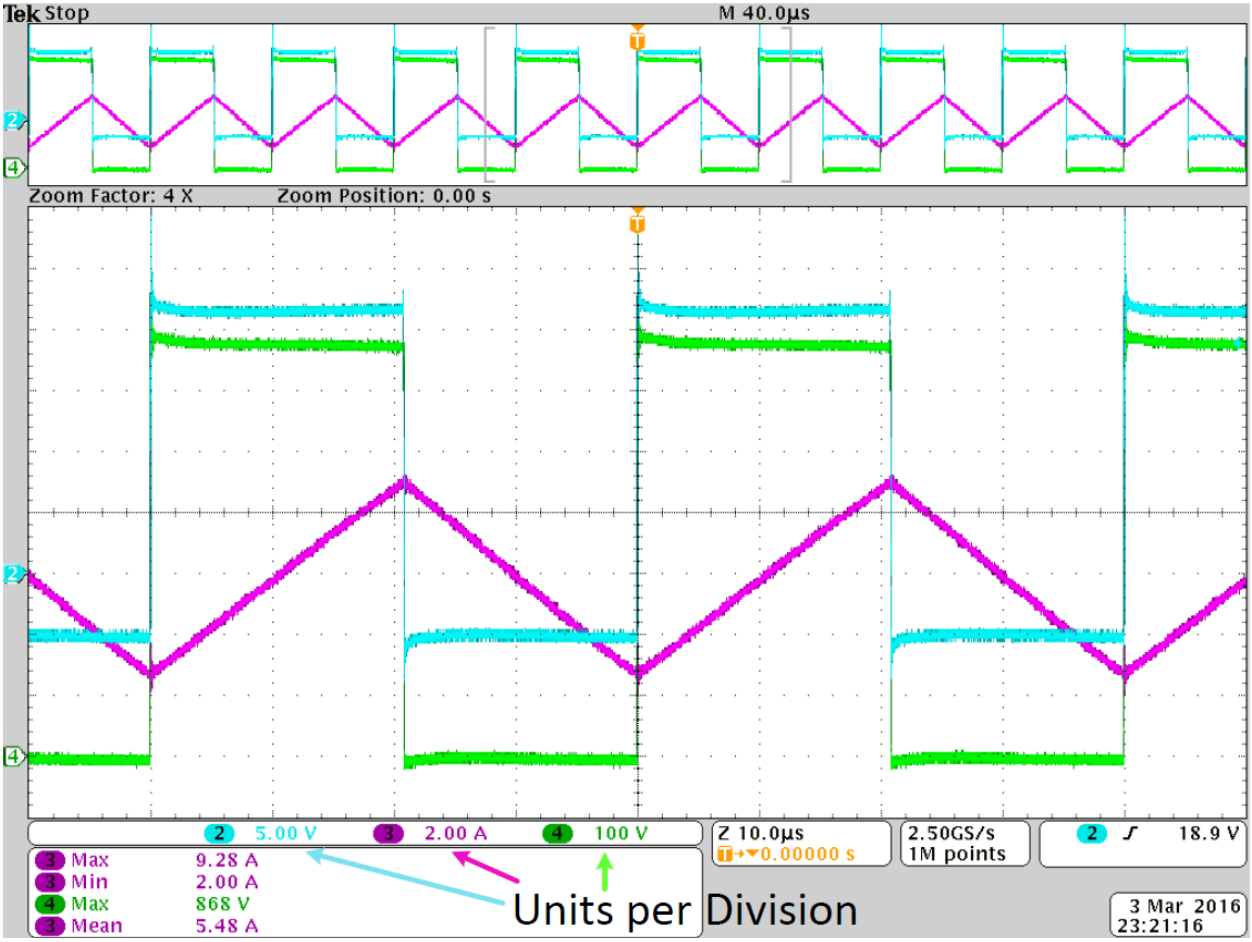

Figure 44 - Converter Waveforms V_{GS} (blue), V_{SW} (green), and I_L (magenta); time scale is [10 us/div]

5.2.1 Device Thermals

The temperature of the part was monitored by a FLIR thermal camera positioned so that it had a clear line of vision to the DUT from the end of the enclosure as shown in Figure 45. This was necessary to ensure that the DUT did not exceed its maximum allowable junction temperature at any point during the testing procedures described here.

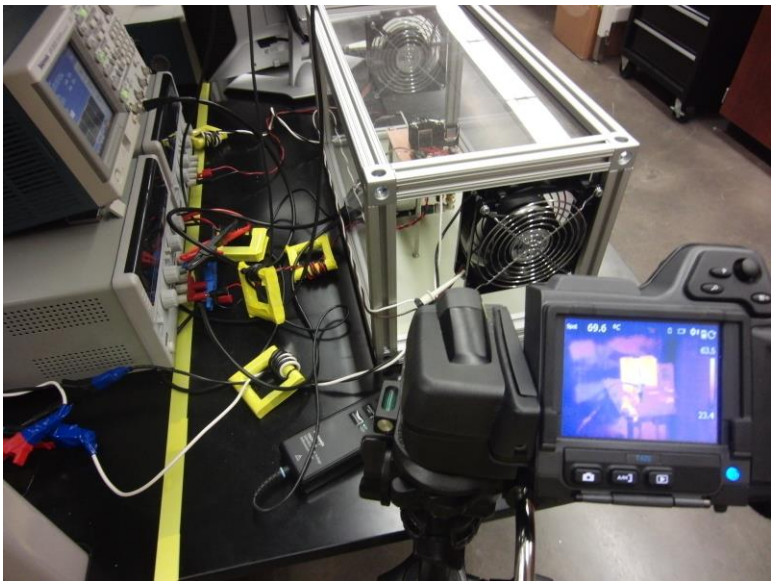

Figure 45 - FLIR Thermal Camera Monitoring DUT Temperature

5.3 Test Outline & Objectives

The following test procedures had two primary objectives. The first objective was to compare the SiC MOSFET to the Si IGBT in terms of how the device selection affected the overall performance of the converter under identical operating conditions. The second objective was to make a direct performance comparison across several different models of SiC MOSFET's. The metric used to make these comparisons was overall converter efficiency. The converter's efficiency was calculated using a PQA connected to the converter as shown below in Figure 46.

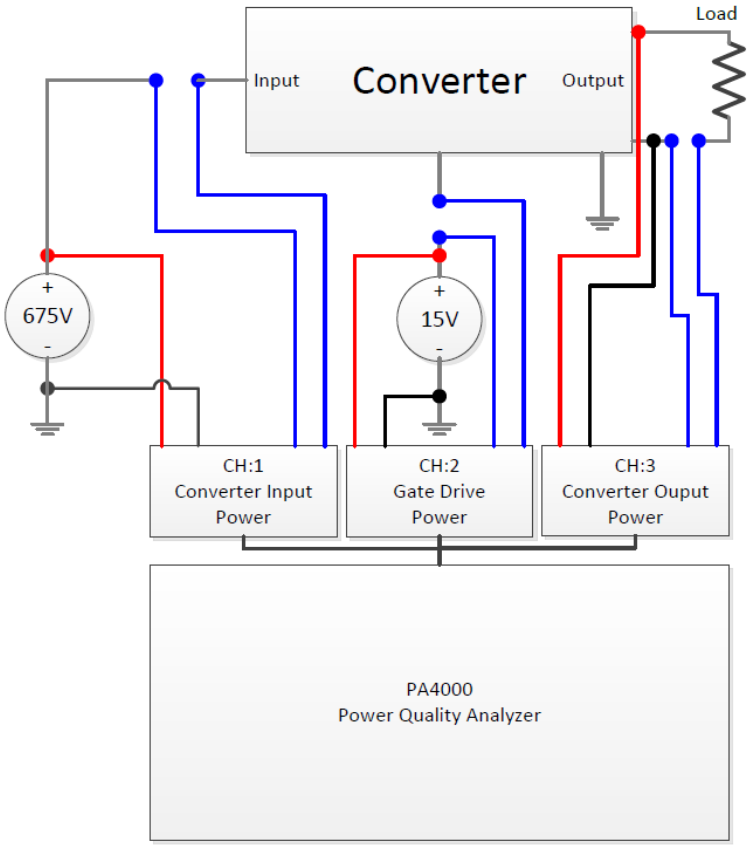

Figure 46 - PQA Configuration

In this configuration, the overall converter efficiency is described by Equation (18).

$$\eta = \frac{CH{:}\,3(Watts)}{CH{:}\,1(Watts) + CH2{:}\,(Watts)} \times 100 \qquad (18)$$

Where:

η: efficiency

CH:1: converter input power

CH:2: gate Drive Power

CH3: converter output power

It should also be noted that testing was terminated immediately due to the risk of part failure during any test run if the DUT temperature exceeded 150° C.

5.4 Test Outline & Results

As mentioned previously, the converter testing described in this chapter had two underlying purposes:

1) Illustrate the operating characteristics (efficiency and thermal management) of SiC MOSFETs compared to Si IGBTs across a 1 kW to 5 kW load range at low operating frequencies (25 kHz, 35 kHz, and 50 kHz).
2) Illustrate a head-to-head comparison of an array of SiC MOSFETs from different manufacturers across a 1 kW to 5 kW load range operating at 200 kHz.

For these tests, a manual switched resistive load bank was used to subject the converter to each of the desired load steps.

5.4.1 SiC MOSFET vs. Si IGBT

For this test, two Si IGBTs and on SiC MOSFET were subjected to identical operating conditions within the converter testing environment. The converter load was swept across a range from 1 kW to 5 kW in 1 kW load steps. This test was repeated for a 25 kHz, 35 kHz, and 50 kHz switching frequency.

Figure 47, Figure 48, and Figure 49 give a clear indication that the SiC MOSFET outperformed the Si IGBT across the entire load range at the 25 kHz, 35 kHz, and 50 kHz operating

frequencies. Testing for the IGBT was terminated in some cases due to thermal runaway as shown in Figure 50, Figure 51, and Figure 52. This same test was not possible at any switching frequencies greater that 50 kHz due to the thermal limitations of the Si IGBT.

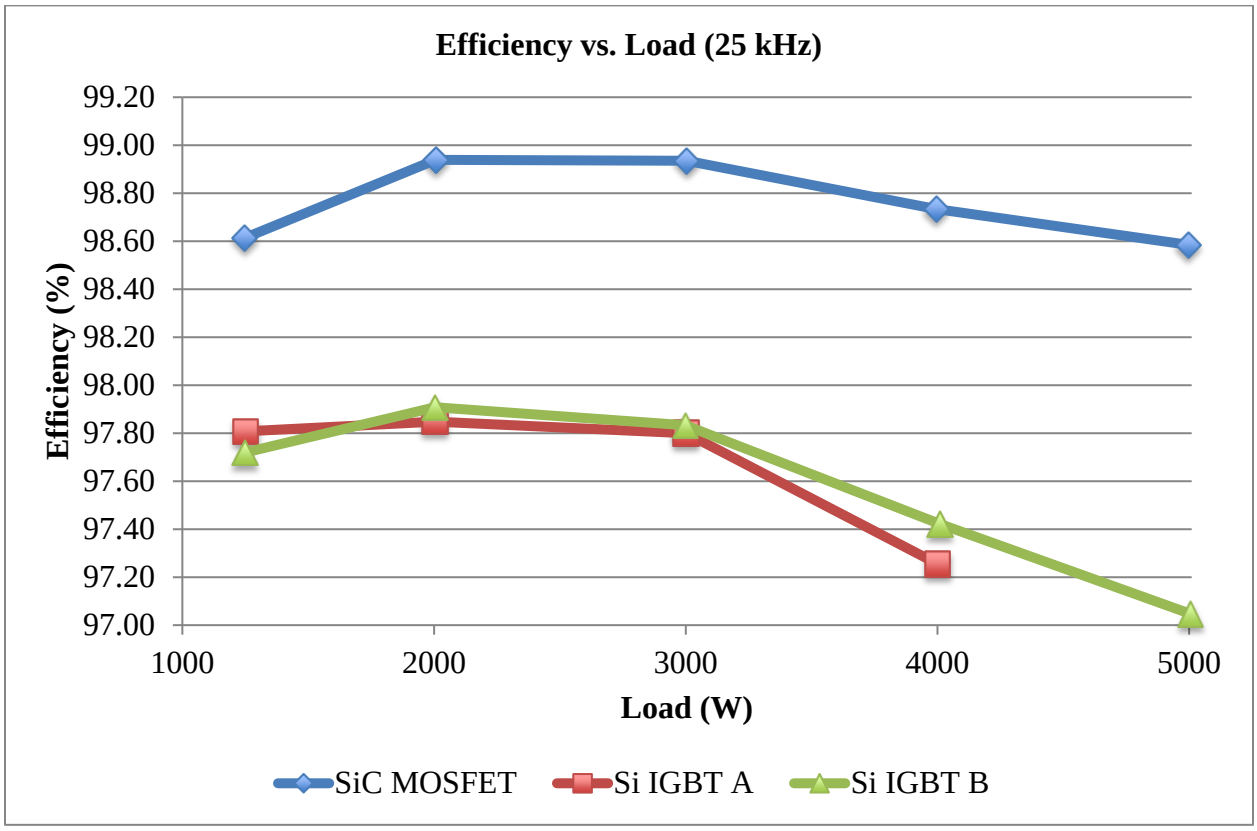

Figure 47 - SiC MOSFET vs. Si IGBT Efficiency Comparison (25 kHz)

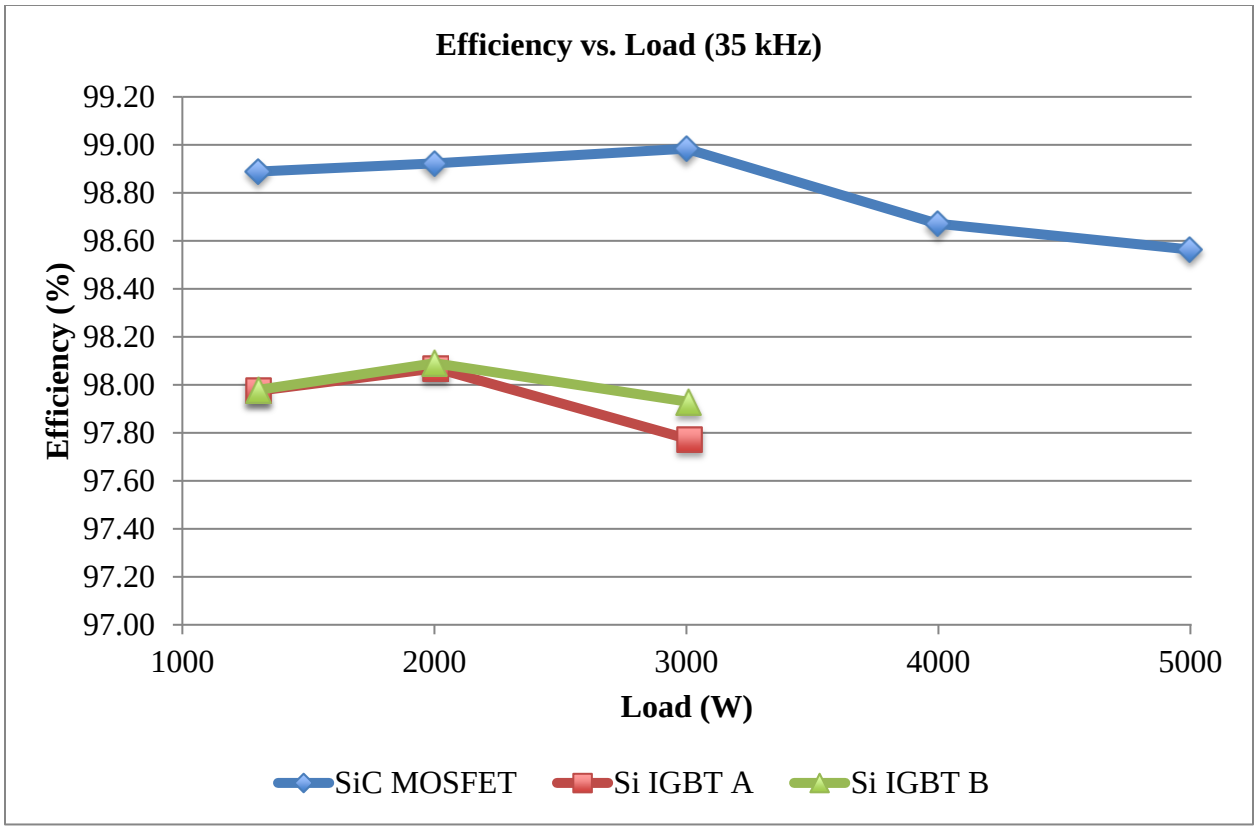

Figure 48 - SiC MOSFET vs. Si IGBT Efficiency Comparison (35 kHz)

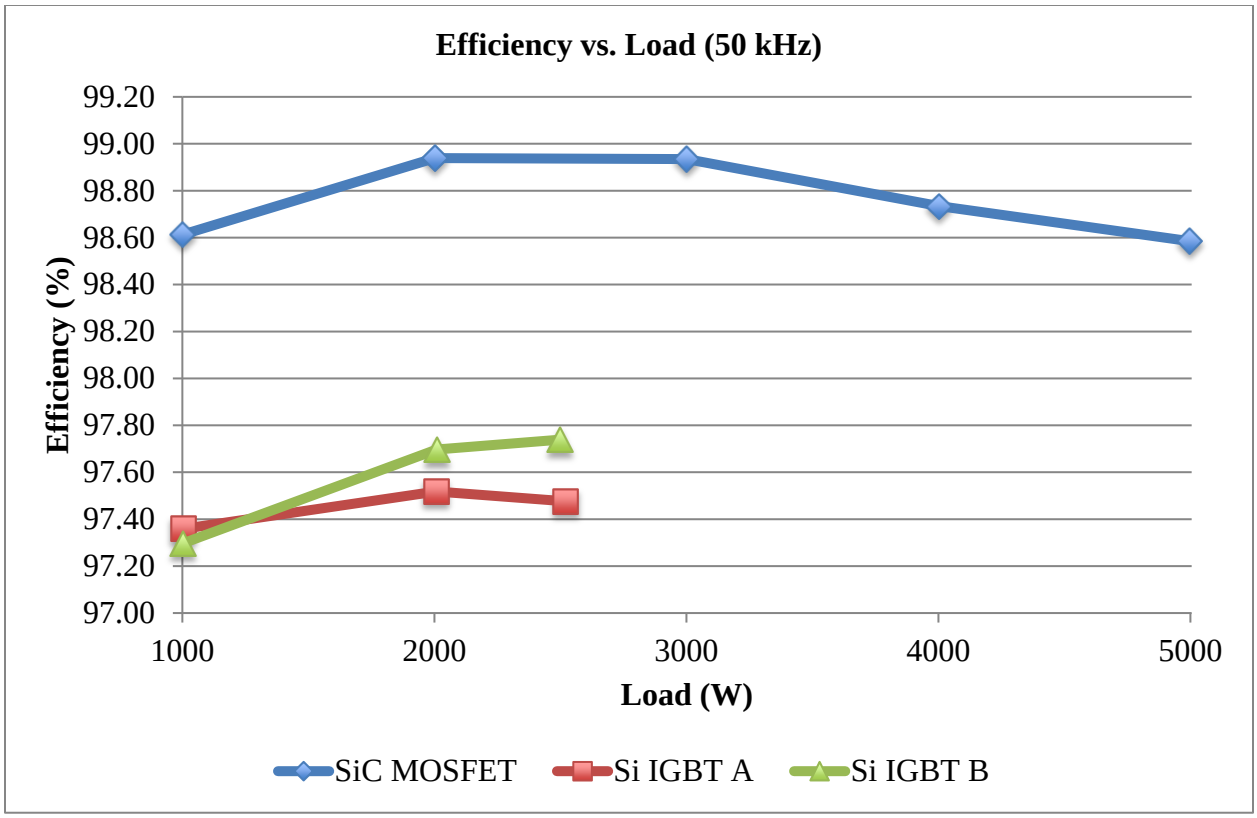

Figure 49 - SiC MOSFET vs. Si IGBT Efficiency Comparison (50 kHz)

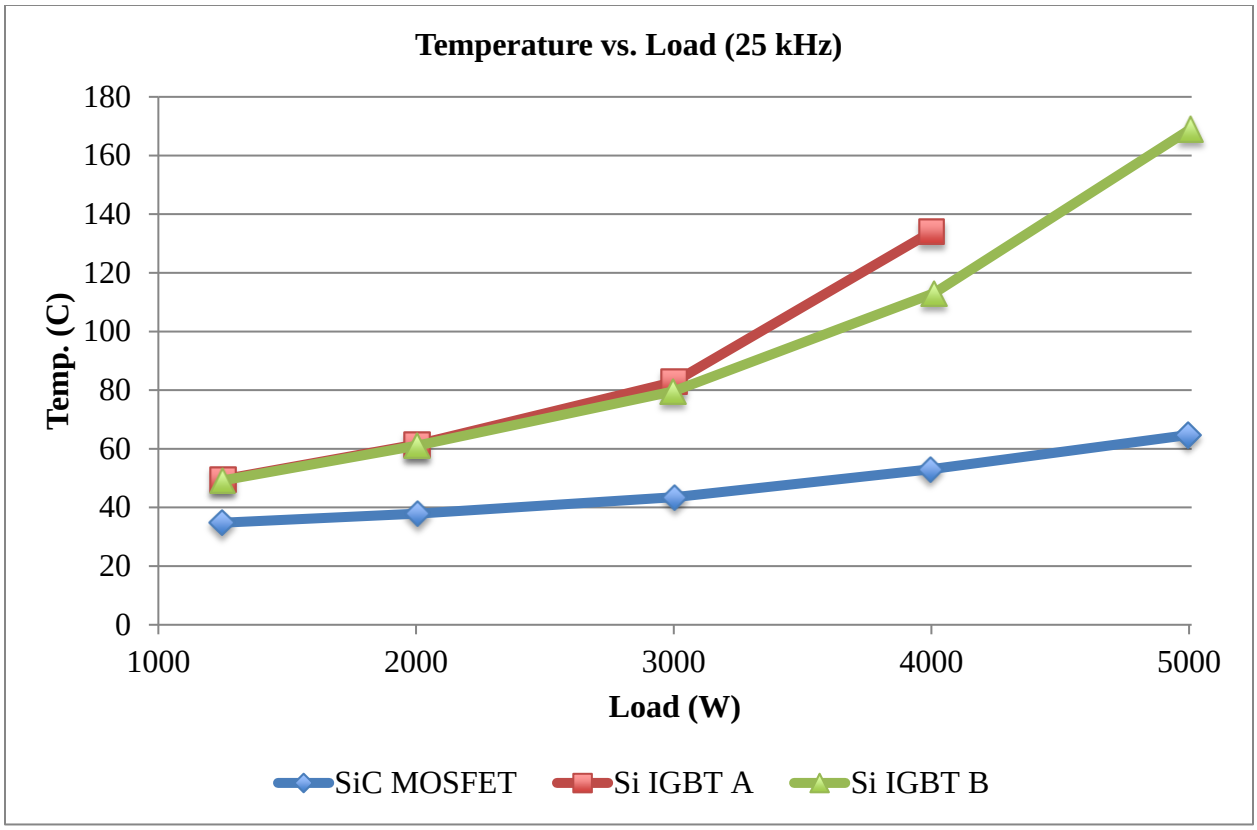

Figure 50 - SiC MOSFET vs. Si IGBT Temperature Comparison (25 kHz)

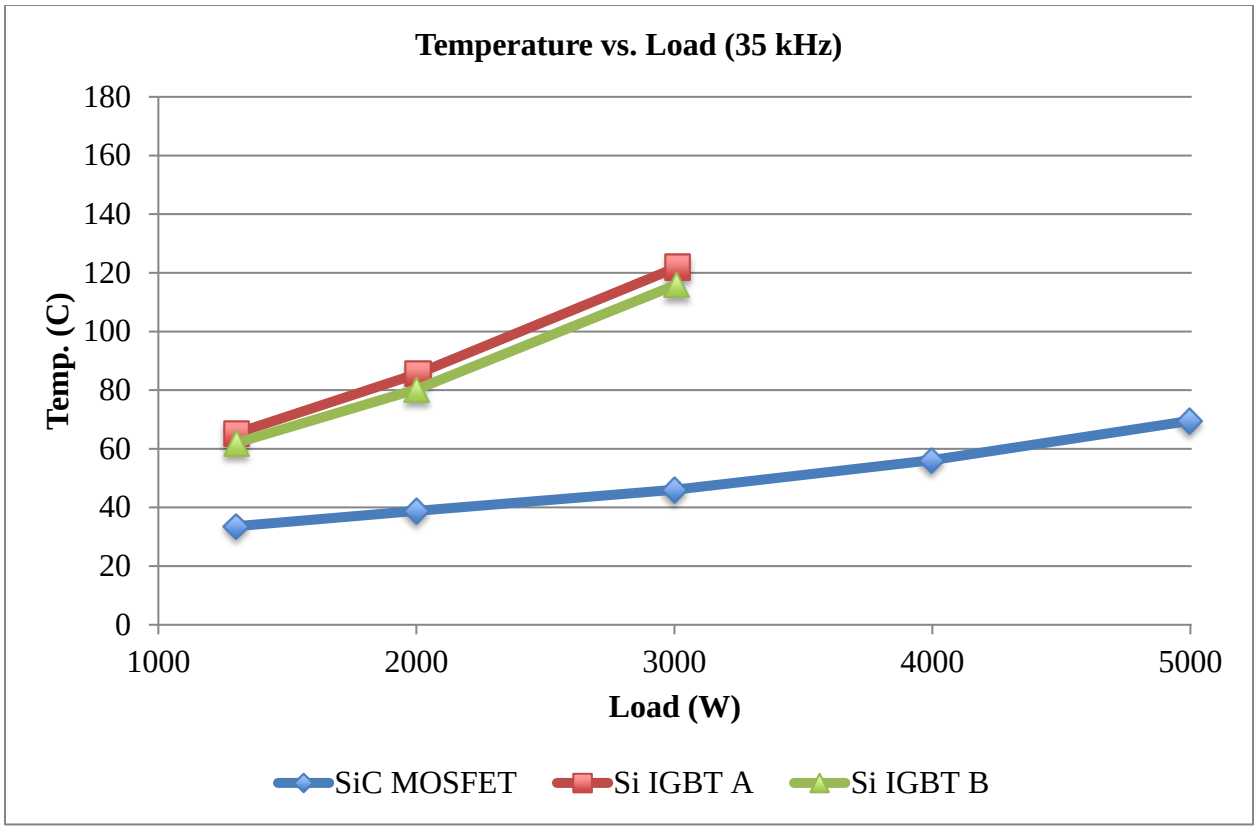

Figure 51 - SiC MOSFET vs. Si IGBT Temperature Comparison (35 kHz)

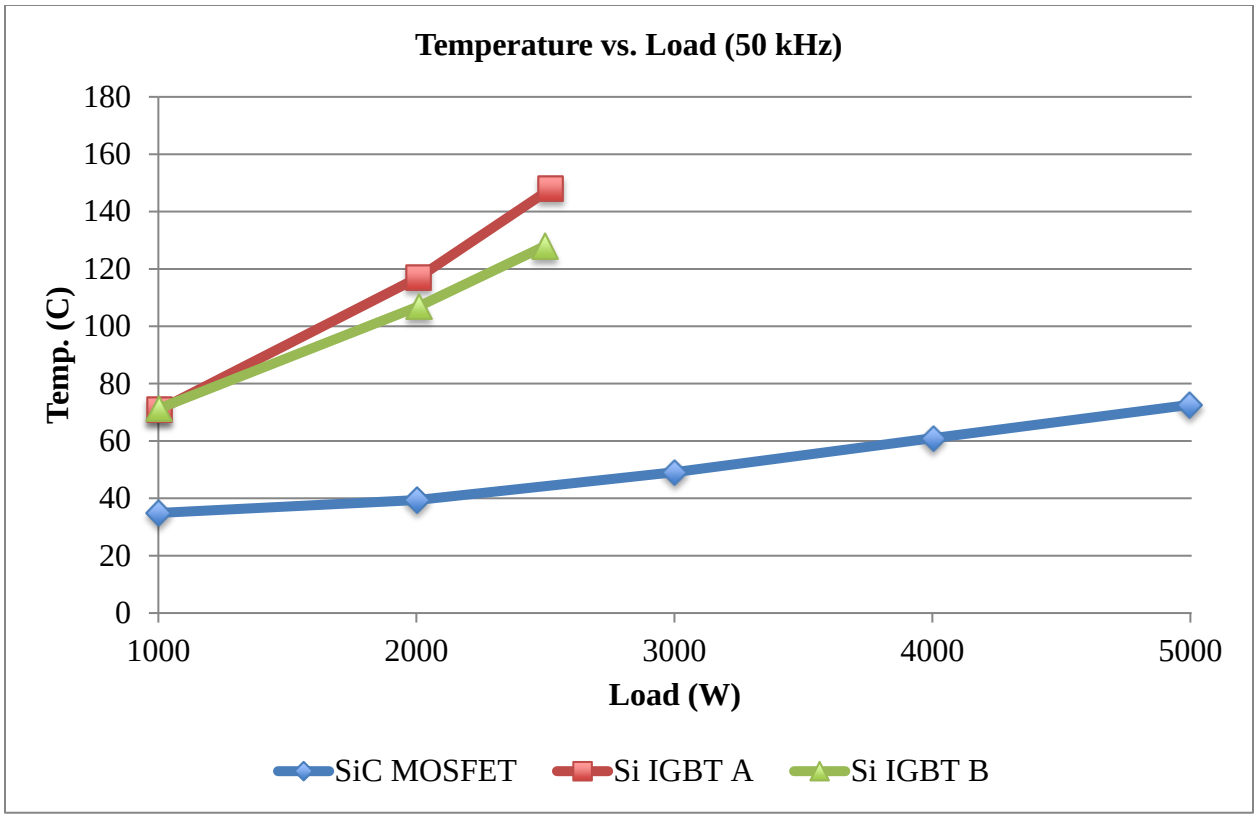

Figure 52 - SiC MOSFET vs. Si IGBT Temperature Comparison (50 kHz)

5.4.2 SiC MOSFET Head-to-Head Comparison

The second set of tests involved evaluating an array of SiC MOSFETs from a number of different manufacturers. This test served the two purposes:

1) Illustrating the operating characteristics and relative performance of SiC MOSFETs from different device manufacturers.
2) Illustrating the power density benefit of operating a converter at a much higher switching frequency than is possible with a Si IGBT.

Similarly to the previous tests, each of the SiC MOSFETs was subjected to identical converter operating conditions which included a 1 kW to 5 kW load sweep at an operating frequency of

200 kHz. Each of the device's thermal properties and its effect on the converter's efficiency were subsequently observed and are shown in Figure 53 and Figure 54.

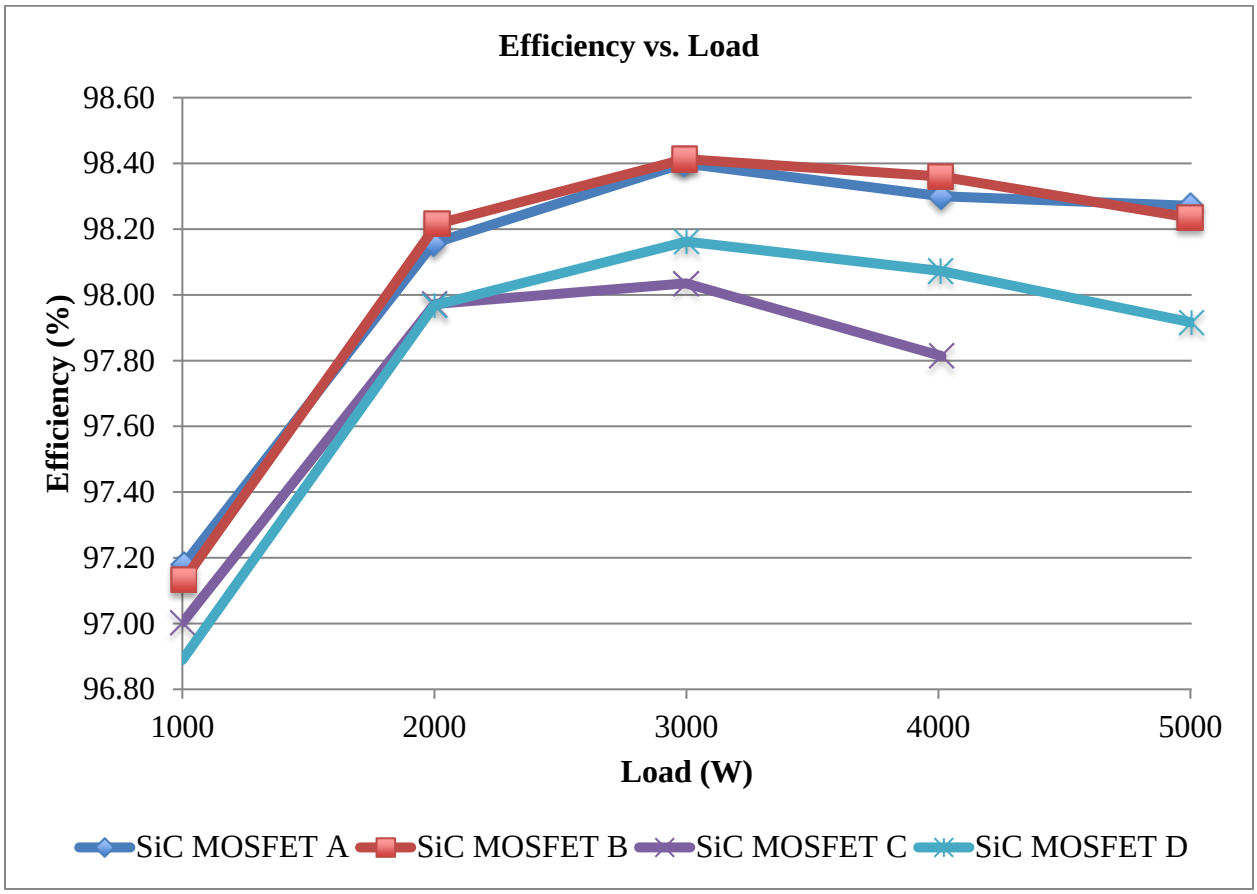

Figure 53 - SiC Head-to-Head Efficiency Comparison (200 kHz)

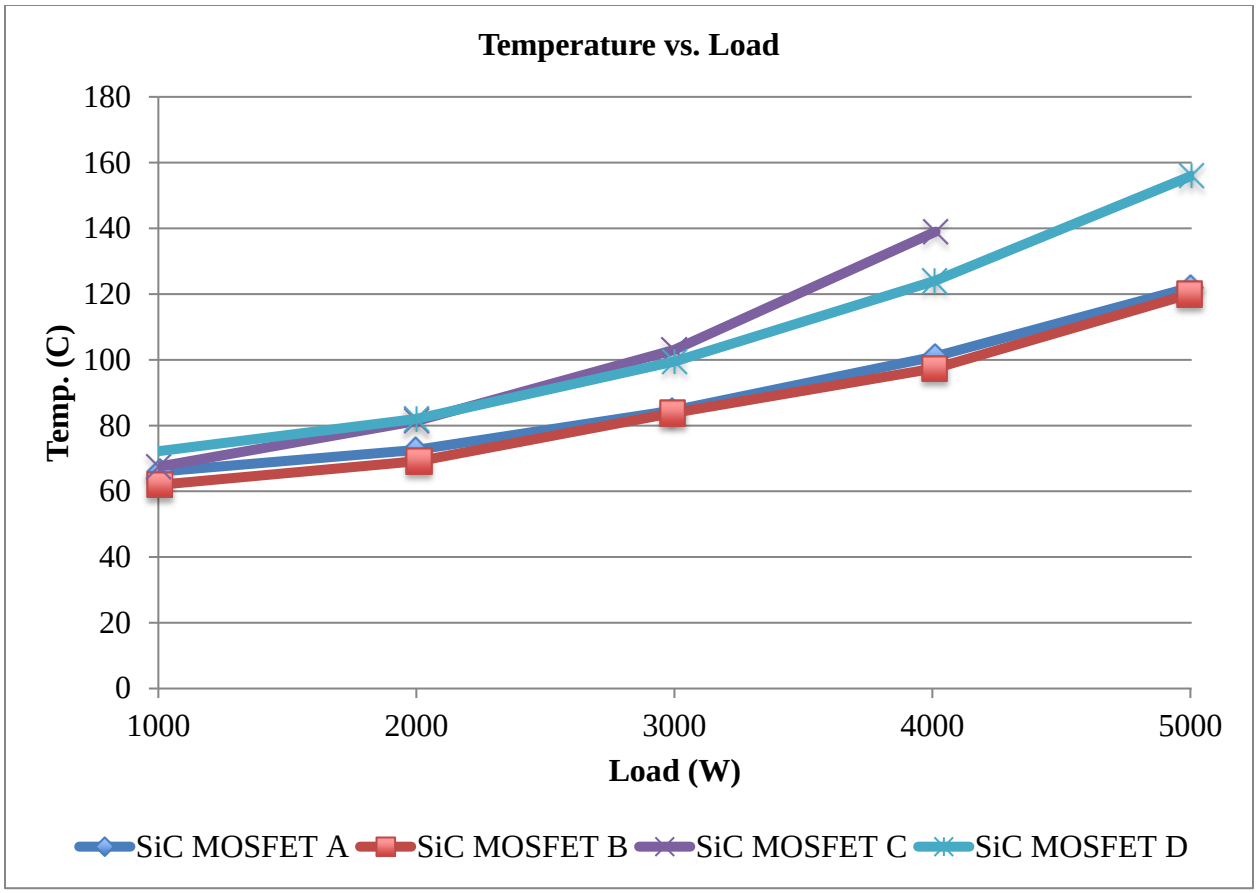

Figure 54 - SiC Head-to-Head Temperature Comparison (200 kHz)

As Figure 53 and Figure 54 indicate, each of the SiC MOSFETs tested performed with similar efficiency metrics and only one device's testing had to be terminated prematurely due to thermal run away.

This section mentioned previously that the power density of the converter was improved drastically by implementing a 200 kHz operating frequency as opposed to a 25 kHz operating frequency. Chapter 3 detailed the selection of a filter inductor for the same converter tested in this chapter operating at a minimum switching frequency 100 kHz. That inductor had a volume approximately equal to 4.4 in^3. In order to operate the converter at 25 kHz and perform the tests

discussed in Section 5.4.1, an inductor network, shown in Figure 55, was implemented in order for the converter to operate in continuous conduction mode (CCM). This inductor network is has a volume of approximately 133 in^3, roughly thirty times larger than the inductor needed to operate at 100 kHz.

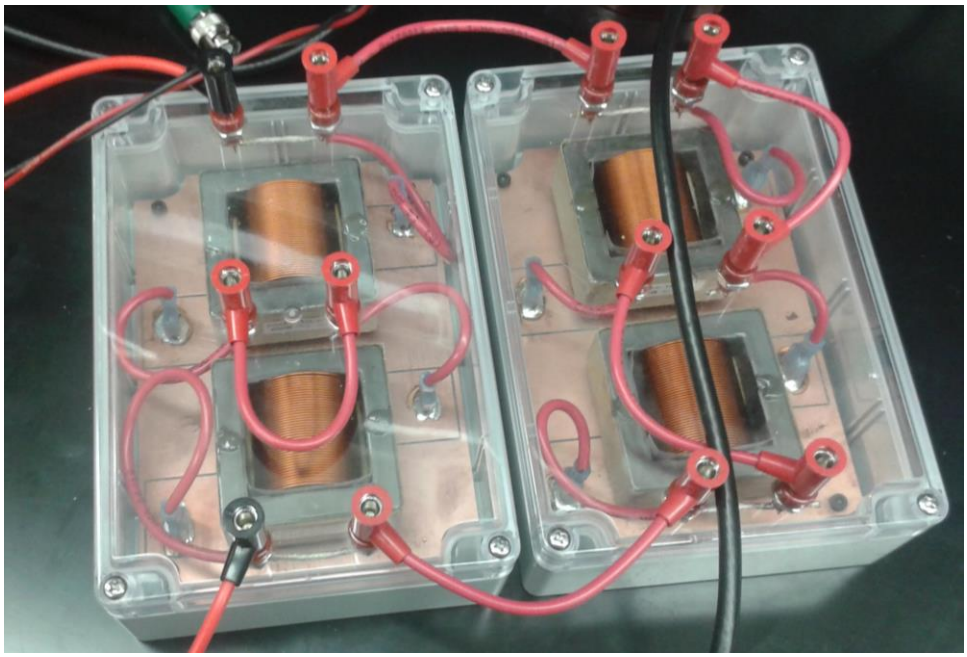

Figure 55 - Filter Inductor Network Necessary for Converter Operation at 25 kHz

CHAPTER 6

CONCLUSION & FUTURE WORK

6.1 Summary of Data Presented and Future Work

This thesis has discussed the performance capabilities of recently commercialized SiC MOSFETs. Methods for confirming the claims made about the single cycle characteristics of these devices have been presented in terms of static characterization and CIL test results. In addition, a practical application example for these devices has been presented in the form of a hard switched DC-to-DC buck converter that was able to achieve a system level efficiency of 99%. Results from testing this converter were presented in the form of converter efficiency and DUT temperature plots. These results confirmed that SiC MOSFETs offers significantly improved performance compared to traditional devices such as the Si IGBT.

Future work envisioned for this project includes more elaborate control techniques that will allow for further optimization of the converter design presented in Chapter 3 and Chapter 4. Some examples of these of these optimization opportunities include: improved dynamic response, synchronous rectification, load-based switching frequency optimization, and user interface capabilities.

The primary contribution of this thesis is a set of practical examples demonstrating the system-level performance benefit available to applications when adopting SiC MOSFETs instead of traditional devices like Si IGBTs and Si MOSFETs. The results presented here demonstrate that

a SiC-based hard-switched converter is substantially more efficient than a design based on Si IGBTs at low switching frequencies. In addition, the SiC-based converter design allowed for higher operating frequencies than the Si IGBTs were capable of accommodating, which was shown to produce a substantial system-level benefit in terms of power density.

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