AUTOMATIC TEST PROGRAM GENERATION AND NOVEL TEST TECHNIQUES FOR TESTING RADIO FREQUENCY AND HIGH-VOLTAGE DEVICE INTERFACE BOARDS

by

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ABSTRACT

This dissertation describes the development and application of two software tools: RF Analyzer and Diagnostic Program Generation (RADPro), and High-Voltage Program Generation (HVPro). We developed these tools to automate the process of testing device interface boards for production testing of IC chips. Testing device interface board is an essential part of a production testing to ensure all components on the board are assembled properly and operational before the actual IC chips can be tested. Our software tools utilize the netlist, bill of materials and component model library. Automatic test program generation by RADPro and HVPro reduces design expense and time to market a new IC product significantly by reducing manual hand-coding work. We have validated some of our pseudocode with the existing automatic test equipment at Texas Instruments, Inc.

DEDICATION

This dissertation is dedicated to my grandparents, the late Srivilliputhur Narayanan Srinivasan and Ramakrishnan Muthuraman, Kamala Srinivasan and Rukmini Muthuraman. I also dedicate it to my parents Kannan Srinivasan and Girija Kannan, for their guidance, support and confidence in me.

LIST OF ABBREVIATIONS AND SYMBOLS

ADS	Advanced Design System
ATE	Automatic Test Equipment
BJT	Bipolar Junction Transistor
BOM	Bill of Materials
CUT	Circuit under Test
CDM	Charged Device Model
DIB	Device Interface Board
DUT	Device under Test
ESD	Electrostatic Discharge
ETS	Eagle Test System
FCMV	Force Current Measure Voltage
FCMVDT	Force Current Measure Voltage with Delay Time
FOX	Field Oxide
FVMC	Force Voltage Measure Current
HBM	Human Body Model
HV	High-Voltage
HV-LDMOS	High-Voltage Laterally Diffused Metal Oxide Semiconductor

HVPro	High-Voltage Program Generation Tool
IC	Integrated Circuit
ICT	In-Circuit Test
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MM	Machine Model
MOS	Metal Oxide Semiconductor
MTDT	Multi-Tone Dither Test
PCB	Printed Circuit Board
RADPro	RF Analyzer and Diagnostic Program Generation Tool
RESURF	Reduced Surface Electric Field
RF	Radio Frequency
SCR	Silicon Controlled Rectifier
TLP	Transmission Line Pulse
TVS	Transient Voltage Suppressor
VLCT	Very Low Cost Test System

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To the casual observer, a doctoral dissertation may appear to be a solitary work. However, to complete a project of this magnitude requires a network of support, and I am indebted to many people.

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CHAPTER 1

INTRODUCTION

Conventional wisdom on integrated circuit (IC) chips constitutes an area of nanoelectronics to produce small and low-cost electronic systems for military and commercial applications. Analog, mixed-signal and RF integrated circuit chips are composed of highly integrated transistors, capacitors, resistors and inductors. Due to their extremely small footprint, the utilization of IC chips has been proliferating in modern electronics such as smart phones and cameras. The significant advances in nanoelectronics have made most of the hand-held electronic products smaller and cheaper; however, developing low-cost test technology for IC chips has been extremely difficult to keep up with the industry demands.

A typical IC production cycle starts from identifying the specifications for a particular application, followed by design and layout, where a design engineer would validate the design in a software environment. The designs are then sent to the fabrication facility, where the chip is fabricated. These chips are then packaged to be used as an end product [1]. Electronic packages provide a means for interconnecting, powering, cooling and protecting IC chips. Since semiconductor chips are expensive, a testing scheme is necessary to ensure the integrity and performance of the entire package interconnect paths. Finally, the finished product is ready to be tested and shipped to the customers.

Testing involves verification of functional requirements of the IC and elimination of bad products at the early stage of production, thus saving on cost and time. This involves verification during the design and layout cycle and also post-silicon validation.

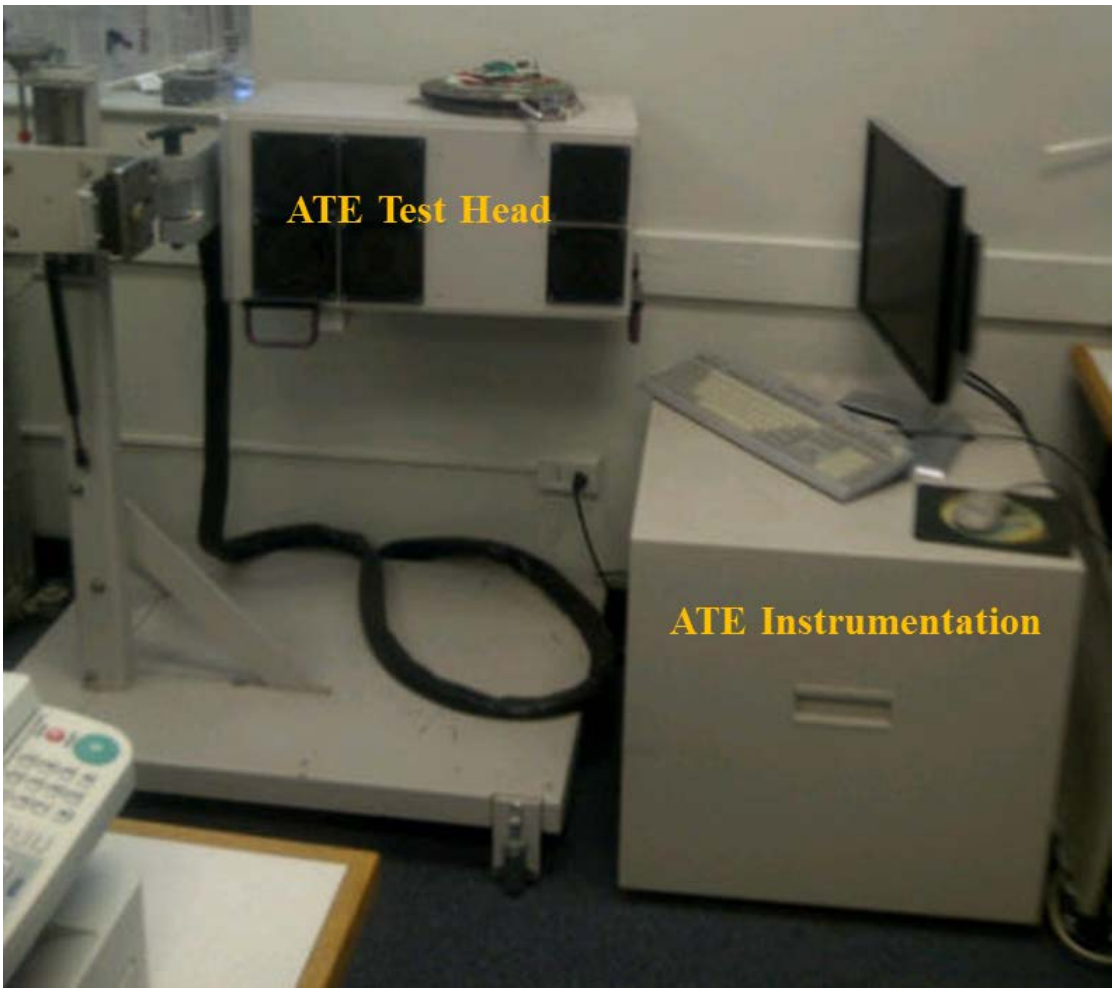
Post-silicon validation includes:

1. Wafer level testing.
2. Bench characterization of ICs.
3. Production floor validation and testing.

Wafer level testing involves testing of unpackaged bare silicon dies. This process eliminates the defective bare dies which involves detection of process related defects. Post silicon bench characterization is the first step of evaluating a packaged IC. The next step is the production floor validation and testing to identify the manufacturing defects. They are tested for different specifications based on their applications.

Production testing is done using an Automatic Test Equipment (ATE) that has inbuilt instrumentation and provides programming capability to test the ICs as shown in Figure 1 [2].

Figure 1. Automatic Test Equipment used to Test ICs



With the decrease in footprint of the ICs, there is a constant increase in the complexity of testing procedures. The complexity of the Device Interface Boards (DIBs) used to test ICs also increase with the Device under Test (DUT) complexity. Some of the challenges include development of test techniques, reduction of test time and cost, and increasing the accessibility and controllability for testing the IC. Since the test time and cost of testing have a direct impact on the time it takes to get the IC on the market, it has become necessary to offer solutions to provide fast, reliable and cost effective methods to test the ICs.

The testing infrastructure plays a vital role in the measurements to be verified, time and cost of testing. The testing infrastructure primarily includes,

1. Hardware platform and instruments to provide input stimulus and measure the output response.
2. Software tools for programming the instruments to automate the test procedure.
3. DIB to provide interface between the tester instrument and the ICs to be tested.

These instruments must be reliable and calibrated to perform measurements. They should also meet the challenges for making measurements for all the specifications of the ICs.

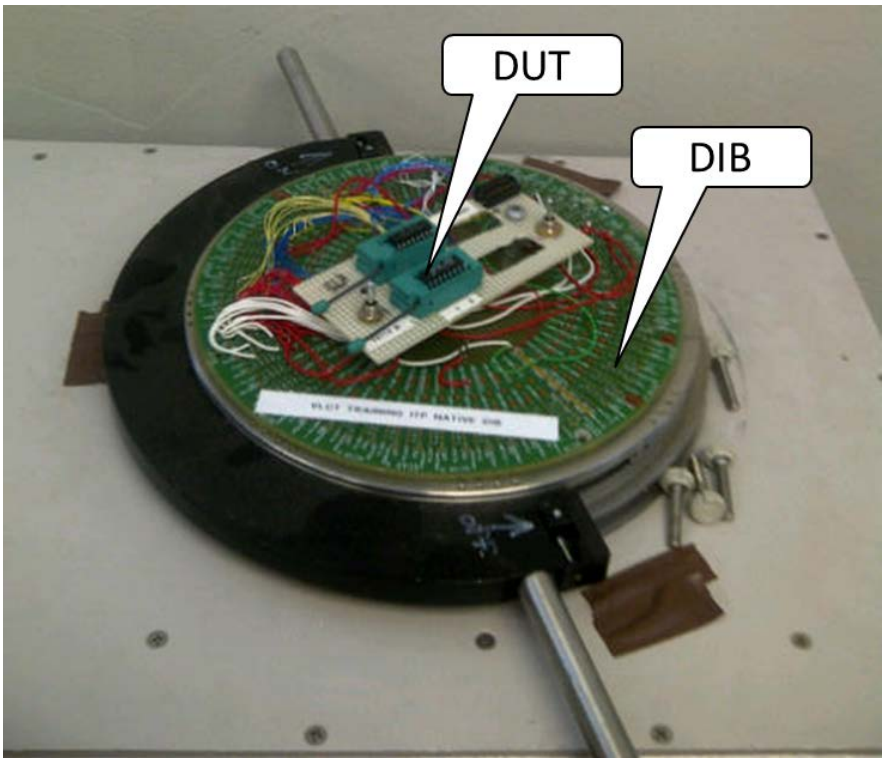
The most essential part of the testing procedure is the DIBs. They contain circuits to facilitate the user to make measurements for different specifications, which vary with each IC. Their complexity increases with that of the DUT. New software tools have been developed to perform tests to verify the DIBs. This dissertation discusses in detail the different algorithms and testing procedures used to automatically generate diagnostic test instructions for the RF and high-voltage DIBs with the added capability of testing high voltage devices.

1.1. DEVICE INTERFACE BOARD

A DIB, load board, interface board or DUT board is a circuit board designed to serve as an 'interface' between the ATE and the DUT. They are designed to provide test input stimulus to the DUT. A typical DIB for testing Radio Frequency (RF) devices predominantly comprises analog and RF circuits on a printed circuit board with multiple component types (capacitors, resistors, diodes, filters, baluns and ICs). Presently there are several techniques used for testing assembled DIBs, such as in-circuit tests, functional tests and flying probes. Each of these test

methodologies is labor-intensive and expensive for achieving high test coverage. In addition there is a lack of accessibility to test nodes on the board, with small footprint components and connectivity from the DUT socket to the board [2]. Although the importance of testing these DIBs in a timely and accurate manner is well understood, test engineers currently do not have the proper set of tools to achieve the goal of testing the boards in hours rather than days [3]. In the absence of these tools, the engineer inserts new silicon into a new DIB that is not certain to be fault-free. Hence there is an urgent need to expedite automatic hardware diagnostic capabilities to ensure expedite functioning of the test hardware.

Figure 2. Typical RF Device Interface Board



The ICs are tested for their functionality and characterized extensively for their performance under different specifications. The next stage of production testing mainly involves

identifying manufacturing defects in ICs on the production floor [4]. DIBs are designed as a means to provide test signals to the DUT. They also provide the means to stimulate the operating conditions for the DUT to evaluate its performance.

A typical DIB, as shown in Figure 2, comprises mixed-signal and RF circuits with several component types, including capacitors, resistors, RF filters, RF traces, ICs and SMA connectors. Apart from these discrete components, they also have sockets that hold the DUT and enable contact between DUT pins and the traces on the DIB. In high-voltage DIBs these components are subjected to extremely high voltages in the order of 300 V to 1000 V. This charge has to be extracted in an efficient manner, such that the devices and other discrete components are protected once the test is completed. The complexity of these boards is also determined by the trace interconnecting these components on board. The overall complexity of the DIB primarily depends on the complexity of the DUT, tester hardware platform and test functions required. A DIB used with an ATE in the IC production environment is comparatively simpler than the DIBs designed for bench characterization of ICs. Furthermore, on the IC production floor, where massive IC testing is carried out on ATEs, DIBs become faulty because of the failure of components on boards in use. This creates a requirement for techniques to test DIBs before they are deployed for IC testing and also at regular intervals on the IC production floor, to ensure that the DIBs remain fault-free. The existing techniques for testing DIBs are very expensive, time-consuming and limited in their capability due to the tester instrumentation. Thus, a novel test generation methodology for testing complicated DIBs in an efficient manner is presented.

1.2. MOTIVATION FOR DEVICE INTERFACE BOARD TESTING

As the first batch of silicon arrives from the fabrication facility, the test engineer is responsible for testing the IC and characterizing data. This task is accomplished by performing testing on the ATE. Once a new IC is made, a DIB is created to specifically test that IC [5]. The test engineer does not have the proper set of tools to verify the DIB with its schematic. In the absence of these tools, the test engineer inserts the silicon into the DUT socket in the DIB. During the testing process any deviation from expected results cannot be attributed to the malfunction of the DUT or the DIB [6]. Also on production floors, DIBs already tested to work efficiently and in use can become faulty as some passive components may fall off or a relay fails to switch. This creates a requirement for the DIBs to be tested before the silicon is inserted and device testing is performed. Some tester platforms use the floating ground concept for differential testing. Hence for testing RF DIBs and also mixed signal DIBs on such tester platforms, a new test methodology was developed, and test generation was automated with RF Analyzer and Diagnostic Program Generation Tool (RADPro). This tool was further developed to incorporate testing high-voltage devices and DIBs, where the charge extraction is a major bottleneck. The Electro-static Discharge (ESD) path of the high-voltage device is identified, and the charge is extracted using ESD protection devices such as Silicon Controlled Rectifiers (SCR) that employ a unique triggering mechanism. The ultimate goal in production testing is to develop a single software tool that can perform production level testing on both the device and board levels over various tester platforms. To realize this goal, we developed a novel test methodology and incorporated it into the software tool for testing high voltage devices. This methodology

performs fault modeling for various process-related defects associated with high-voltage devices, such as gate-oxide shorts, gate stress and drain leakage, due to high voltage and thermal overload respectively. These fault models were then used in device testing to obtain the AC timing specifications.

1.3. CURRENT DEVICE INTERFACE BOARD TESTING TECHNIQUES

There are several test techniques used to test DIBs. The most commonly used are in-circuit testing, functional testing and a flying probe test. An in-circuit test (ICT) is an example of white box testing, where an electrical probe tests a populated DIB, checking for shorts, opens, resistance, capacitance and other basic quantities to determine correct fabrication and assembly. It may be performed with a bed of nails type test fixture and specialized test equipment, or with a fixtureless in-circuit test setup. This technique of testing DIBs is being slowly superseded by boundary scan techniques (silicon test nails), automated optical inspection and built-in self-test, due to shrinking product sizes and lack of space on DIBs for test pads.

In the flying probe tester, the bed of nails is replaced by flying probes, which make a mechanical contact with the DIB. The capabilities of a flying prober should be separated into two categories: electrical test and mechanical interface. First it is necessary to physically make contact with the board, and then to perform a test [7]. Deficiencies in either of these areas will rapidly diminish the effective use of the system. But first and foremost, a flying prober is still an in-circuit tester. The main challenge faced by the flying prober is the accessibility for small footprint components [8]. Also the time to test one DIB takes weeks, compared to the automatic program generation testing, which takes a few hours.

This dissertation describes novel test methodologies used to test embedded passive RF components, which are a major bottleneck in testing RF DIBs, and high voltage devices. Chapter 2 describes the software architecture and algorithms to automatically test RF DIBs. It also discusses modeling of embedded passive RF components for detecting process-related defects, such as opens and shorts. Test methodology, and its implementation in the software tool along with simulation and measurement results including board coverage are also presented. Chapter 3 describes leveraging the principles of RADPro, developing new algorithms, and modifying the existing software architecture to create High Voltage Program Generation Tool (HVPro) which automatically generates test programs for high-voltage devices and DIBs. This chapter also describes the test challenges associated with high-voltage devices, development of hybrid MOS-π model for High Voltage Laterally Diffused Metal Oxide Semiconductor (HV-LDMOS), and fault models for structural defects. Chapter 4 presents a novel test technique using a noise-reduction scheme to test HV-LDMOS. This test technique overcomes the test challenges pertaining to power supply and tester system noise and its inherent advantages over conventional test methods are also presented. Chapter 5 presents the implementation of the noise reduction scheme to test a MOSFET driver IC with a 700V LDMOS. Test simulations were performed by building a prototype test setup and making hardware measurements for breakdown and leakage tests. Chapter 6 presents an alternate test technique to test HV-LDMOS using low-voltage stimulus, by developing electrical and fault models. These models are based on device physics fundamentals and reliability test principles, and are used to perform transmission line pulse (TLP) simulations. Chapter 7 discusses testing high-voltage DIBs using HVPro, and charge extraction in DIBs using ESD protection devices. This chapter presents a novel protection

scheme for HV-LDMOS using p-type field effect transistor (PFET) and SCR that employs a unique triggering mechanism and an additional discharge path through the leakage resistor. Finally, Chapter 8 presents the conclusion and highlights future directions.

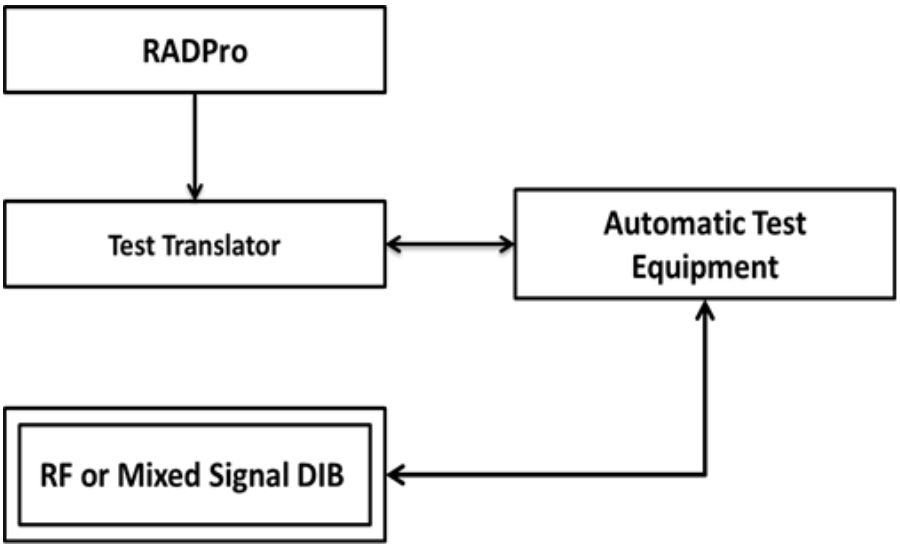
CHAPTER 2

DEVELOPMENT OF TEST TECHNIQUE FOR RF DEVICE INTERFACE BOARDS

2.1. TEST APPROACH AND SOFTWARE TOOL ARCHITECTURE

A typical troubleshooting technique for a DIB involves manually writing tester-specific codes to test circuits on a DIB. This process takes days and even months for multi-site DIBs. Our approach is to automate this troubleshooting process, thus reducing time and test cost, and become competitive in terms of well tested, cheap and early availability in market as shown in Figure 3.

Figure 3. Block Diagram of an Automatic RF DIB Setup [9]



In order to do this properly, test generation and execution have been automated to avoid labor-intensive and time-consuming manual programming by developing a software tool called RADPro for the complete automation of DIB testing.

2.2. RF Analyzer and Diagnostic Program Generator (RADPro)

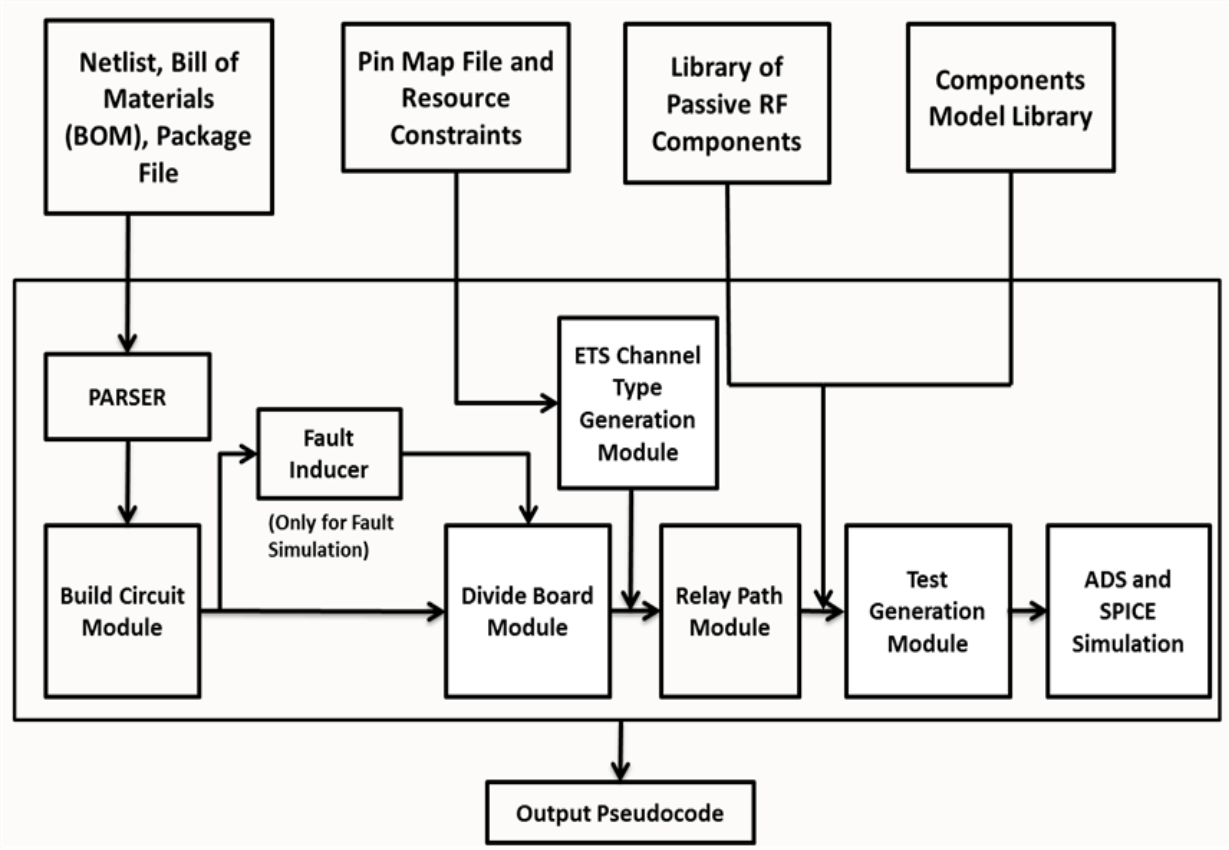
This diagnostic software tool was originally developed for debugging ATE mixed-signal DIBs [4]. The original design was intended for simple DIBs, which had few relays and active components with a limited number of resources on the ATE. An RF DIB is comprised of mixed-signal and RF circuits with several component types including capacitors, resistors, embedded passive RF components, ICs and SMA connectors. The complexity of the boards is also determined by trace interconnecting these components on the board. Hence there is a need to analyze these mixed-signal and RF components and diagnose on the DIB to locate the type of fault.

The main RADPro software architecture uses the schematic information of the DIB, such as the netlist, bill of materials and pinmap files, to replicate the schematic of the board along with all the components and necessary connections. To increase the test coverage of the board at hand a model library is built for all the active and passive components in the board. The tool runs a simulation for the testable circuits in the DIB and stores the results in a lookup table. The output of the program is a pseudocode that consists of test instructions to be carried out on the ATE. After the pseudocode is converted into the native language of the tester using the VLCT bridge or test translation software as shown in Figure 3, the tests are run on the ATE and the

output is sent back to the tool, which matches the values with the lookup table and reflects a pass or fail result for each individual component in the testable circuit.

The software architecture of RADPro consists of six different modules to automate the process of testing. Figure 4 shows the architecture of RADPro and how the testing process is done for each DIB.

Figure 4. RADPro Software Architecture [9]



2.2.1 PARSER

A parser has been implemented to construct the top-level circuit from the netlist and pinmap input files. Bill of materials (BOM), Simulation Program with Integrated Circuit

Emphasis (SPICE) and Advanced Design System (ADS) model files are read to obtain component information [9, 10]. Building the board circuit also involves prior knowledge of available terminations for the board under test. This information is carried forward to the generation of testable sub-circuits. The parser also verifies whether the input files are in the required format. Once the input files are processed, the tool proceeds to build the circuits as present in the DIB. The termination information of the board is obtained from the pinmap files, which are tester specific and also vary from board to board [11]. The tool also checks all the model files stored in the model library for active components.

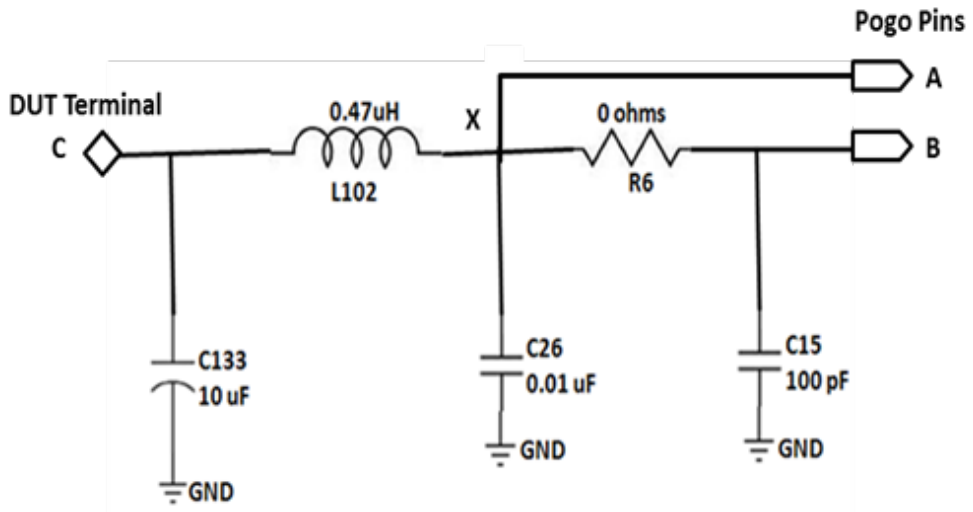
2.2.2 BUILD CIRCUIT MODULE AND FAULT INDUCER

In the build circuit module, the DIB components are segregated and stored as active and passive libraries. The active components are tested based on the availability of a model file [Appendix A], which has to be user-created to increase the test coverage of the board. First, the DIB is realized on the software level using the schematic files in the build circuit module; validation of the components present on the DIB is then performed by forming sub-circuits in the divide board module and testing them. Once validation is performed and the sub-circuits that fail the test are identified, this information is sent to the fault inducer. The passive component library is used to create a serially changing fault inducer module. In this module we automatically induce faults in the passive components of the board to obtain possible fault simulation values. These results are stored in the lookup table and compared with the actual results measured with ATE hardware.

2.2.3 DIVIDE BOARD MODULE

Using the partition algorithm, we divide the board into small sub-circuits. The output of the build circuit module is used to divide the board into sub-circuits based on the availability of terminals for stimulating and measuring test signals. Figure 5 shows a typical RF DIB circuit.

Figure 5. Case Study for a Device Interface Board Circuit [9]



Let us consider the circuit shown in Figure 5. We can use the following partition algorithm to divide the board into sub-circuits:

1) Choose a node X that is connected to a pogo pin of the tester using the information from the pinmap files as shown in Figure 5. Mark this node as visited.

2) Find all the components linked to the start node and group them as a single block. As an example, nodes A and B are connected to start node X.

3) Repeat step 2 for all the nodes in the previously grouped block until another termination node is encountered. Mark this node as a visited node.

4) Mark the path between the start node and the node with termination as a sub-circuit.

5) For Figure 5, paths A-X-C and B-X-C are the partitioned sub-circuits.

6) Repeat steps 3 and 4 until all the nodes are marked as visited.

Once the circuits are divided into sub-circuits, those that contain relays are tested separately for the different operational modes of the relay.

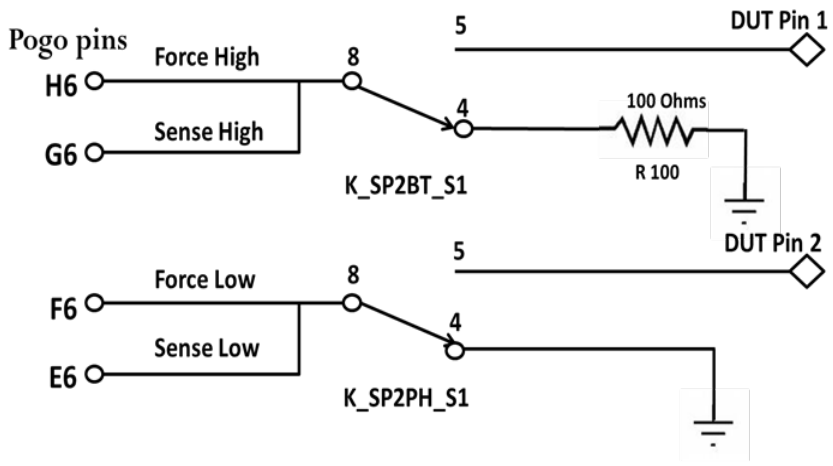
2.2.4 RELAY PATH MODULE

This module validates the functionality of relays with testable circuits. The circuits with relays are tested by switching the relay ON or OFF to check for faults in the relay circuits. We have used stuck-at-0 and stuck-at-1 fault models.

2.2.5 CHANNEL TYPE GENERATION MODULE

This is a special module to accommodate floating ground used in the high-voltage testing performed in some tester platforms, such as Eagle Test Systems (ETS). In ETS, the source meters and the measuring instruments do not share a common ground, and this is used as a platform to apply and measure higher voltages. In such cases, the tool must specifically use the high or low channels, available at the respective pogo pins. This information is taken from the pinmap files [Appendix B] and the channel type is created for each pogo pin to determine whether it is high or low and whether force or sense activity is taking place at the pin. Figure 6 shows a typical DIB circuit with floating ground used in ETS.

Figure 6. Case Study for a DIB Circuit with Floating Ground used in ETS [9]



ETS testers can perform differential testing. To facilitate a differential testing capability, the tester systems have a floating ground concept in which the signal sources are not connected to the tester ground, but to a virtual ground, so that they can be used as a pedestal for performing high-voltage testing.

The pinmap file of the DIB carries the information on the pogo pin, which provides access for testing as well as the specifications of the hardware resources on the tester side. Using this information from the pinmap file, we assign the high and low sides of a testable differential path [12]. However, the partition algorithm used for ETS boards is different from that of other DIBs. By grouping the high and the low sides into one testable circuit, the circuits are partitioned into differentially testable sub-circuits. Tests were performed on these DIBs and the pseudocode was obtained as shown in Figure 7.

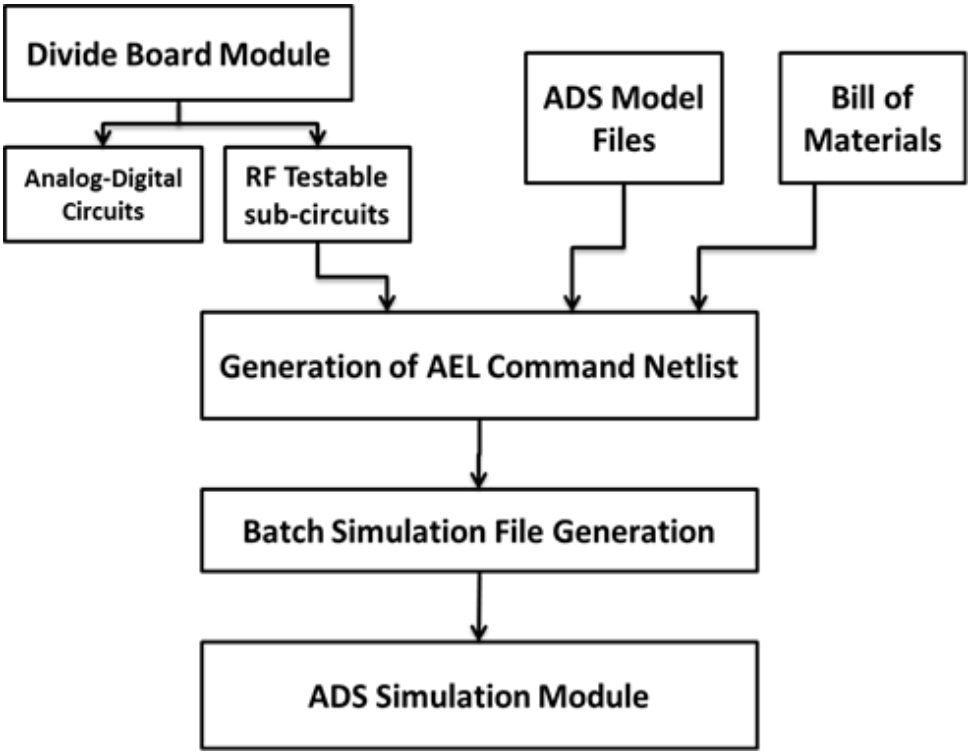
Figure 7. Pseudocode for Differential Testing [31]

```
*****POWER TO GROUND ONLY TEST*****
CONDITION(VERIFY COMPONENT = JP19-1_2)
FCMV(forced current = 1e-4 A, force high pin = CH-J1-I16,
sense high pin = CH-J1-H9, type = force high)
FCMV(forced current = 1e-4 A, force low pin = LowPin_Num3,
sense low pin = LowPin_Ref3, type = force low)
COMPARE_LIMITS(lower limit = 0.06 V, upper limit = 1.99 V,
nominal value = 0.075 V, tested pwr node = +3P3V_MB)
```

2.2.6 TEST GENERATION

This module prepares the ADS and SPICE netlists for each testable circuit. The ADS simulation is performed as a batch simulation. The ADS netlist consists of Applications Extension Language (AEL) commands, which are generated for each testable circuit as shown in Figure 8.

Figure 8. Process of Generating the ADS Netlist



Simulation involves fault modeling and test technique. We have developed a test technique to perform fault analysis on RF DIBs. The results of the simulation are stored in the lookup table and matched with the output of the ATE to determine whether a component has passed or failed the test.

2.2.7 ADS/SPICE Simulation Module

The output of the divide board module gives a set of testable and non-testable circuits using the partition algorithm. To analyze the RF components in the testable circuits, we have performed fault modeling of the commonly present RF components and surface mount passive

components. The simulations are run for a fault-free circuit and also by automatically inducing faults using the serially changing fault inducer module [Appendix C].

After automatically inducing the faults for all testable circuits, we segregate the RF circuits from the mixed-signal circuits. SPICE simulation is run for mixed-signal components. The tests run on mixed-signal circuits are force voltage measure current (FVMC), force current measure voltage (FCMV) and force current measure voltage with delay time (FCMVDT). ADS simulation is run for testable circuits with embedded passive RF components. We performed S-parameter simulations for RF components to generate the force power measure voltage (FPMV) test. The test technique we have developed for detecting faults in RF components is Multi-tone Dither Test. Using the fault models and the test setup developed; we are able to detect faults in mixed-signal and embedded passive RF components.

2.3 FAULT MODELING

Once the testing process has been completed for a testable circuit, we diagnose the DIB. We have developed fault models that can be induced to create opens and shorts in embedded passive RF components present on the DIB.

We have also built a model library, including the different SPICE and ADS models that can perform simulations for the testable circuits. The different fault models are stored inside this model library, which helps us to build the simulation setup for each testable circuit. The open connection in traces for analog-mixed signal boards are modeled with a high resistance and shorts are modeled with a capacitance to ground. The stuck-at-relay faults are also modeled with a capacitance to ground, if the relay is stuck at 0 and resistance, if stuck at 1.

RF traces are modeled using the line calculator in ADS, and the fault conditions are introduced into the model synthesized by the line calculator. An RF trace, acting like a band pass filter, is modeled as a passive band pass filter. A lookup table with measurements of bandwidth, amplitude, center frequency, etc., for each possible fault occurrence is created by simulating the response for different missing components. This is compared with the actual response values to match the type of fault occurring. A balun transformer is commonly used in RF DIBs to connect two microstrip lines with different impedances to balance signals. They convert a balanced RF signal to an unbalanced RF signal.

We have considered a balun transformer formed by an RF trace with open and short faults occurring on the trace at different positions on its surface and then prepared a lookup table. Consider the following circuit in an RF DIB with embedded passive components, such as a balun transformer and surface mount technology (SMT) resistors and capacitors. We performed an ADS simulation and created a lookup table. Figure 9 shows the actual RF DIB circuit with process-related defects induced at certain positions respectively. The dark lines indicate metal traces inside the layers of DIB to form an impedance-matched RF circuit. We performed a frequency sweep and used the data obtained at 5GHz as this shows the maximum difference in measurements. A lookup table is shown in Table 1 with different possible fault measurements, but we see some effect of aliasing. This shows that we were able to find the faulty component; however, localizing the fault in embedded passive components in these conditions was difficult.

Figure 9. Testable RF Sub-Circuit with Open and Short Process-Related Defects at Position 1 and 2 in the Balun Transformer (Dark Lines Indicate Embedded RF Lines) [13]

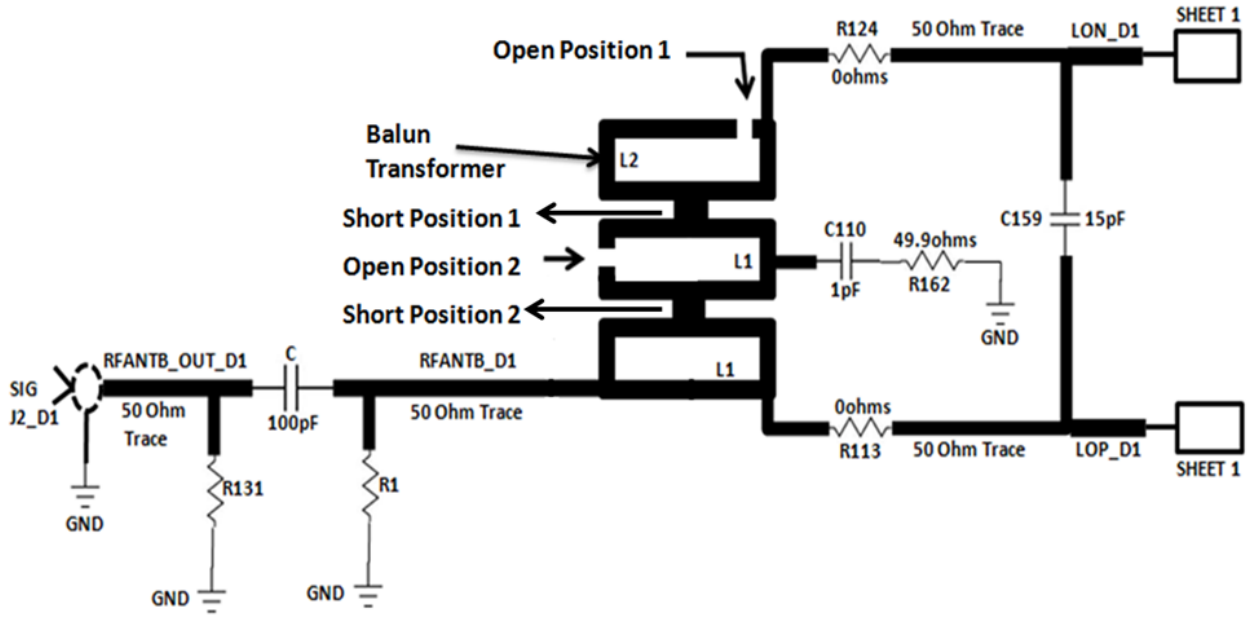


Table 1. Lookup Table to Identify Defects [13]

Name	Power Gain (dB)
Fault Free	-40
Open at Position 1	-45
Open at Position 2	-52
Short at Position 1	-54
Short at Position 2	-56

Depending on the value of the power measured, we match the fault to other similar faults. In cases where two or more faults share the same values at a given respective frequency for

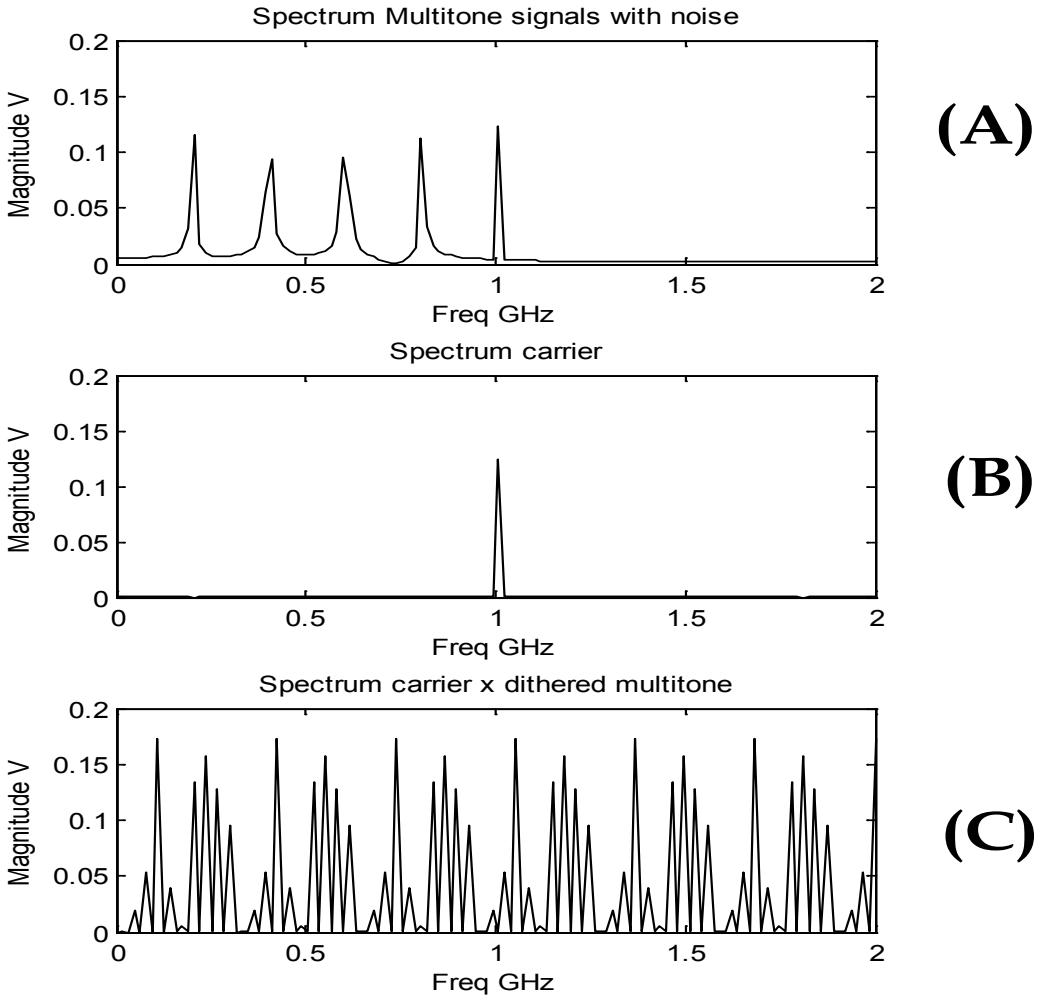
measurement, as shown in Table 1, we call it aliasing and have to perform other measurements to differentiate between the faults. Table 1 could be used for further diagnosis of the circuit shown in Figure 9.

2.4 MULTI-TONE DITHER TEST

Previously, we employed an RF power sensor to monitor the power loss at the DUT terminal for each testable circuit. A defective circuit would contribute to lower power reaching the DUT terminal than in the case of a fault-free DIB circuit. However, some defects are difficult to recognize using this technique. The problem of aliasing also arises when two or more faults are difficult to distinguish.

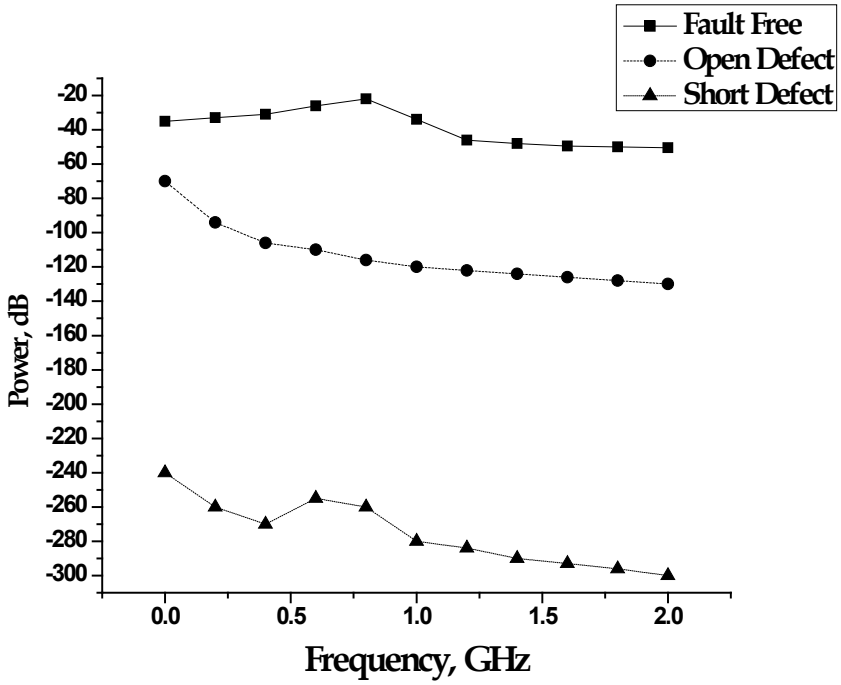
Hence, we developed a better technique called dither testing where we use a multi-tone signal and modulate it with the RF test signal, which overcomes the problem of aliasing and multiple faults, and is able to identify faults on DIB with a higher level of accuracy. The frequencies of the multi-tone and RF source signals are maintained at the same level and Gaussian noise is added to the multi-tone signal [14, 15]. The Gaussian noise is added to the multi-tone signal such that, it increases the sensitivity of the test stimulus to process-related defects, such as opens and shorts. Typically, a signal with very low magnitude of amplitude 0.25 V and a mean variance of 0.18 is used as Gaussian noise. The prepared test signal is given to the circuit under test (CUT) and the output power spectrum is monitored. The test stimulus has a multi-tone signal with randomly changing phases between the individual tones. The input test signal, as shown in Figure 10, depicts the signal in frequency domain.

Figure 10. Input Test Signal for Dither Testing: (A) Multi-Tone Signal, (B) RF Carrier Signal, (C) Multi-Tone Signal Modulated with the RF Carrier Signal [13]



The simulation was run and the output power spectrum was monitored for a fault-free circuit vs. induced open and short faults. The simulated output power spectrum using the dither testing technique is shown in Figure 11.

Figure 11. Power Spectrum of Dither Testing [13]

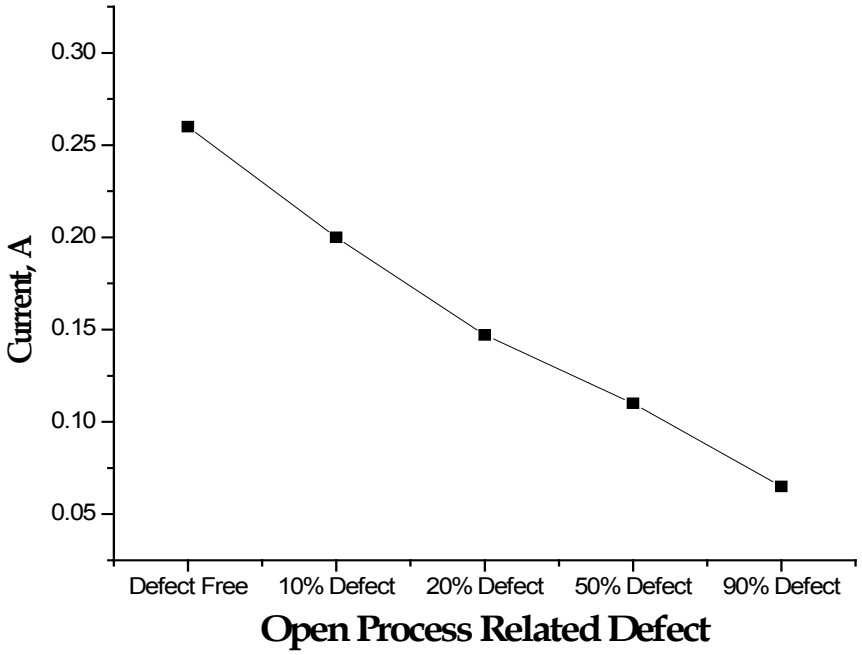


2.4.1. PHYSICAL PHENOMENA

There is a large difference in power loss seen at the output when there is a process-related defect in the CUT. We compared the results of power sensor testing with the dither testing and were able to detect process-related defects effectively. To understand this significant difference in power loss when two different test signals were used, we had to relate it to a physical phenomenon. We studied the multi-tone test signal given to the CUT to understand its advantages over a single-tone test signal as used in the power sensor testing technique. Therefore, when there is a defect in the DIB circuit that has missing or misplaced discrete passive components, there is a phase change in the output response that is identified when we

measure the RMS and peak values at the output of the DIB circuit using a peak-to-average ratio or envelop detector. Analysis was performed on the CUT and the output current was measured as shown in Figure 12.

Figure 12. Output Current for Defect-free vs. Defect-Induced Circuit



The output current for the CUT decreased with an increase in metal shavings confirming the increase in resistance. There was a clear attenuation in current when a defect was introduced into the CUT. Hence, a multi-tone signal was applied and the output voltage waveform was monitored for a respective tone; a phase shift was noticed when a defect was introduced. This phase shift varied with the type of defect introduced and also depended on the number of tones used in the multi-tone signal. The phase shift is in the order of ϕ_k, where k is the number of a

particular tone of the multi-tone signal. This phase shift contributes to a change in the RMS value of the output voltage between a defect-free and defective circuit. Hence multi-tone signals could effectively detect the presence of a defect in the circuit [16, 17]. To effectively utilize this phase shift and its effective change in RMS value, we calculated the peak-to-average ratio of the CUT using the following approximation formula [18].

1. The multi-tone signal consists of N tones of sinusoidal waves, each separated by an angular frequency (change in phase) [19, 20]. The phases for the N tones are generated randomly over a Gaussian distribution. Each individual tone is represented by the product of its amplitude (a_k) and angular frequency (ω). The angular frequency is represented as a complex number. The multi-tone signal in complex form is mathematically represented by the following equation – Eq (1).

$$a(t) = \sum_{k=0}^{N-1} a_k . e^{jk\Delta\left(\omega_k + \omega_0\right)\cdot t + \varphi_k} \qquad \text{Eq (1)}$$

2. The first tone is considered as the fundamental with angular frequency of ω_0. The change in angular frequency is represented as $\Delta\omega_k = 2\pi/T_k$ where T_k is a period [21, 22, 23, and 24]. The multi-tone signal is in complex form but only the real part is observable while making test measurements, therefore Eq (1) is reduced to its real part and the imaginary part is ignored [25, 26, and 27]. Therefore, a new multi-tone signal is represented as in Eq (2).

$$a(t) = \sum_{k=0}^{N-1} \left|a_k\right| \cdot k\Delta\cos(\omega_0 + \omega_k)t + \varphi_k \qquad \text{Eq (2)}$$

3. Peak-to-average of a signal is denoted

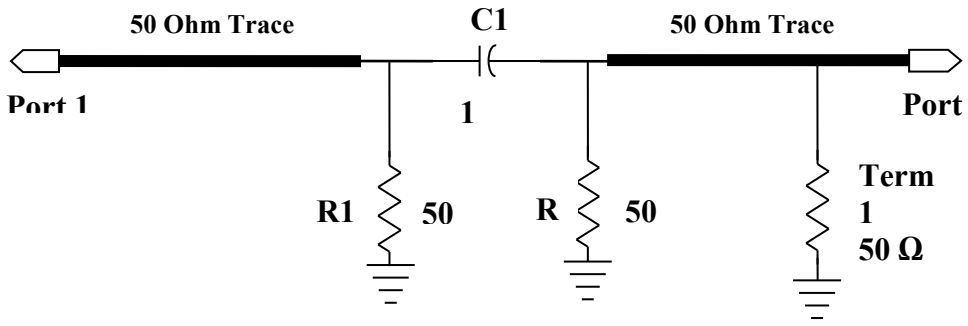
$$P.A.R = \frac{V_{peak}}{V_{rms}} \qquad \text{Eq (3)}$$

$$V_{peak} = \max_t \{|a(t)|\} \quad \text{Eq (4)}$$

$$V_{rms} = \sqrt{\lim_{x \to N} \frac{1}{2x} \int_0^N a^2(t)dt} \quad \text{Eq (5)}$$

These equations were used to calculate the peak-to-average ratio in MATLAB and ADS simulations. The sensitivity of the test was analyzed in an attempt to optimize the multi-tone signal generated [28]. We performed dither testing simulations on the CUT shown in Figure 13.

Figure 13. Circuit under Test (CUT) for Dither Testing [13]

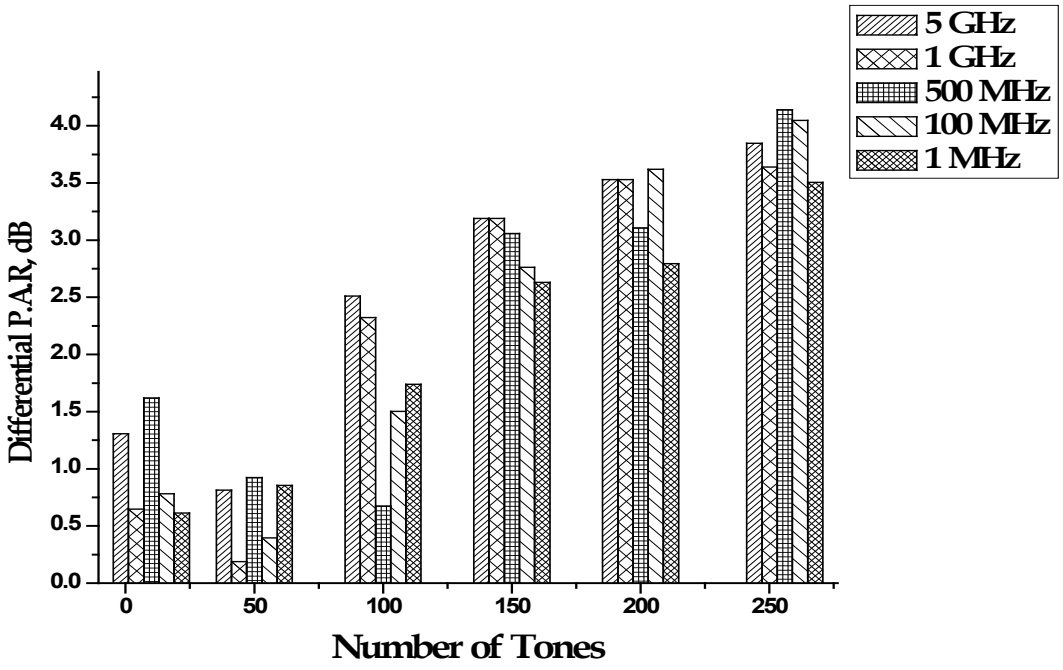


We introduced a near open defect in the input embedded passive metal trace. Table 2 shows the difference in peak-to-average ratio obtained between defect-free and near open defect for various test frequencies and an increasing number of tones of the test signal; the results are plotted in Figure 14.

Table 2. Differential Peak-to-Average Ratio for Varying Test Signal Frequencies

# of Tones	1 GHz	5 GHz	500 MHz	100 MHz	1 MHz
10	0.65	1.31	1.62	0.78	0.61
20	0.65	1.15	1.62	0.78	0.67
50	0.19	0.81	0.93	0.39	0.85
100	2.32	2.51	0.67	1.50	1.74
150	3.19	3.19	3.06	2.76	2.63
200	3.53	3.53	3.11	3.62	2.79
256	3.64	3.85	4.14	4.05	3.50

Figure 14. Difference in Peak-to-Average Ratio between Defect-Free and Open-Defect in DIB circuit [13]

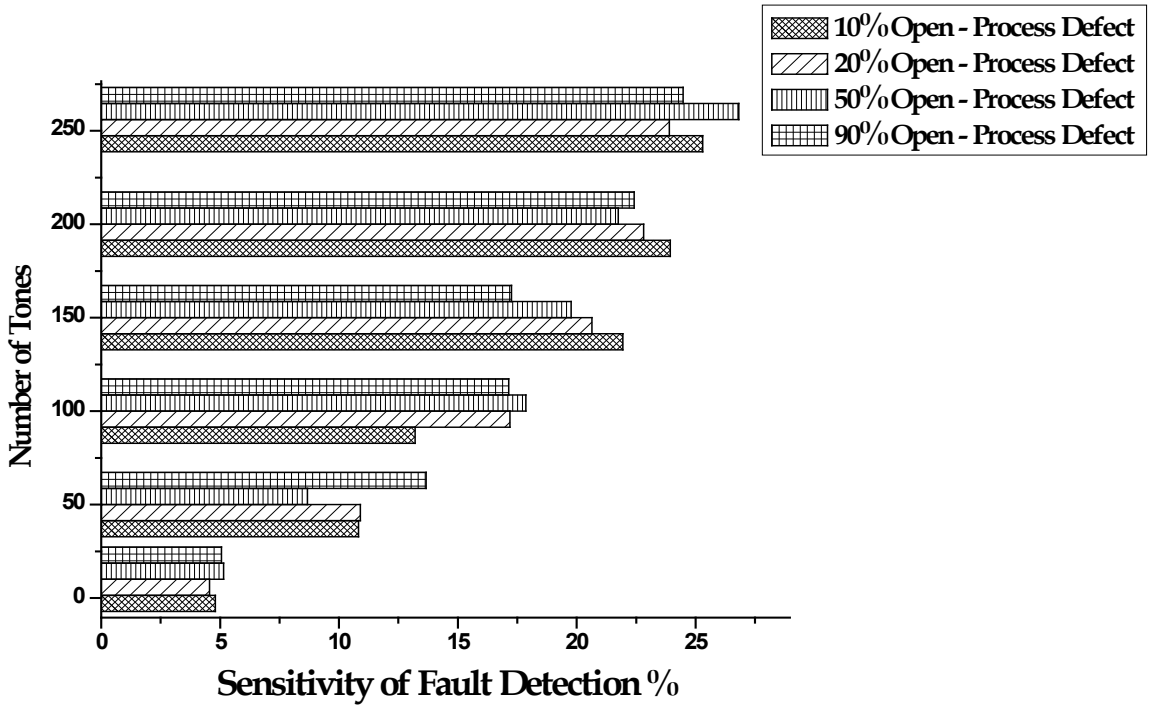


From the simulation results, the CUT showed an effective difference at 1GHz and hence the number of tones had to be optimized based on the CUT by performing a sensitivity of fault detection simulation by varying the number of tones for the test signal at 1GHz; and their sensitivity percentage is shown in a bar graph in Figure 15.

Sensitivity of Fault Detection % = No. of tests open defect is identified / Total no. of tests run.

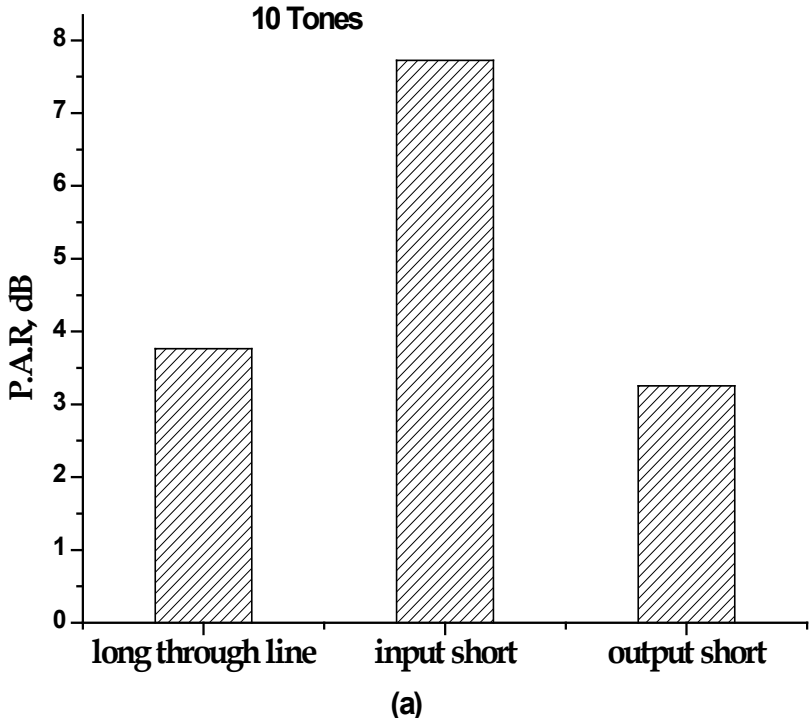
The phase for each individual tone is obtained by using a random number generation with a fixed spacing interval or variance (range of 0.01 to 0.15). This spacing interval is varied in each test run to identify the induced fault. So if we run 10 tests and 4 tests are able to identify the fault induced then sensitivity of fault detection percentage is 40%. For each of the 10 trials run this spacing between the tones is varied to identify the best possible combination for our synthesized input test stimulus.

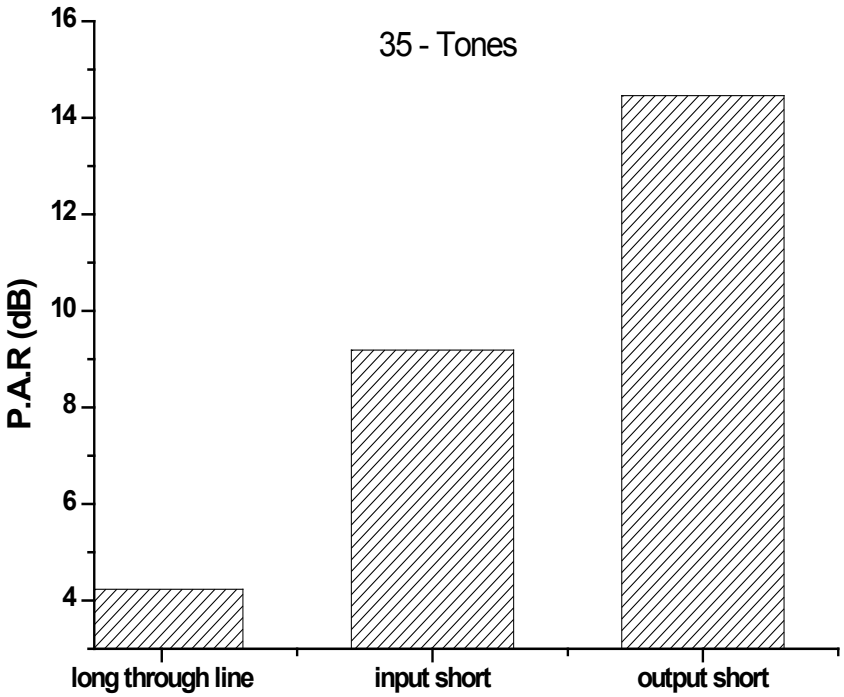
Figure 15. Fault Coverage [13]



An increase in the number of tones causes higher difference in peak-to-average ratio between defect-free and defective circuits, as seen in other simulation results [29, 30]. Hardware testing and validation was performed on a DIB with a 20 cm long resistive trace to verify the simulation results, and compare them to the outputs of the RF sensor technique for a long through line vs. input shorted and output shorted as shown in Figure 16. Dither testing was comparatively more sensitive in identifying process defects in the embedded RF passive components. The results are as shown in Figure 16.

Figure 16. Dither Testing Result for Embedded Passive RF Components (a) 10 tones, (b) 35 tones [13]





(b)

In the experimental setup using the envelope detector, we measured the peak and rms voltage outputs for a testable circuit. These output results were used to obtain the peak–to-average ratio of the testable circuit using Eq. (3). We noticed a significant change in the peak-to-average ratio values between fault-free and fault induced circuits. A multi-tone dither test was performed using RADPro for a CUT; pseudocode was generated as shown in Figure 17.

Figure 17. Pseudocode for Circuit under Test using Multi-tone Dither Testing [13]

```
*****MULTI-TONE DITHER TEST*****
CONDITION(circuit id = 1001, component tested = C317, test frequency = 1 GHz, number of tones = 15, multi-tone amplitude = 5 V, test pin = driving pin, termination pin = grounded pin)
MTDT(force voltage = 250 e-3 V, driving pin = J14, termination pin = IFN_D1, type = crest factor measurement)
COMPARE_LIMITS(CF lower limit = 4.0895 dB, CF upper limit = 4.5485 dB, CF nominal value = 4.135 dB)
*****MULTI-TONE DITHER TEST*****
CONDITION(circuit id = 1001, component tested = ADT4-1WT, test frequency = 1 GHz, number of tones = 15, multi-tone amplitude = 5 V, test pin = driving pin, termination pin = grounded pin)
MTDT(force voltage = 250 e-3 V, driving pin = J14, termination pin = IFP_D1, type = crest factor measurement)
COMPARE_LIMITS(CF lower limit = 4.0895 dB, CF upper limit = 4.5485 dB, CF nominal value = 4.135 dB)
```

2.5 Test Coverage and Limitations

The test coverage obtained on a DIB depends on various contributing factors such as the accessibility, availability of models for various components in the circuits and extensive library of fault models. Modeling of embedded RF circuits is extremely difficult as the user must prepare them with the dimensions specified in the DIB schematics. Using these models we can generate various fault models that can be used for fault diagnosis. Once these models are stored in the model library, RADPro can access them during the test generation process. DIBs contain hundreds of components such as jumper wires, SMT, resistors and capacitors; these all must be modeled for RADPro to perform testing. Hence the model library has to be extensive and is decisive in the test coverage obtained using RADPro.

We worked with two different DIB boards used on the ETS with RADPro. The two different DIBs run on RADPro were highly successful, which indicated that all the components were tested. Furthermore, the fault coverage and fault diagnosis percentages with respect to each

component type tested, along with the total board components, was reported by RADPro shown in Table 3.

Table 3. Test Coverage Statistics obtained for DIB using RADPro [13]

Components	**Total # of Components in BOM**	**Total # of Testable Components**	**% of tested components**	**% of Fault Coverage**	**% of Fault Diagnosis**
Capacitors	193	174	90.2	84	79.2
Resistors	67	54	80.5	78	76.9
Relays for functionality	23	19	82.6	79	77.1
SMA Connectors	31	31	100	100	100
Diodes	56	45	80.4	76.5	71.9
Jumper Wires	27	23	85.2	83	82.3

The test coverage percentage depends on the accessibility provided by the board [7, 8]. Tests are run only for circuits that originate at a pogo pin and terminate at a DUT pin as these two pins are used to provide input stimulus and measure the output response [31]. In addition, the total number of active components depends on the availability of their model in the model library, which the users have to keep updating to increase the board coverage. Table 4 provides the test coverage on ETS DIB boards with differential testing capability.

Table 4. Summary of Test Coverage [13]

% Coverage	**DIB 1(6486024C)**	**DIB 2(WG2K_ETS_364)**
Total number of components	1174	1058
Capacitors	67	81
Resistors	52	74
Inductors	29	23
Relays	47	58
Overall Coverage	71.3	84.5

The above results indicate that the test coverage varies over a range of about 70% to 85%. This is due to accessibility that the DIB provides [13, 32]. Thus we achieved extremely satisfactory fault coverage in testing DIBs using our software tool and the diagnosis produced by the test techniques is highly accurate at localizing faults [33, 34].

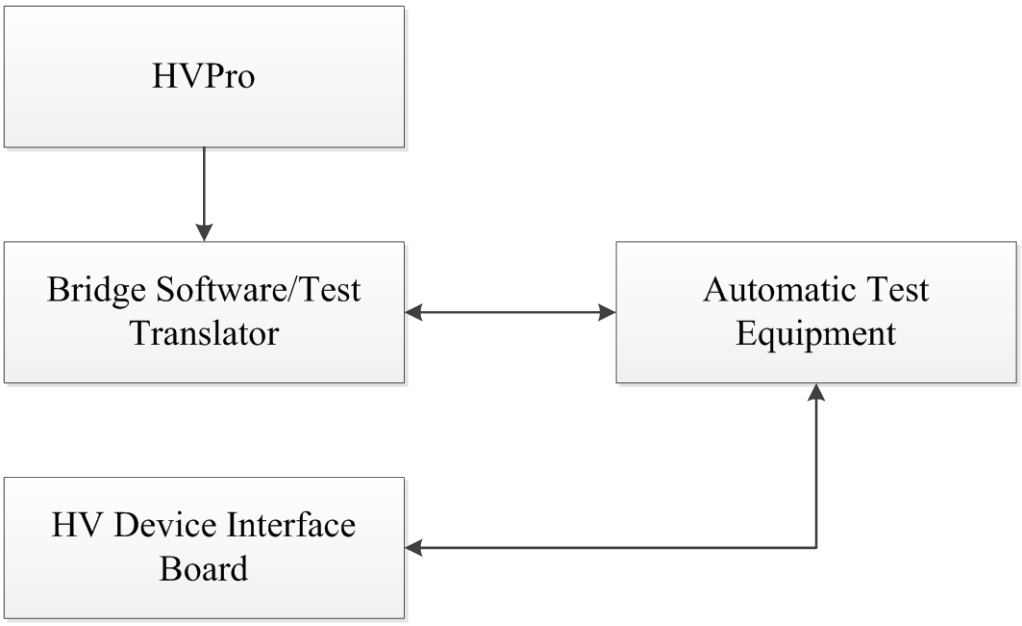
CHAPTER 3

HIGH-VOLTAGE AUTOMATIC PROGRAM GENERATION (HVPRO)

RADPro discussed in Chapter 2 was developed to automatically generate test programs for RF-DIBs. In this chapter the principles of RADPro are leveraged to develop a new software tool called HVPro to automatically generate test programs for high-voltage devices and their DIBs. On the production floor a basic test setup for high-voltage devices involves the use of an ATE; typically ETS platform or alternate tester platforms with high-voltage test capabilities. Testing is performed on high-voltage devices using a HV-DIB, which facilitates providing a test stimulus and measure the output response. This is a labor intensive and cumbersome process. HVPro has been developed to automatically generate test programs for both high-voltage devices and DIBs to drastically reduce test cost and time. It also reduces engineers' manual interaction with the ATE.

The test hardware consists of a tester platform, DIB and DUT. The software uses the noise reduction scheme presented in Chapter 5 of this dissertation. We have developed a new software tool HVPro as shown in Figure 18, to automatically test both the DIB and the DUT.

Figure 18. Block Diagram of Automatic HV-DIB Testing



3.1. HIGH-VOLTAGE TESTING

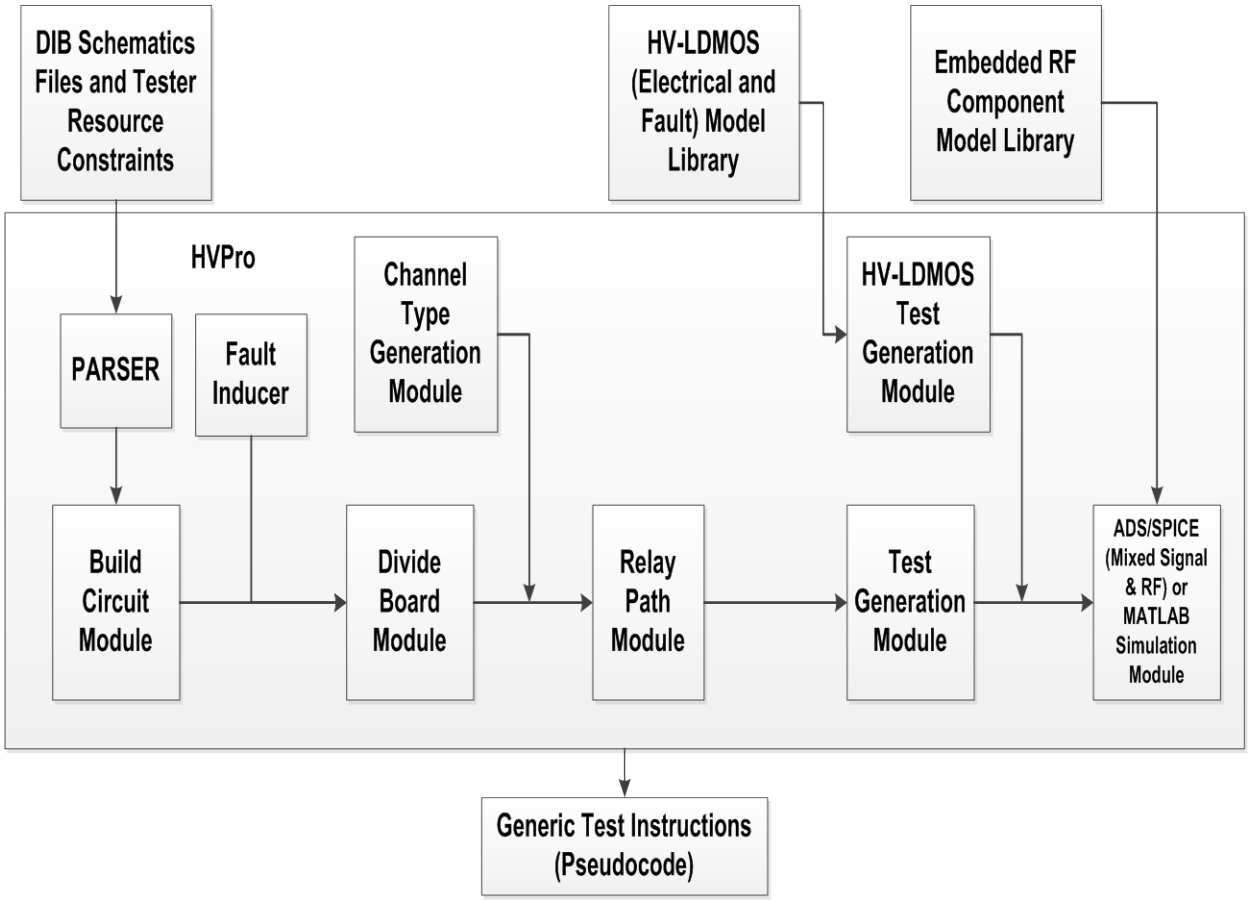
Production test development and performing parametric test measurements on high-voltage devices are potentially dangerous tasks. A typical high-voltage device has a drain to source voltage (V_{ds}) rating greater than 200 V DC up to several hundred volts, and in certain test cases high currents ranging from 1 A to 10 A might also be present. The ratings of high-voltage devices are expected to increase in future products; hence, there is an urgent need to automate the testing process for high-voltage devices so that manual interaction with high-voltage test equipment is minimized. The software tool we have developed (RADPro) for RF DIB Testing already has the capability to perform diagnosis on ETS boards, which are typically used for high-voltage testing. RADPro has been enhanced to perform both functional testing of high-voltage devices as well as fault detection and diagnosis on high-voltage DIBs. Testing high-voltage

devices involves the use of DIBs with analog circuits having components with high-voltage ratings; hence, it is extremely vital to perform diagnosis of the high-voltage DIB before performing high-voltage device testing itself. Currently, there is no standard algorithm or software tool that can automatically perform component-level diagnostics of high-voltage DIBs. The principles of RADPro were leveraged to develop an enhanced software tool for testing high-voltage DIBs called HVPro. A major bottleneck in high-voltage device testing is that the high-voltage stimulus is applied through the DIB. The high-voltage remains on the DIBs for an extended period of time because interconnects on the DIBs act as capacitors. To overcome this problem, a new technique to discharge high-voltage on a trace line using SCR was developed. This technique employs a unique triggering mechanism with additional leakage path for charge extraction that can be automated using HVPro. To perform high-voltage device testing, it is necessary to subject the device to its maximum voltage ratings, which involves additional test resources thereby increasing the test cost and time. Hence, it is advantageous to test high-voltage devices using non-conventional low-voltage stimulus that can drive the device to the same level as the conventional high-voltage stimulus. New test techniques and algorithms were also developed for testing high-voltage devices using non-conventional low-voltage stimulus, such as impulses and wavelets.

HVPro is a revised version of the previously developed software tool RADPro. New algorithms were developed to incorporate high-voltage test capability. This tool is designed to automatically generate electrical and fault models for structural defects in high-voltage devices and perform testing. The basic architecture of HVPro is similar to RADPro, but contains with

additional modules to enable the tool to automatically generate test programs for both HV-DIBs [Appendix D] and high-voltage devices. The architecture of HVPro is shown in Figure 19.

Figure 19. HVPro Software Architecture



The software architecture of HVPro consists of seven different modules to automate the process of testing. The parser, build circuit module, divide board module, relay path module and test generation module are inherited from RADPro. HVPro is designed to perform both DIB as well as device testing. The HV-LDMOS model library automatically generates models and computes their transfer function using MATLAB scripts. The HV-LDMOS test generation module generates MATLAB scripts to perform functional device testing where the device is

represented by its transfer function. The ADS/SPICE/MATLAB simulation module is modified so that HVPro is capable of performing high-voltage test simulations using the noise reduction scheme.

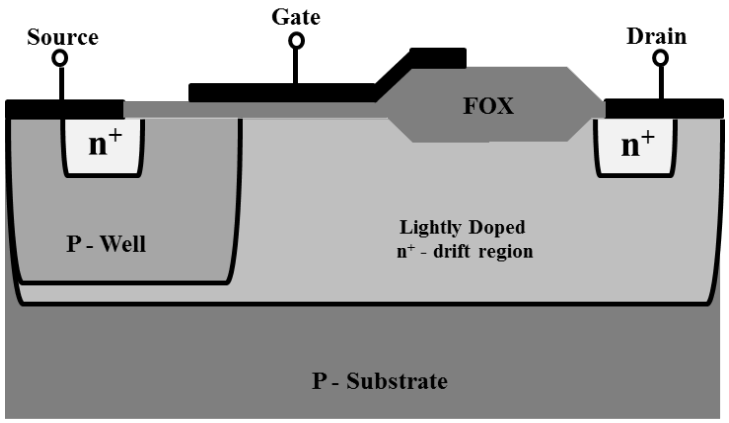
3.2. HIGH-VOLTAGE DEVICES

The semiconductor industry has been delivering on Gordon Moore's prediction of doubling the transistor density every 18 months and has done so for nearly half a century. As the computing power soared, the need to integrate more product functionality into a single chip led to "More than Moore." The difference was that Moore had referred to transistor scaling, but "More than Moore" deals with scaling the printed circuit board down to a single chip [35]. This is achieved by a high level of integration. Power devices that were on the printed circuit board are increasingly integrated into the IC itself. One of the first areas to benefit from "More than Moore" concept is power management. The combination of computational power, programmability and high power driver circuits provide a platform to control and manage power [36]. The widely accepted solution to high voltage tolerance for deep submicron is the development of LDMOS. HV-LDMOSs are extensively used for high voltage applications due to its advantages over other metal oxide semiconductor structures. HV-LDMOSs are being widely used as output drivers in numerous applications for smart phones, power amplifiers in base stations and motor drives in automotive applications.

HV-LDMOSs are structurally different from CMOSs, due to the presence of a lightly doped n-drift region at the drain terminal. The structure of HV-LDMOS is shown in Figure 20. These transistors use the lightly doped n-drift region to separate the standard drain terminal of a

MOS from the gate-channel region. The n-drift region provides a voltage drop between the drain terminal and gate-channel, thus decreasing the electric field across the gate oxide, and keeping it below the oxide breakdown levels. Variations of specific dimensions, such as Field Oxide (FOX) and doping concentration of these transistors, enabled us to achieve high breakdown voltages [37].

Figure 20. Structure of HV-LDMOS [38]



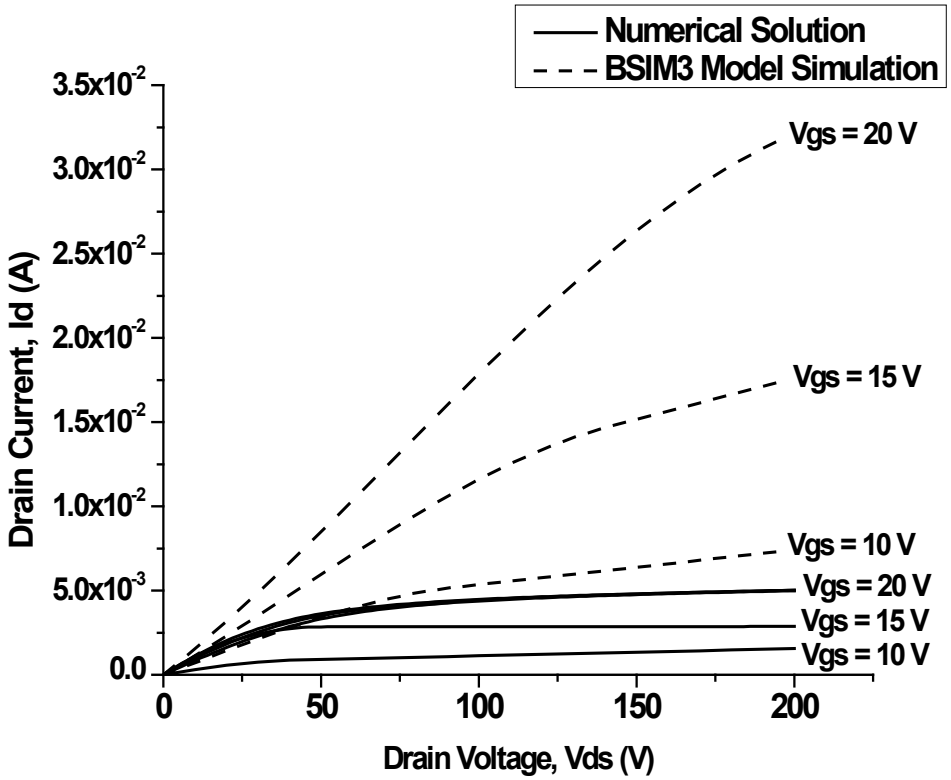
HV-LDMOSFET

3.3. Drawback of Existing BSIM3 Model for HV-LDMOS

There are various intricate structural differences between a HV-LDMOS and conventional CMOS. The doping concentrations, well depth, thickness of field oxide and gate-channel length of HV-LDMOS are all comparatively much larger than that of low-voltage MOS. The drain terminal is in a more lightly doped region than the gate-channel, leading to the quasi-saturation effect. This laterally diffused structure increases the parasitic resistance at the drain terminal, and causes the voltage between the drain terminal and gate-channel to drop, thereby

maintaining the electric field below the oxide breakdown level. A FOX layer provides isolation between the drain and gate terminals. This layer tapers towards the drain terminal as seen in Figure 20. The tapering of FOX allows for a low electric field between the drain terminal and gate-channel, thus preventing breakdown. This is known as reduced surface field (RESURF) effect. These additional features of the HV_LDMOSs act as major bottlenecks in device simulation using the BSIM3 model. Figure 21 represents the I-V curves of HV-LDMOS.

Figure 21. Comparison between Numerical Solution of Drain Current Equations and BSIM3 Model Simulation [39]



The solid line represents numerical solution data obtained by solving the drain current equations, while the dotted line represents simulated data using the BSIM3 model. The

numerical solution is obtained using information in the datasheet, as shown by the following high level algorithm, and is computed using MATLAB.

```
Begin
 set Temperature (T) = 323 K
  set Nominal Temperature (TNOM) = 298 K
   compute temperature dependant parasitic resistances Rg, Rd, and Rs.
    for j = 0:5:20
     set gate-source voltage (Vgs) = j
      for i = 0:5:200
       set drain-source voltage (Vds) = i
        compute gate-drain potential difference (Vgd)
         calculate transistor turn-on threshold limit (Vto)
          calculate field-oxide capacitance (Cox)
           set transconductance parameter (kn)
            calculate drain current (Id)
             set early voltage effect from datasheet
calculate output resistance (r0)
 return
plot I-V characteristics
 hold
  return
end
```

The parameters for numerical solution can be calculated using the following equations:

Parasitics resistance for gate terminal is

$$R_G = R_{G_0} + R_{G_1}.(T - TNOM) \qquad \text{Eq(6)}$$

Parasitic resistance for drain terminal is

$$R_D = R_{D_0} + R_{D_1}.(T - TNOM) \quad \text{Eq(7)}$$

And parasitic resistance for source terminal is

$$R_S = R_{S_0} + R_{D_1}.(T - TNOM) \quad \text{Eq(8)}$$

Device transconductance for the LD-MOS is given by

$$g_m = k_n.\left(V_{GS} - V_{to}\right).\left(1 + \lambda V_{DS}\right) \quad \text{Eq(9)}$$

where, k_n and λ are obtained from the datasheet.

Drain current is given by

$$I_d = \mu_n.C_{ox}.\beta.\left(V_{gst}^{VGEXP}\right).\left(1 + \frac{\lambda.V_{DS}}{V_{gst}}\right).\tanh\left(\alpha.V_{DS}\right) \quad \text{Eq(10)}$$

where, μ_n, β, α, V_{gst} and $VGEXP$ are obtained from the datasheet of the HV-LDMOS.

These equations are used to obtain the I-V characteristics of the HV-LDMOS as a numerical solution. When the gate voltage is increased beyond a threshold limit HV-LDMOSs exhibit the quasi-saturation effect: the drain current appears to saturate but then increases before actually saturating. The BSIM3 model deviates completely from the numerical solution data because it does not take the lightly doped n-drift region into account. The n-drift region increases the parasitic resistance in the drain terminal, thereby limiting the drain current. The drain current limitation is exhibited by the numerical solution of HV-LDMOS.

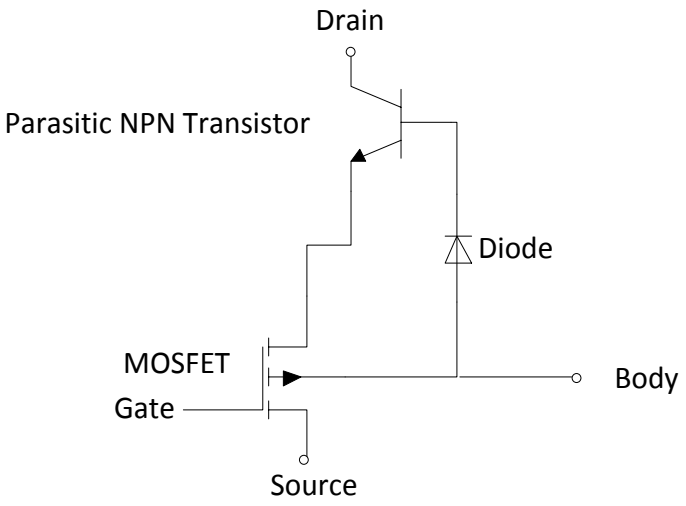
3.4. ELECTRICAL MODELING FOR HV-LDMOS

The special features of the HV-LDMOSs such as quasi-saturation and RESURF effects act as major bottlenecks in device simulation using BSIM3 model, since there are obvious differences between the simulated and experimental data using the BSIM3 model. Hence, there is a requirement for an accurate HV-LDMOS model for device simulation.

3.4.1. HV-LDMOS CIRCUIT MODEL

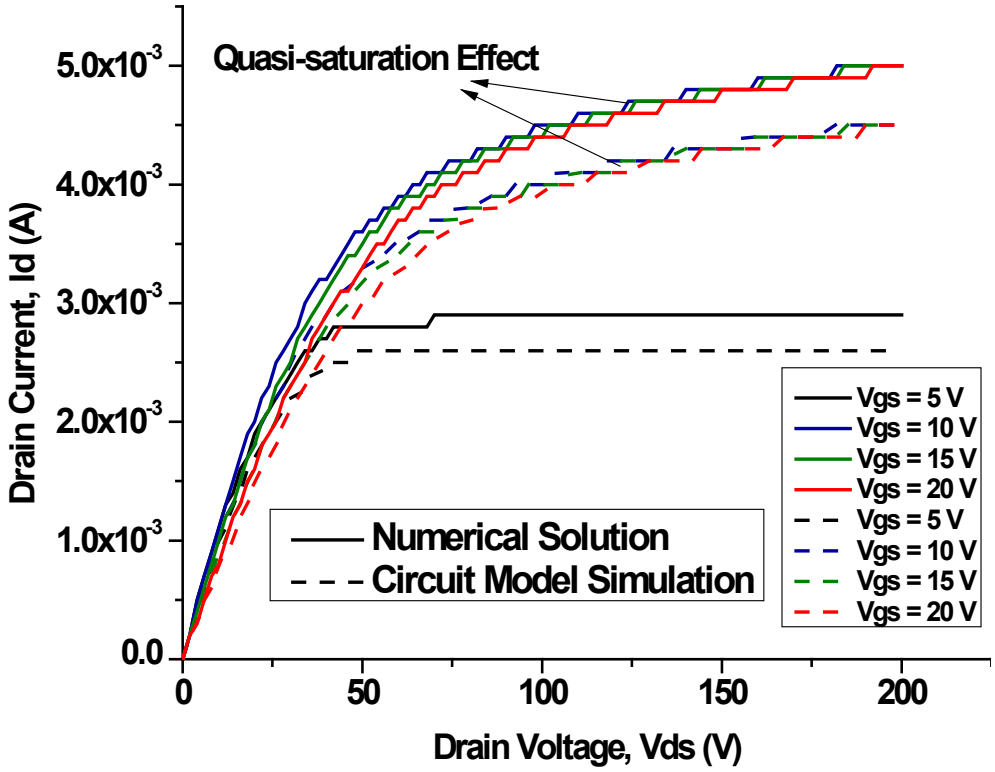
Previously various research efforts have attempted to model HV-LDMOS, such as modifying the BSIM3 model function equations and creating new simulators for HV device simulation [40, 41], redefining the physical meanings of the device parameters like the drain current equations of the conventional BSIM3 model [42], and creating macromodels [43]. These approaches involve various modeling strategies, but an industry standard model that can be used for device simulation, production test and diagnosis has not been established. Considering the device characteristics such as quasi-saturation effect and RESURF effect, we have developed a new circuit model for HV-LDMOS as shown in Figure 22.

Figure 22. Circuit Model for HV-LDMOS [39]



It consists of an n-MOS connected in cascode with a parasitic NPN-BJT. The parasitic NPN-BJT represents the substrate, and a diode represents the depletion layer extension effect of the body with the drain terminal (PN junction) under reverse bias condition [39]. The parasitic NPN-BJT makes the MOS saturate at high gate voltages, thereby exhibiting the quasi-saturation effect. This model is used for device simulation during production testing of high-voltage devices. Figure 23 shows the I-V curves comparison between the circuit model and numerical simulation for HV-LDMOS.

Figure 23. I-V Characteristics Comparison between Circuit Model and Numerical Solution [39]

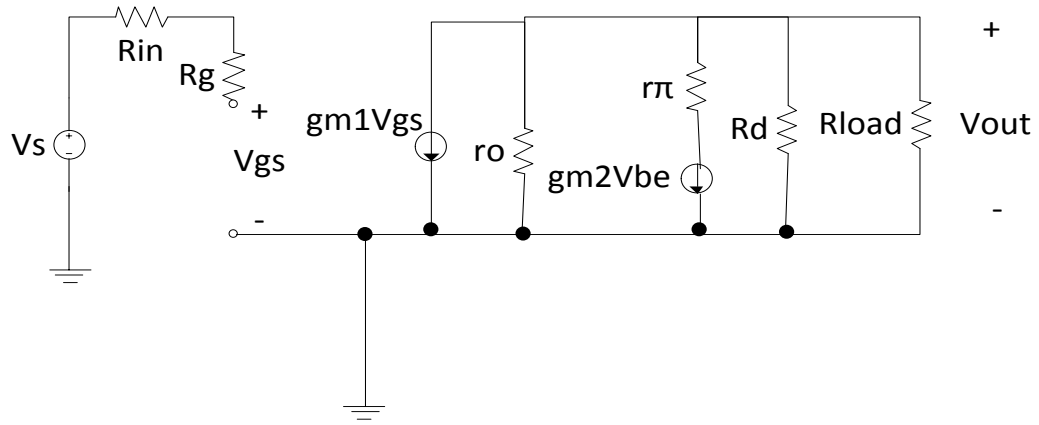


The bulk or body effect turns the diode ON, which triggers on the parasitic NPN-BJT. The circuit model requires more test resources, and determining the I-V characteristics through voltage sweep increases the test cost and time, which is a major disadvantage. The circuit model holds good for device simulation; however it is not suitable to use this model for production testing and diagnosis because of the inherent difficulty in inducing structural defects to develop fault models. We have developed the hybrid MOS-π model by integrating the small-signal model of the n-MOS with the hybrid-pi model of the parasitic NPN-BJT. Since the hybrid model consists of basic parasitic elements structural defects, can be easily induced to replicate its physical effects, and its transfer function can be computed to be used as a block in test simulation.

3.4.2. HYBRID MOS-π MODEL FOR HV-LDMOS

The n-MOS is represented by its small-signal model with infinite impedance between the gate and source terminals. The drain-to-source path is modeled by a current source representing the device transconductance. It also has an output resistance and the resistance of the lightly doped n-drift region at the drain terminal. Finally a load is connected to the drain terminal. The parasitic NPN-BJT is connected in cascode with the n-MOS. This is modeled by using the hybrid-pi model of the transistor with a current source representing its device transconductance and a resistance representing the junction contact. The model is as shown in the Figure 24.

Figure 24. Hybrid MOS-π based Equivalent Circuit Model for HV-LDMOSs [44]



The model shown in Figure 24 can be simplified into a transfer function by treating it in the common-source mode and obtaining its gain as follows:

$$A_V = \frac{-R_G\left(g_{m1}+g_{m2}\right)\left(r_0 \parallel r_\pi \parallel R_d \parallel R_{load}\right)}{R_{source}+R_G}. \qquad \text{Eq(11)}$$

This transfer function can be used as a block for production testing and diagnosis. To perform diagnosis, we induced structural defects into the hybrid MOS-π model.

3.4.3. Simulation Results of Hybrid MOS-PI Model for HV-LDMOS

A series of HV-LDMOSs with varying geometries were tested in the common-source mode, and the gain was computed using the transfer functions presented in Section 3.4.2. This was validated by simulation using the circuit model in the common-source mode. The results are presented in Table 5 for HV-LDMOS using the hybrid MOS-π model.

Table 5. Gain – HV-LDMOS Using Hybrid MOS-π Model

Id(V_{gs}, V_{ds})	**Gain (Av)**		
	HV-LDMOS Dimensions	**Hybrid MOS-π Model**	**Circuit Model**
2.5mA(10V, 200V)	L=20µm, W=20µm	-1.76	-1.81
2.8mA(20V, 200V)	L=20µm, W=20µm	-1.87	-1.98
3mA(5V, 200V)	L=1.8µm, W=20µm	-3.28	-3.25
3.5mA(10V,200V)	L=1.8µm, W=20µm	-3.65	-3.68
5mA(20V,200V)	L=1.8µm, W=20µm	-4.39	-4.48

From Table 5 we see that the gain calculated using the hybrid MOS-π model is in very good agreement with that of the simulated gain using the circuit model. These results show us that the hybrid MOS-π model is an accurate representation of the HV-LDMOS and their transfer

function can be used as a block to represent the device during production testing and diagnosis of high-voltage devices.

3.5 TEST CHALLENGES IN LDMOS

In order to test HV-LDMOS it is very important to investigate the test challenges associated with these high-voltage devices. The fault models for structural defects in HV-LDMOS should address these test challenges. Generally, a special test suite consisting of more than 50 parametric test measurements using CMOS process control monitoring is performed on LDMOS devices. The first test challenge is that the LDMOS device must be tested at high voltage and sometimes using high current, which primarily includes breakdown and leakage tests. These tests require voltage well beyond the range of parametric test systems and also sometimes they need to be tested up to 1 A [38]. Breakdown tests are not just a simple matter of testing a two-terminal dielectric structure. The off-state channel-breakdown and leakage must also be characterized, and to perform this gate must be in a controlled state. Hence, breakdown tests involve the use of source-measure unit at the gate, and a high voltage source-measure unit connected to the drain. The most likely failure mode during this test is shorts between the drain and gate in the FOX layer. This failure mechanism consists of hot carrier generating interface states (traps) and trapped electron charge, which results in negative charge building up at the Si/insulator interface. The location of this charge is likely to be in the vicinity of impact ionization intersection with the Si-SiO_2 interface. This negative charge attracts holes depleting the charge in the LDMOS n-drift region and increases the dc-on resistance of the device. Furthermore, the device transconductance shows a positive shift.

The second test challenge is the gate-stress test due to thermal overload. LDMOS transistors have low reliability due to inherent parasitic NPN transistor, resulting in snapback breakdown at high voltages [45]. The snapback breakdown is caused by a high drain voltage, which inherently provides base current to the parasitic bipolar transistor. In the presence of high base current, the bipolar transistor turns on hard, to cause latch up, and makes the device fail. At this point, the device would have reached its maximum thermal state. Hence to test for this defect we have to measure the thermal resistance.

The third test challenge in LDMOS transistors is the drain-leakage test due to high voltages. This is done at high voltages to ensure that the transistor has a low leakage current. During voltage overloads the transistor undergoes undesired stress resulting in higher leakage current. Traditionally the drain leakage test consists of three steps [46, 47]. First, the LDMOS is turned off by forcing the gate to ground through the driver or the gate clamping. Then, a HV pulse is applied to the pad that is connected to the drain of the transistor under test. Finally, the leakage current flowing into the test pad is measured by the ATE. This leakage current is a characteristic of the reverse breakdown that occurs during high voltage overloads. To overcome aforementioned test challenges and to automatically diagnose defects in high-voltage devices it is necessary to develop fault models.

3.6. STRUCTURAL DEFECTS IN HV-LDMOS

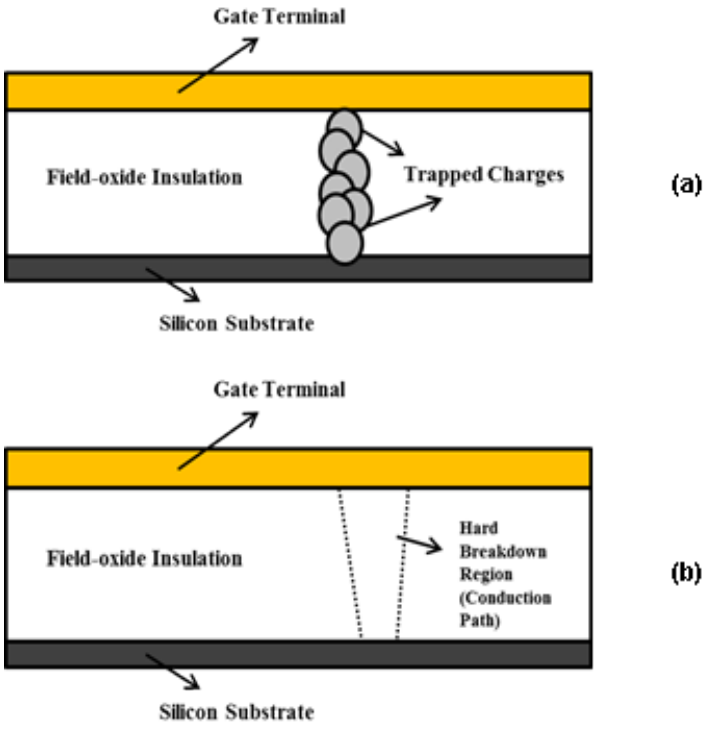
Structural defects arise mainly due to process-variations. Using the statistical data obtained from production floor testing the most commonly found structural defects are gate-FOX short (soft and hard breakdown), post-breakdown gate-stress (thermal-overload), and drain-

leakage (band-to-band tunneling of electrons) [44, 47]. We have developed fault models for these structural defects by inducing its physical behavior through parasitic elements in the hybrid MOS-pi model of HV-LDMOS.

3.6.1 GATE-FOX BREAKDOWN DEFECT

HV-LDMOS has a thick FOX layer which allows it to reach very high breakdown voltage levels. However, structural defects may occur in the FOX layer due to process-variations leading to two different breakdown mechanisms, soft and hard breakdown [48, 49]. Soft breakdown is shown in Figure 25(a). It occurs due to hot carrier injections where trapped charges accumulate and start to overlap in the FOX layer. This forms a conduction path which shorts the gate terminal to the bulk or body of the LDMOS. Hard breakdown is shown in Figure 25(b). It is more severe wherein there is excessive accumulation of trapped charges, and the silicon in the breakdown spot melts releasing oxygen. Hard breakdown results in the formation of a silicon filament through the FOX layer, which acts as a conduction path or short between the gate terminal and body of the LDMOS. Both soft and hard breakdown results in shorting the gate terminal with the body of the LDMOS [50], and increases the device-ON resistance drastically. To model a gate-FOX breakdown structural defect accurately we have to compute both the breakdown position and breakdown intensity. The breakdown position varies along the gate-channel and can occur at three different regions such as the source extension region, gate-channel region and drain extension region.

Figure 25. Gate-FOX Breakdown Defect (a) Soft Breakdown, (b) Hard Breakdown [44]



Since the breakdown occurs due to short of gate-FOX, the conduction path is modeled as a parasitic resistance from either gate to source or gate to drain. This resistance depends on the doping concentration of the corresponding layer. Now using the traditional breakdown test approach the drain and source terminals are shorted to ground, to measure the post-breakdown resistance by applying a positive gate voltage (V_g), and measure the gate current (I_g) as shown in Figure 26. The post breakdown resistance acts as an inverted bath-tub curve shown in Figure 27.

Figure 26. Breakdown Resistance as Conduction Path

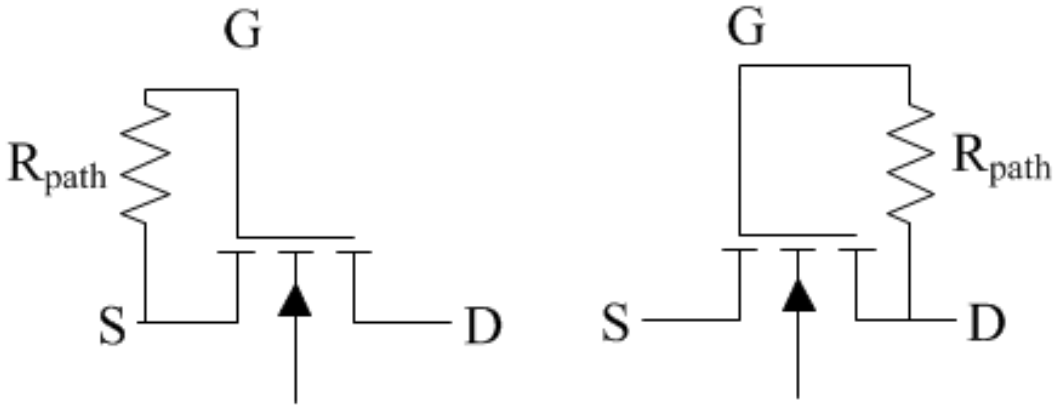
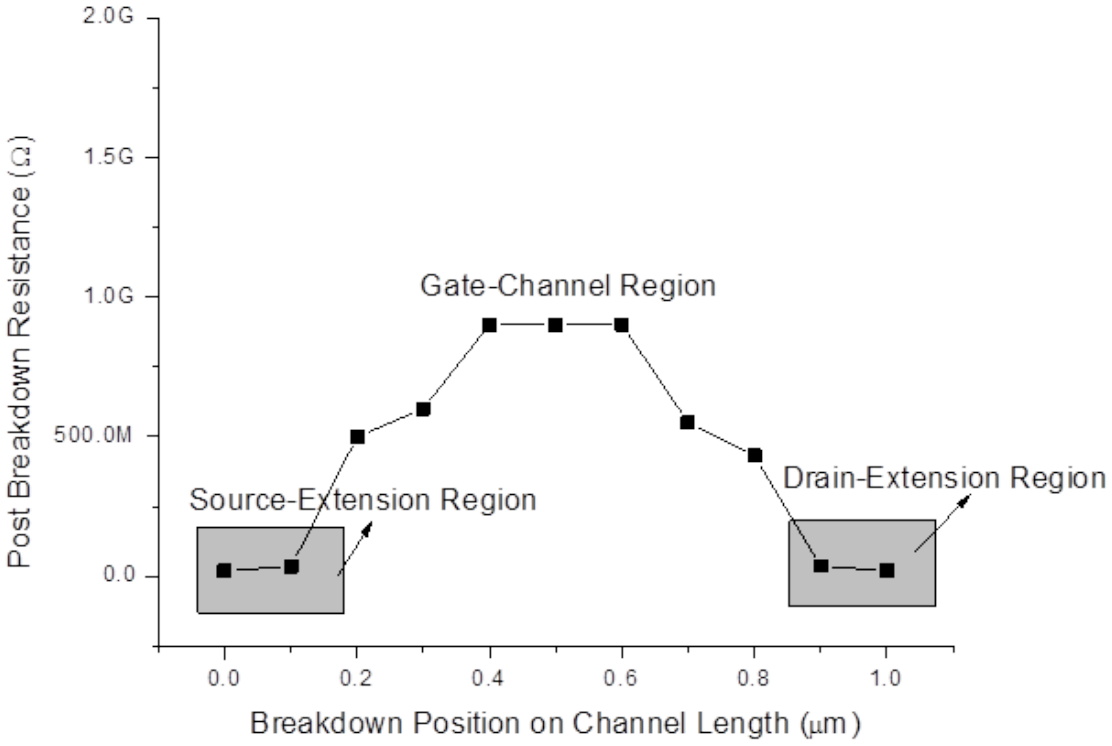
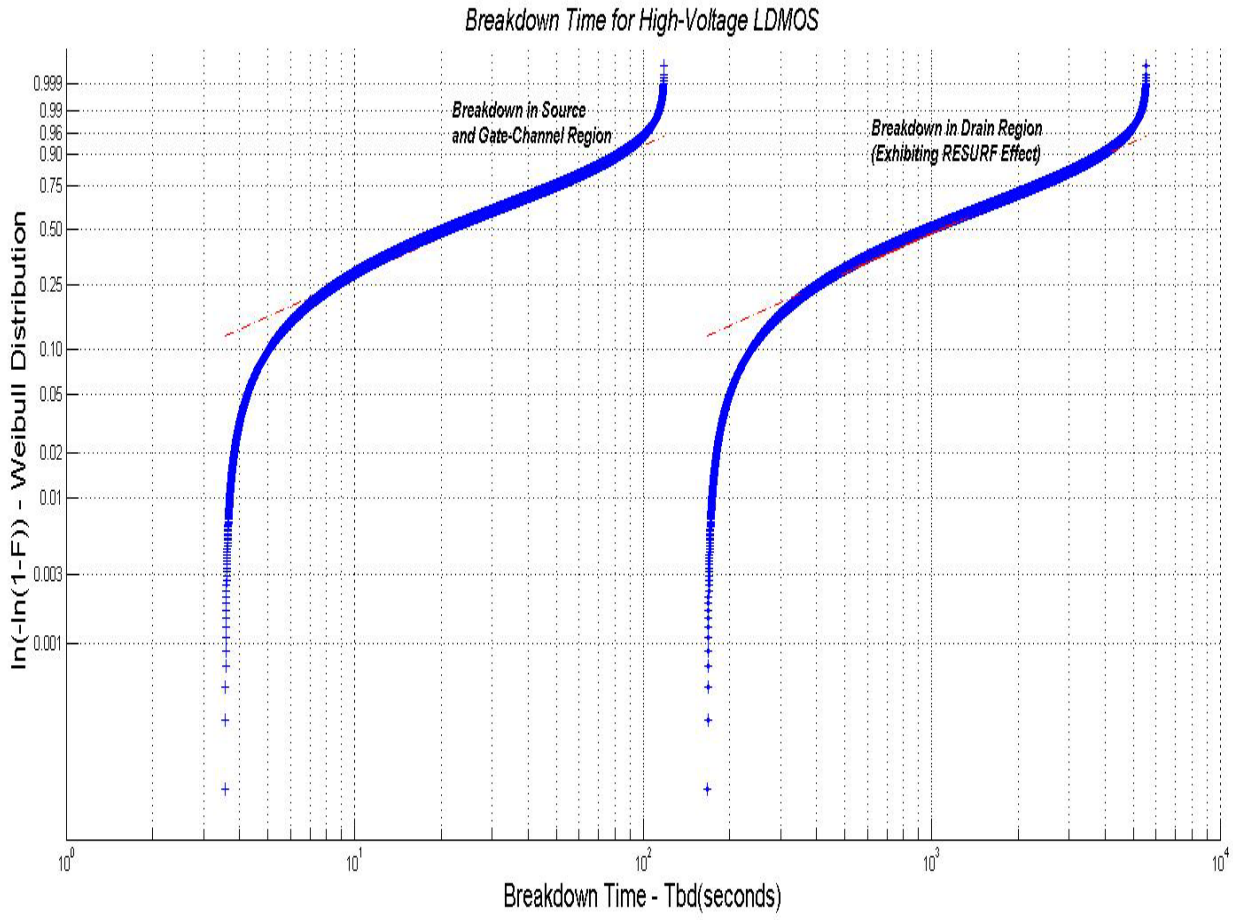


Figure 27. Post-Breakdown Resistance Curve for HV-LDMOS across the Channel Length [44]



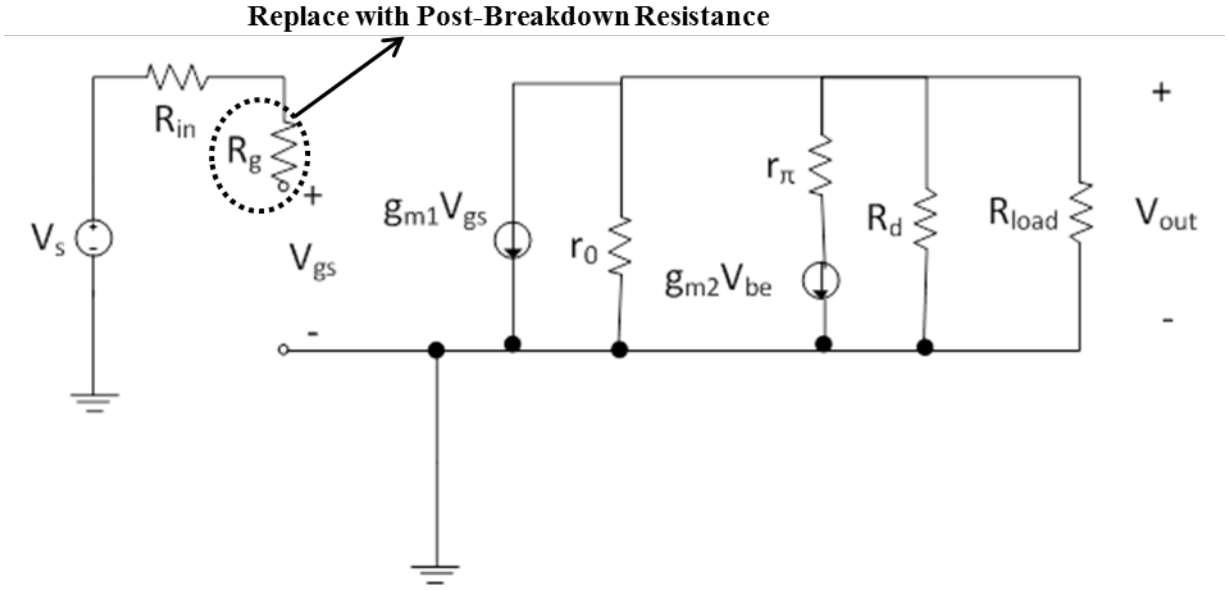
The breakdown time is also an interesting characteristic that is observed in HV-LDMOS where two breakdown curves are observed due to the RESURF effect as shown in Figure 28.

Figure 28. Gate-FOX Breakdown Defect (a) Post Breakdown Resistance, (b) Breakdown Time [44]



The fault model for gate-FOX breakdown is shown in Figure 29 with a post breakdown resistance replacing the gate resistance in the hybrid MOS-π model for HV-LDMOS.

Figure 29. Gate-FOX Breakdown Fault Model [44]



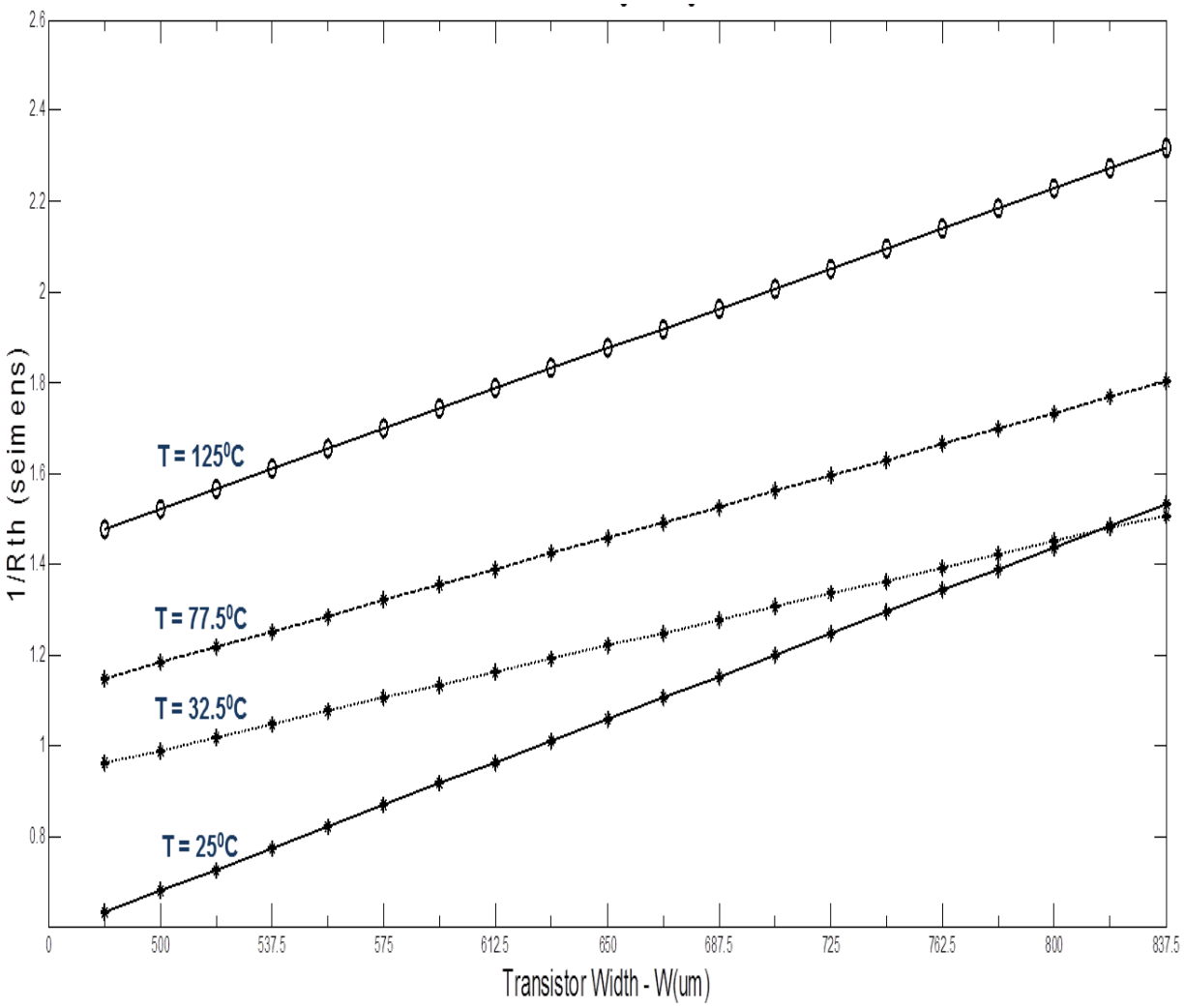
The new gain for HV-LDMOS with gate-FOX breakdown structural defect is as follows:

$$A_V = \frac{-R_{BD}\left(g_{m1}+g_{m2}\right)\left(r_0 \parallel r_\pi \parallel R_d \parallel R_{load}\right)}{R_{source}+R_{BD}} \qquad \text{Eq(12)}$$

3.6.2 Post-Breakdown (Thermal) Gate-Stress Defect

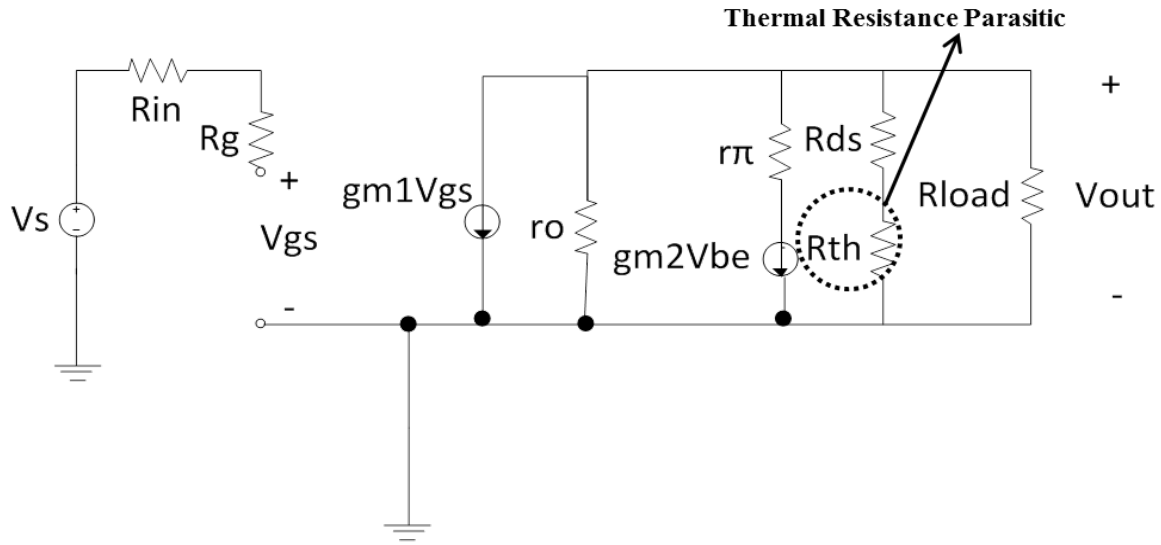
After gate-FOX breakdown occurs it subjects the HV-LDMOS to thermal stress at the gate terminal. This is termed as a self-heating effect, where the drain current decreases because the mobility of charge carriers decreases with increase in temperature [51, 52]. This structural defect gives rise to a parasitic thermal resistance as shown in Figure 30. The thermal resistance decreases with increase in transistor width due to the availability of more charge carriers, which negates the self-heating effect.

Figure 30. Post-Breakdown Thermal Resistance [44]



The fault model for post-breakdown thermal stress is shown in Figure 31 with a post-breakdown thermal resistance between the drain and source in series with the drain resistance in the hybrid MOS-π model for HV-LDMOS.

Figure 31. Post-Breakdown Thermal Stress Fault Model [44]



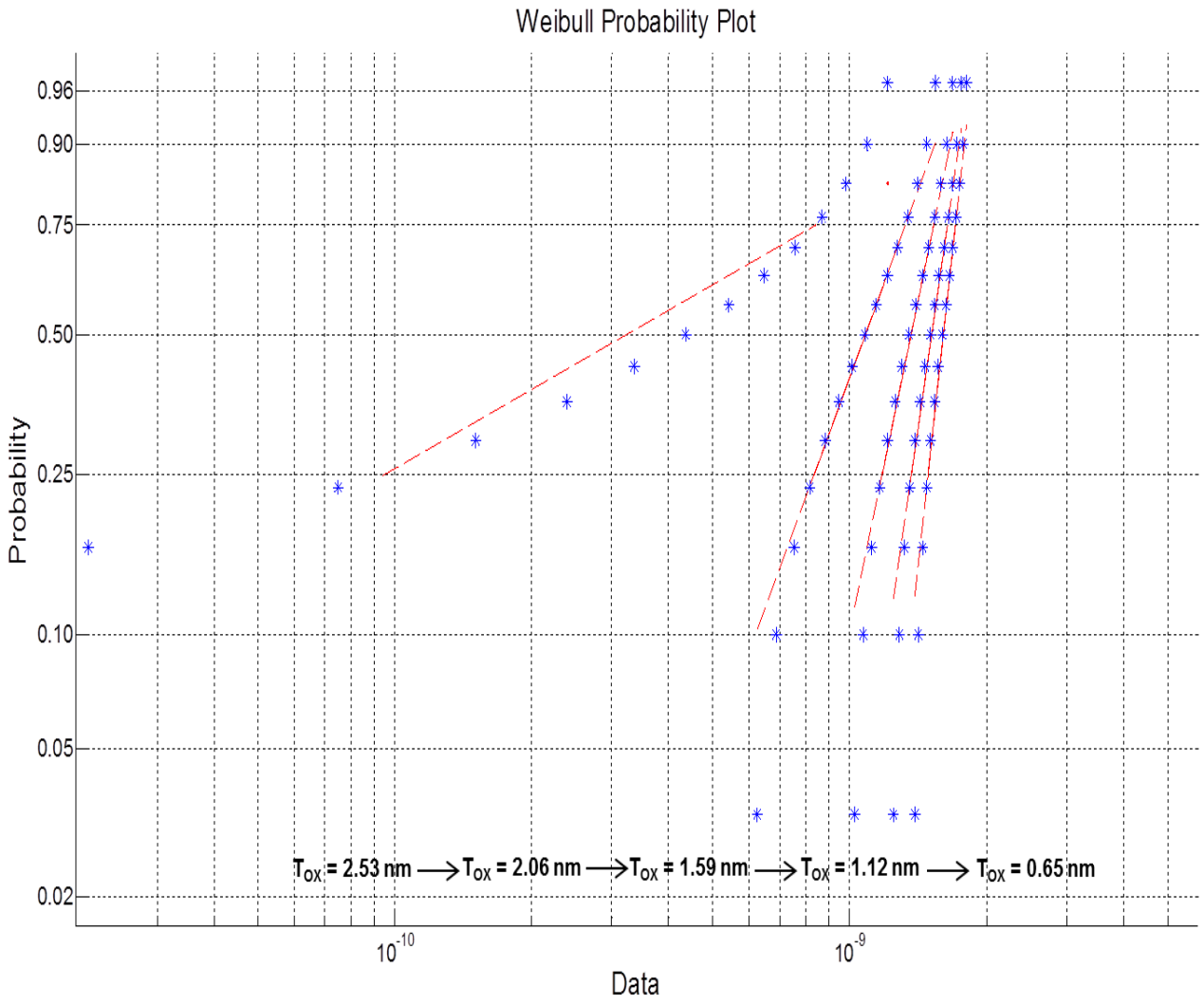
The new gain for HV-LDMOS with post-breakdown gate-stress defect is as follows:

$$A_V = \frac{-R_{BD}\left(g_{m1}+g_{m2}\right)\left(r_0 \parallel r_\pi \parallel R_d + R_{th} \parallel R_{load}\right)}{R_{source}+R_{BD}} \qquad \text{Eq(13)}$$

3.6.3 DRAIN-LEAKAGE DEFECT

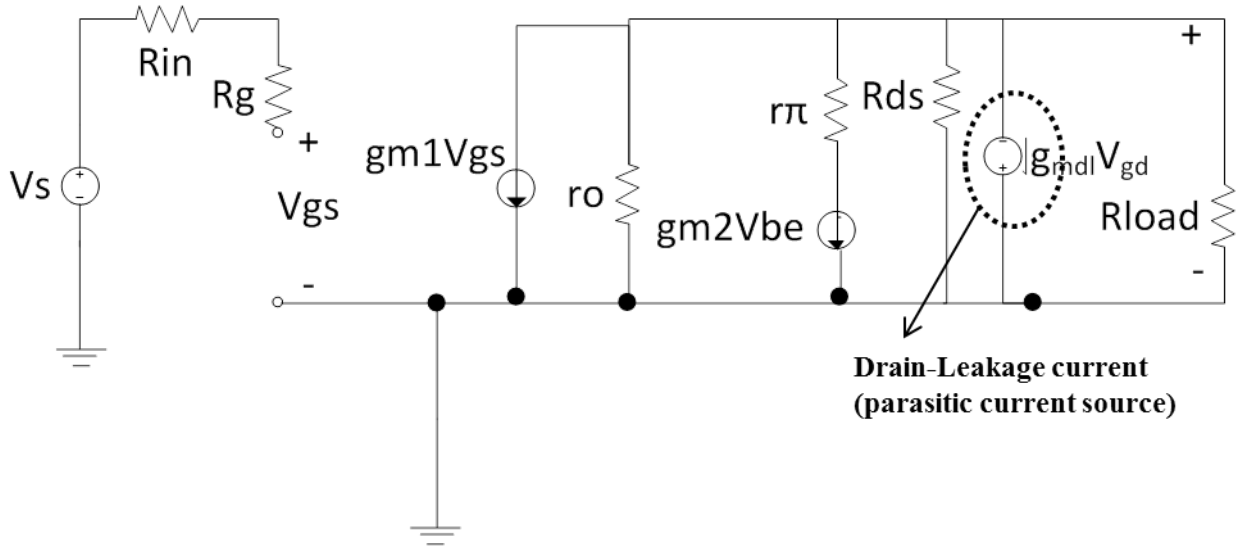
Band-to-band tunneling in silicon at the drain terminal of the HV-LDMOS results in drain-leakage structural defect. The drain leakage current is much higher even when the drain voltage (V_d) is lower than breakdown voltage level. The drain leakage current for different FOX thickness is shown in Figure 32.

Figure 32. Drain-Leakage Current for Different FOX dimensions [44]



This occurs due to poor gate-FOX insulation and can be prevented by varying the thickness of gate-FOX along the channel-length with a bulky FOX layer at the drain extension region. The fault model for drain-leakage defect due to high voltage stress is shown in Figure 33 with, a current source representing the leakage current between the drain and source in the hybrid MOS-π model for HV-LDMOS.

Figure 33. Drain-Leakage Fault Model [44]



The new gain for HV-LDMOS with drain-leakage structural defect is as follows:

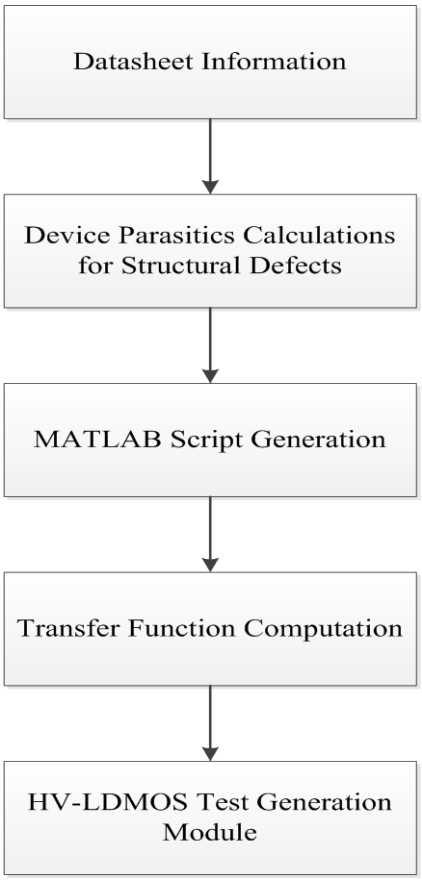
$$A_V = \frac{-R_{BD}\left(g_{m1}+g_{m2}+g_{mdl}\right)\cdot\left(r_0 \parallel r_\pi \parallel R_d \parallel R_{load}\right)}{R_{source}+R_{BD}} \qquad \text{Eq(14)}$$

Using equations (11)-(14) we can automatically generate electrical and fault models for HV-LDMOS test simulations using the algorithm presented in Section 3.7.

3.7. HV-LDMOS MODEL LIBRARY

This module generates electrical and fault models for HV-LDMOS using the device datasheet information and the transfer function equations presented in Section 3.6. The electrical and fault models are automatically generated using MATLAB scripts and their transfer functions are computed in MATLAB as shown in Figure 34.

Figure 34. Process of Generating HV-LDMOS Transfer Functions

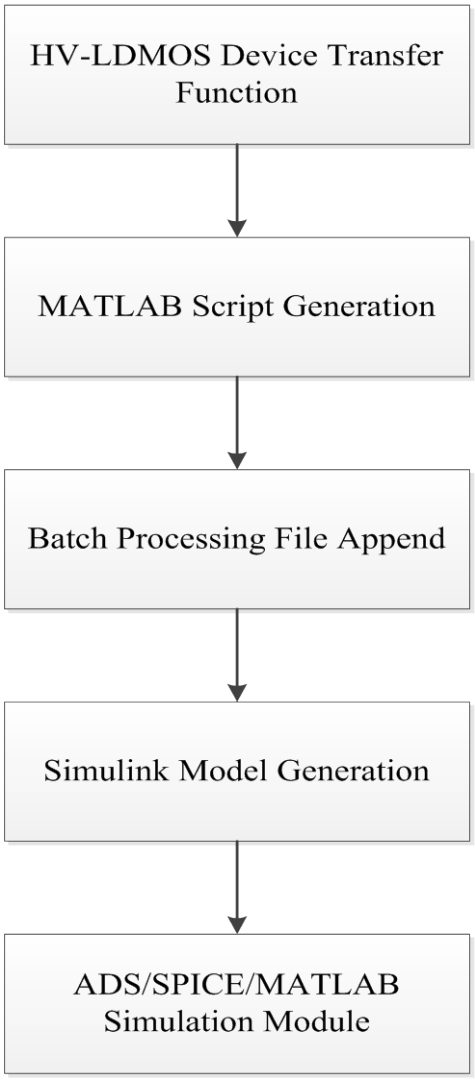


These transfer functions are used as blocks to generate Simulink models which incorporate the noise-reduction scheme to perform high-voltage device testing.

3.8. HV-LDMOS Test Generation Module

This module prepares MATLAB scripts for generating Simulink models for both fault-free and fault induced cases in HV-LDMOS. The Simulink models are simulated in a batch process thereby reducing the test simulation time. The Simulink models are generated as shown in Figure 35.

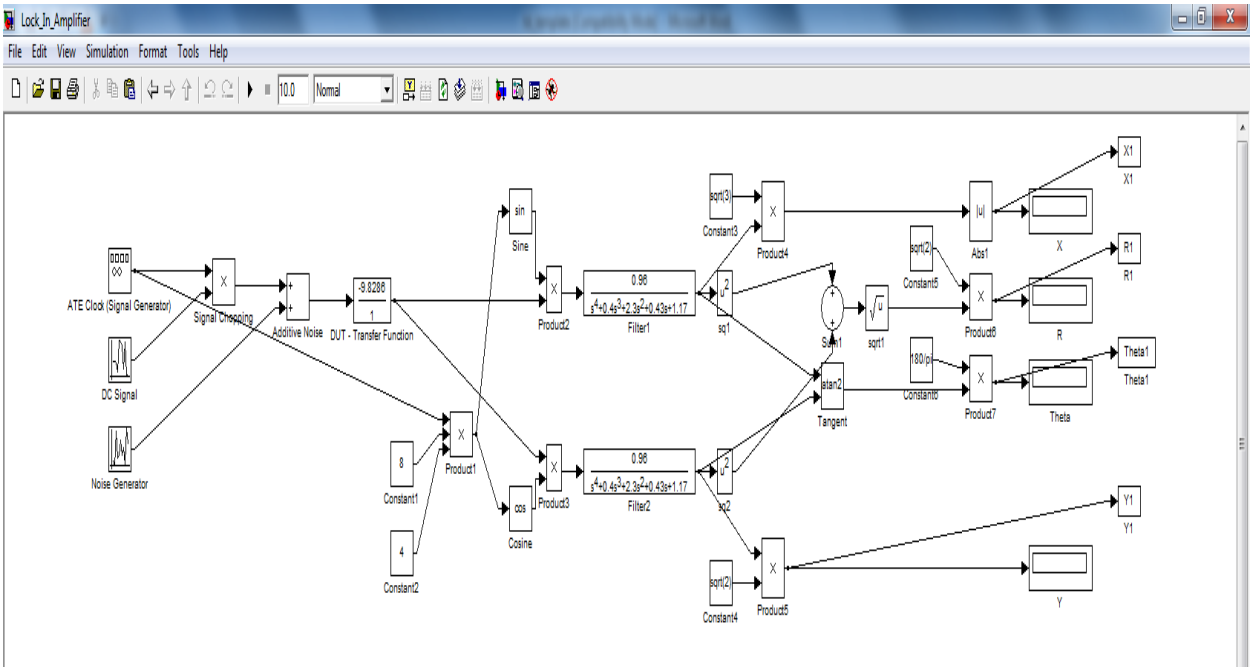
Figure 35. Process of Generating Simulink Models



The output of the HV-LDMOS model library gives a set of transfer functions for HV-LDMOS in fault free cases as well as faulty cases, such as soft-breakdown, hard-breakdown, thermal stress, and drain leakage. These transfer functions are used in the HV-LDMOS test generation module to generate MATLAB scripts. The MATLAB scripts are then internally

translated to Simulink models, and tested using the noise-reduction scheme. The Simulink models are as shown in Figure 36.

Figure 36. Simulink Models for Testing HV-LDMOS



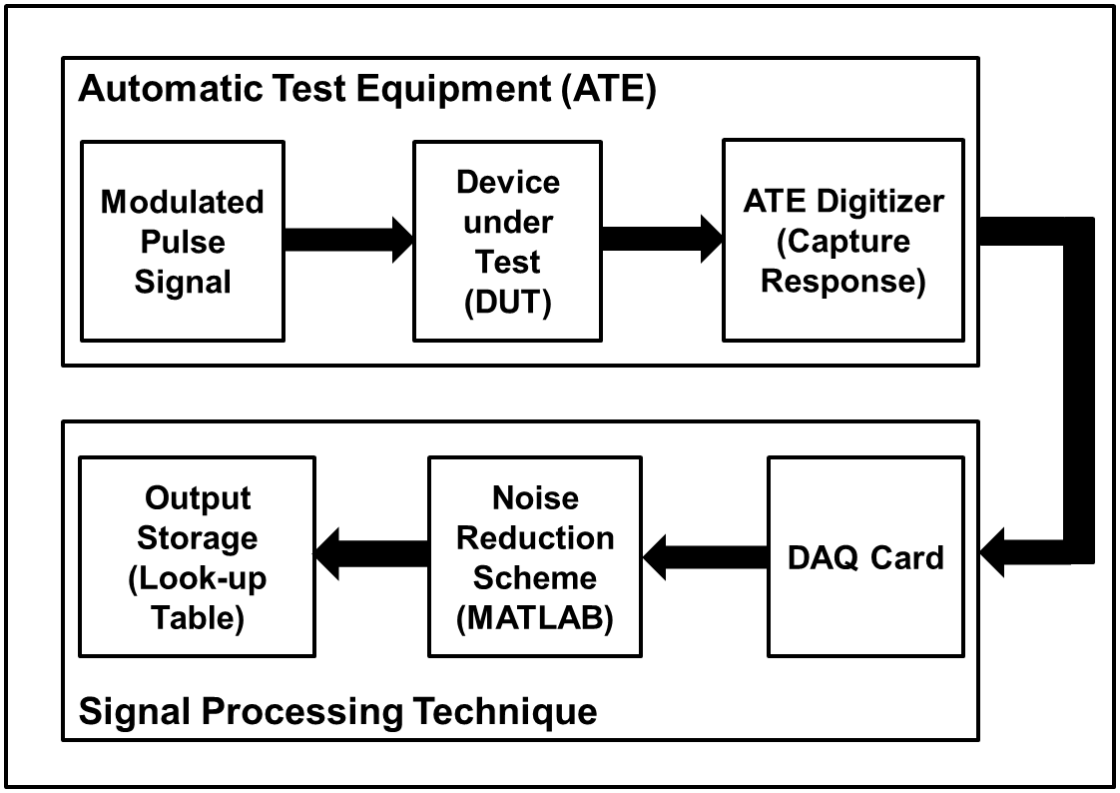
Breakdown and leakage tests are performed using the noise-reduction scheme presented in Chapter 4.

CHAPTER 4

LOW COST TEST TECHNIQUE FOR HIGH-VOLTAGE DEVICES

High voltage testing of LDMOS is cumbersome and a hazardous task. There are many intricate measurements to be made on the production floor. Breakdown and leakage tests are the two conventional test measurements on LDMOS devices. During breakdown tests, the drain and source terminals are grounded and the gate has to be in a controlled state to make the necessary test measurements. During leakage tests, making extremely low magnitude measurements typically of the order of sub-nano amperes is very challenging due to the presence of power supply and ATE noise (~60 Hz). Sub-nano current amplifiers are generally used to make leakage test measurements; however, this additional test circuitry increases the test costs. Coupled with the large charging and discharging time of the ATE and power supply noise, it is very difficult to make accurate test measurements in the range of sub-nano amperes [53, 54]. Our proposed test technique uses a new signal processing technique to differentiate between system noise and actual test measurements. We modulate a DC source with ATE clock signal (~1 KHz) to produce relatively high pulse signal to power supply noise for extracting the required DC response. The DUT digitized response is captured by the ATE. The test setup is shown in Figure 37.

Figure 37. HV-LDMOS Test Setup



Signal processing of the captured response is performed using a noise-reduction scheme with a homodyne receiver and demodulating the response to retrieve the DC value of the test measurement with modulated pulse.

The noise-reduction scheme is capable of extracting signals from an extremely noisy environment typically when the signal-to-noise ratio (SNR) is as low as -60 dB. Essentially the noise-reduction scheme consists of a homodyne receiver with a bandpass filter resulting in a very narrow bandwidth (~10 Hz) which can be used to extract the DC components of the test measurement. This test methodology involves modulation-demodulation (mixing) to extract the DC components from the frequency and phase of the test measurement.

4.1. TEST TECHNIQUE PRINCIPLE

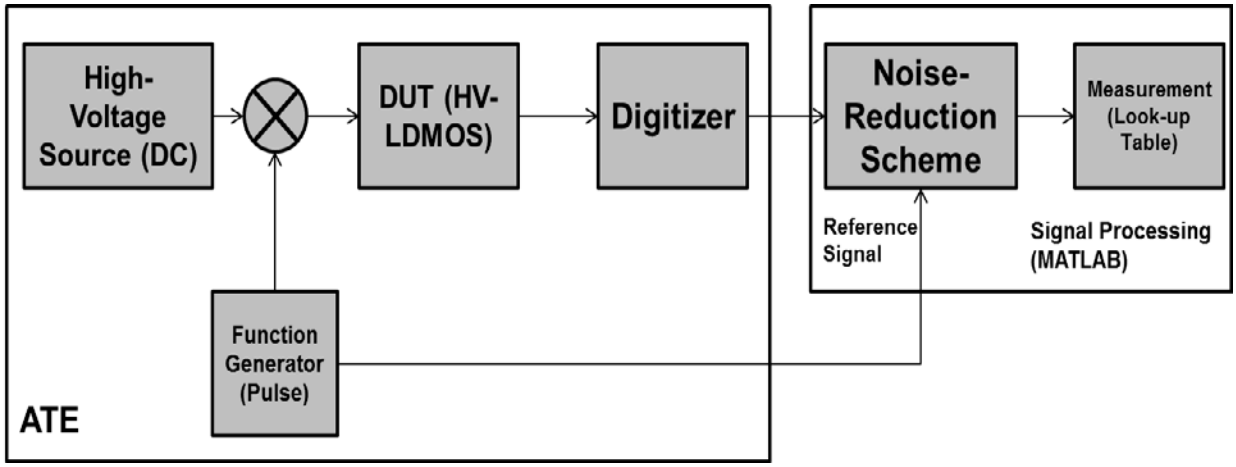
In principle a homodyne receiver is used to extract signals from a noisy environment where it detects signals based on modulation at some known frequency. Power supply noise is at 60 Hz and much of the tester system noise is associated with DC and low frequency. The homodyne receiver measures within a narrow spectral range thus helping in reducing the noise bandwidth. In our proposed test technique we modulate the DC test stimulus with a reference internal ATE clock signal (pulse) at a relatively higher frequency of 1 KHz when compared to power supply and tester system noise. This step is referred to as the modulation part or "chopping" and is represented by the following mathematical expression;

$$V_{in} = V_s \cos(\omega t + \phi) \qquad \text{Eq(15)}$$

where V_s represents the magnitude and $\omega t + \varphi$ represents the frequency and phase component of the test stimulus.

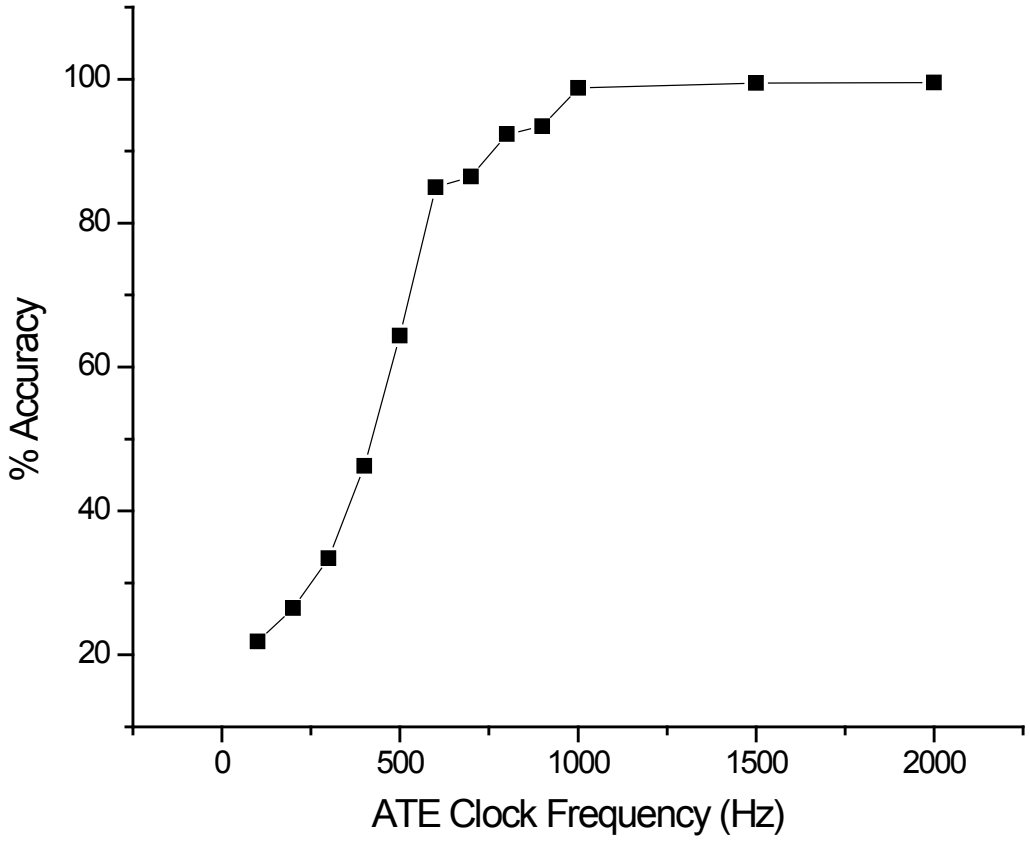
Using the same internal ATE clock signal as reference we filtered out the DC component of the test measurement with respect to the frequency component which is referred to as the demodulation part. Since noise is at a different frequency it will be filtered out providing a highly accurate test measurement without the presence of any additional complex test hardware. The test setup of the proposed test technique is shown in Figure 38.

Figure 38. Hardware Test Setup of Proposed Test Technique



From Figure 38, we can infer that the DC signal is obtained from a high-voltage source which is modulated using the ATE clock pulse. The modulated pulse signal is provided as test stimulus to the DUT. The DUT response is captured using the ATE digitizer and signal processing is performed in MATLAB. In signal processing the same ATE clock pulse is used as the reference signal, to perform demodulation and retrieve the test measurement. The extraction of test measurements implicitly depends on frequency of the ATE clock pulse. This was analyzed by using different ATE clock pulse frequencies, and retrieving the DC value by signal processing as shown in Figure 39.

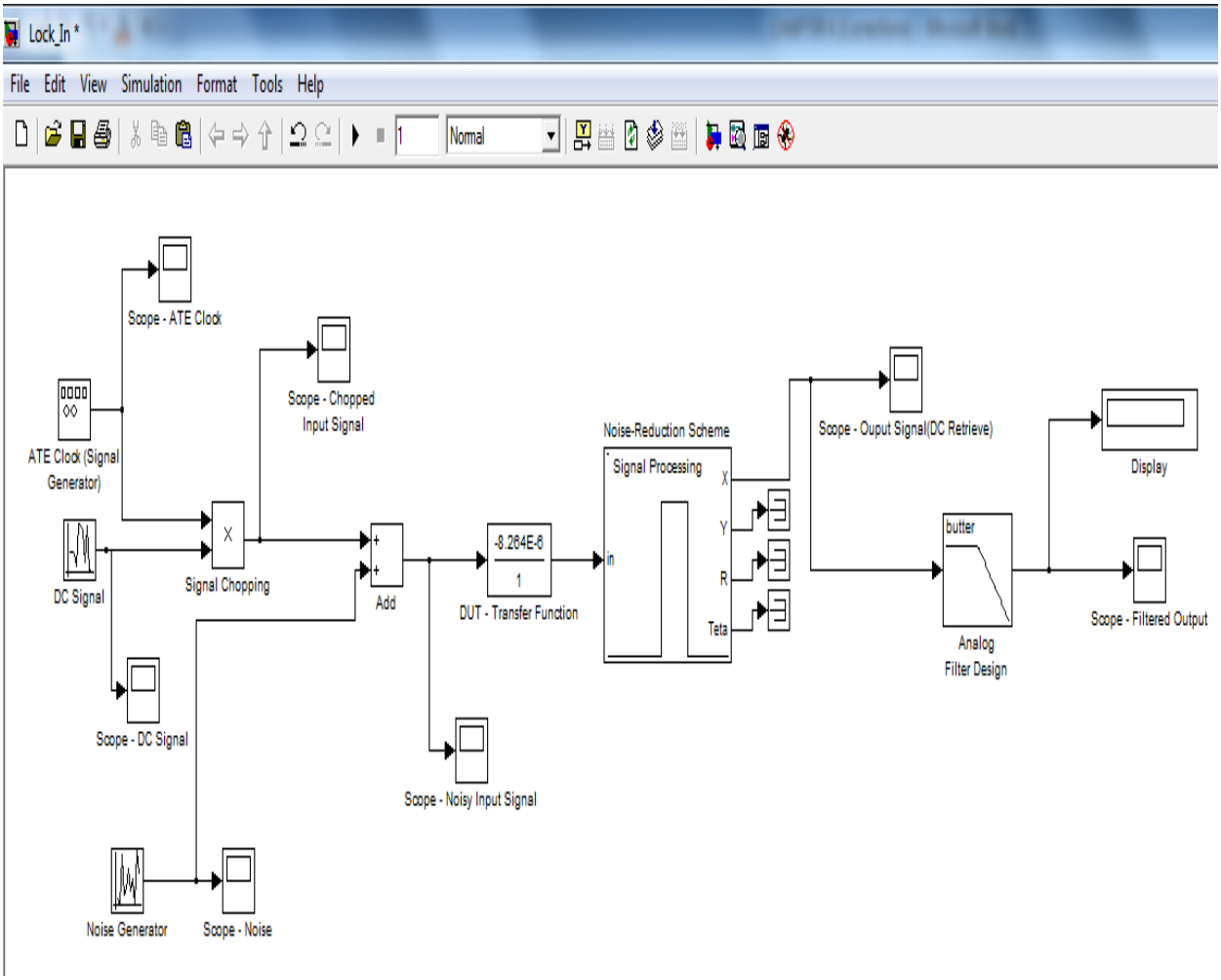
Figure 39. ATE Clock Frequency vs. Signal Extraction Accuracy



A 5 V DC signal was modulated with an ATE clock pulse of varying frequencies with amplitude of 0.6 V noise signal was added for modulating two signals. This noisy modulated pulse signal was processed using the homodyne receiver (very narrow band receiver) and DC value was extracted. Below frequencies of 1K Hz, the accuracy of retrieving the test measurement ranged from 20 to 90%. When the ATE clock pulse frequency was increased to 1000 Hz, the accuracy improved dramatically and the accuracy stabilizes. For cost effectiveness of our new technique, we have decided to use a 1 KHz ATE clock pulse for all simulations and hardware measurements.

The test measurements are stored in a look-up table for diagnostic purposes. To perform diagnosis, we compared the results of test simulation with the actual hardware test measurements. We had previously discussed the equivalent electrical model for HV-LDMOS and fault models for structural defects in Chapter 3 of the dissertation. These models are used to perform test simulations in MATLAB-Simulink domain and the results are compared to actual device measurements to perform diagnosis for structural defects in HV-LDMOS. The test setup in MATLAB is shown in Figure 40.

Figure 40. Noise Reduction Scheme MATLAB-SIMULINK Domain Test Setup



This test technique is highly accurate, and the fault-model based test approach reduces the test suite for HV-LDMOS to a couple of test measurements. It also reduces the overall test cost and time.

4.2. Simulation Results Using Noise Reduction Scheme

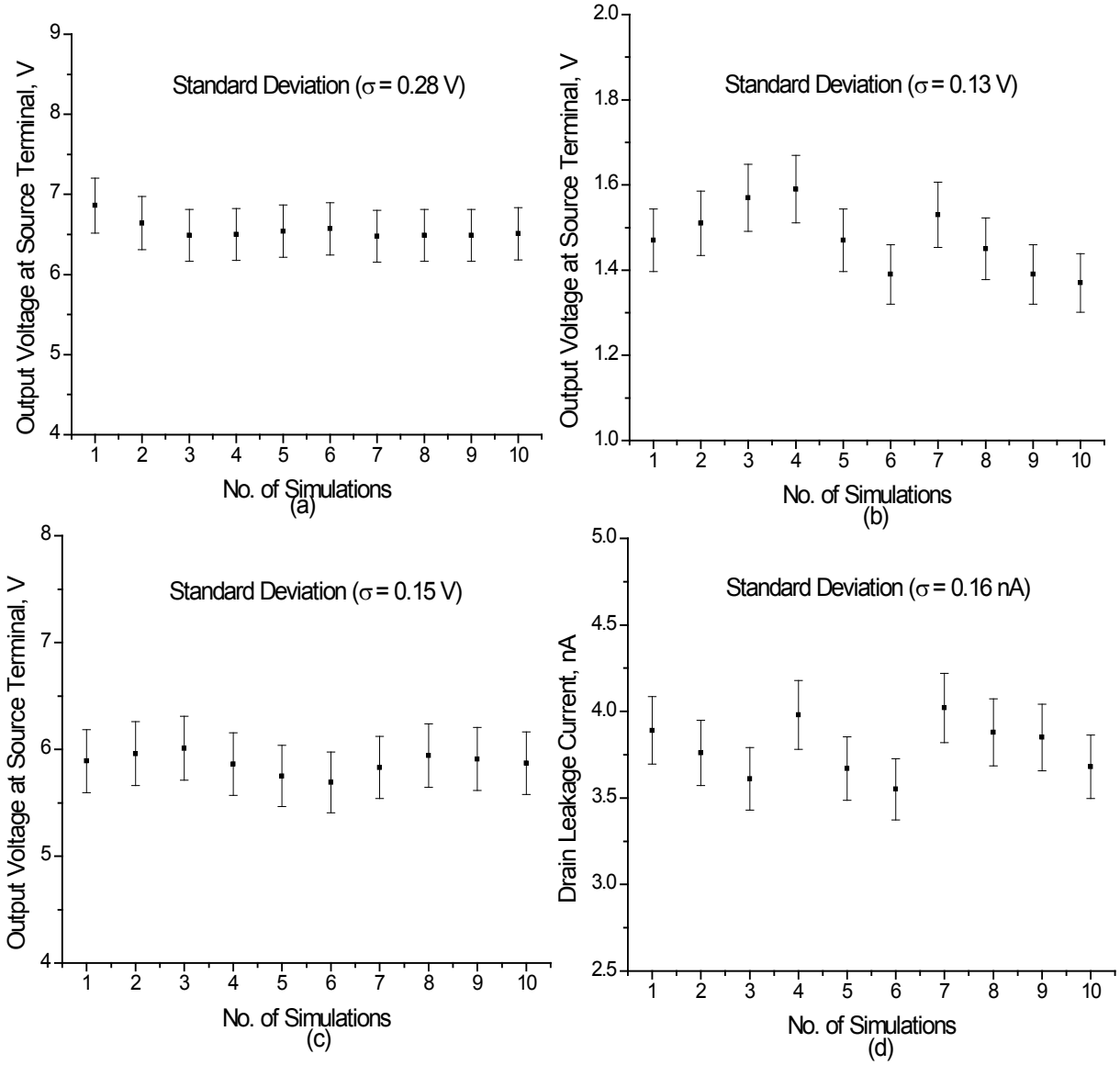
A test simulation was performed for a 700V MOSFET driver with 2 short-channel HV-LDMOSs. The fault models were developed by inducing different structural defects in the HV-LDMOS and output test measurements are computed for both fault-free and fault induced cases using the noise-reduction scheme. The proposed noise-reduction scheme simulations results are shown in Table 6.

Table 6. Noise Reduction Scheme Simulation Results

Test Condition	**DUT Specifications** $\{I_d(V_{gs}, V_{ds})\}$	**Noise Reduction Scheme**
Fault Free	1 mA (10 V, 700 V)	6.68 V
Soft-Breakdown Test	0 mA (17 V, 0 V)	2.76 V
Hard-Breakdown Test	0 mA (20 V, 0 V)	0.79 V
Thermal Stress (R_{th} = 12 Ω @ 120 ^{0}C)	1 mA (10 V, 700 V)	6.19 V
Drain Leakage Test (I_{dl})	1 mA (0 V, 700 V)	6.83 nA

To verify the accuracy of the noise-reduction scheme, 10 repetitive test simulations were run on the MOSFET driver with HV-LDMOS, and the standard deviation for each test was computed. The simulation results are shown in Figure 41.

Figure 41. Noise Reduction Scheme Simulation Results (a) Fault-Free, (b) FOX Breakdown, (c) Thermal-Stress, (d) Drain-Leakage



The test simulation results show that the proposed test technique based on the noise-reduction scheme can identify structural defects by performing breakdown and leakage measurements. We also calibrated to ensure that the test measurements were accurate.

4.3. PSEUDOCODE GENERATION

After test simulations were performed on the 700V MOSFET driver HVPro automatically generates, pseudocodes (generic test instructions), and stores the simulation results in a look-up table. The pseudocode is shown in Figure 42.

Figure 42. Pseudocode for HV-LDMOS Testing

```
*** EVEREST-DUT IN SOCKET (SITE 4) ***

**** FAULT-FREE TEST ON EVEREST-DUT ****
GATE_STIMULUS (forcing pin = P104_F7, sensing pin = P104_E7)
WAKE_INPUT (driving pin = P111_J9, must be grounded pin = A4)
HV_STIMULUS (forcing pin = P104_F6, sensing pin = P104_E6)
DC_CHOPPING (gate stimulus = 1, forcing pin = 2, sensing pin = 3)
LIA_MEASUREMENT (forcing pin = P104_H9, sensing pin = P104_G9)
COMPARE_LIMITS (lower limit = 1.103925 V, upper limit = 1.839875 V, nominal value = 1.4719 V)

**** SOFT-BREAKDOWN TEST ON EVEREST-DUT ****
GATE_STIMULUS (forcing pin = P104_F7, sensing pin = P104_E7)
WAKE_INPUT (driving pin = P111_J9, must be grounded pin = A4)
HV_STIMULUS (forcing pin = A4, sensing pin = A4)
DC_CHOPPING (gate stimulus = 1, forcing pin = 2, sensing pin = 3)
LIA_MEASUREMENT (forcing pin = P104_H9, sensing pin = P104_G9)
COMPARE_LIMITS (lower limit = 0.4477575 V, upper limit = 0.7462625 V, nominal value = 0.59701 V)

**** HARD-BREAKDOWN TEST ON EVEREST-DUT ****
GATE_STIMULUS (forcing pin = P104_F7, sensing pin = P104_E7)
WAKE_INPUT (driving pin = P111_J9, must be grounded pin = A4)
HV_STIMULUS (forcing pin = A4, sensing pin = A4)
DC_CHOPPING (gate stimulus = 1, forcing pin = 2, sensing pin = 3)
LIA_MEASUREMENT (forcing pin = P104_H9, sensing pin = P104_G9)
COMPARE_LIMITS (lower limit = 0.0516345 V, upper limit = 0.0860575 V, nominal value = 0.068846 V)

**** THERMAL-STRESS TEST ON EVEREST-DUT ****
GATE_STIMULUS (forcing pin = P104_F2, sensing pin = P104_E7)
WAKE_INPUT (driving pin = P111_J9, must be grounded pin = A4)
HV_STIMULUS (forcing pin = P104_F6, sensing pin = P104_E6)
DC_CHOPPING (gate stimulus = 1, forcing pin = 2, sensing pin = 3)
LIA_MEASUREMENT (forcing pin = P104_H9, sensing pin = P104_G9)
COMPARE_LIMITS (lower limit = 0.6895275 V, upper limit = 1.1492125 V, nominal value = 0.91937 V)

**** DRAIN-LEAKAGE TEST ON EVEREST-DUT ****
GATE_STIMULUS (forcing pin = A4, sensing pin = A4)
WAKE_INPUT (driving pin = P111_J9, must be grounded pin = A4)
HV_STIMULUS (forcing pin = P104_F6, sensing pin = P104_E6)
DC_CHOPPING (gate stimulus = 1, forcing pin = 2, sensing pin = 3)
LIA_MEASUREMENT (forcing pin = P104_H9, sensing pin = P104_G9)
COMPARE_LIMITS (lower limit = 9.3045e-010 A, upper limit = 1.55075e-009 A, nominal value = 1.2406e-009 A)
```

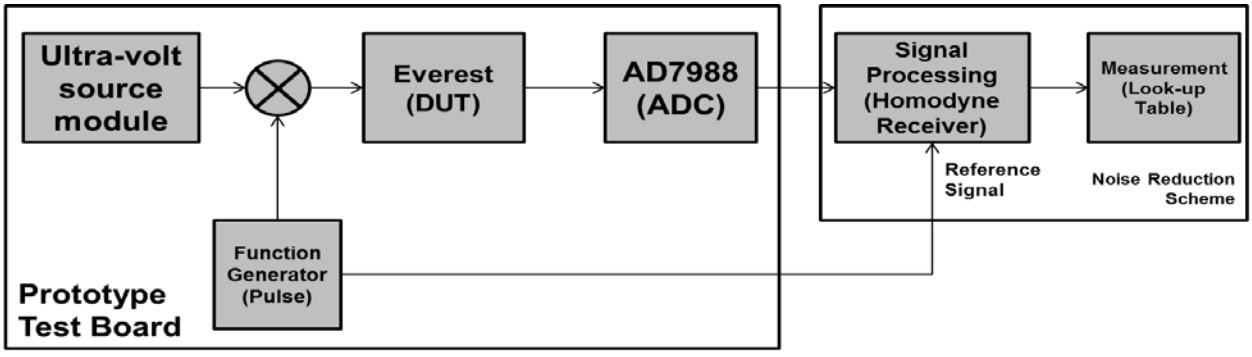
This pseudocode is used to automatically perform testing on the ATE. The hardware measurement results from the ATE are then compared with the simulation results stored in the look-up table, to identify structural defects in HV-LDMOS.

CHAPTER 5

EXPERIMENTAL VALIDATION

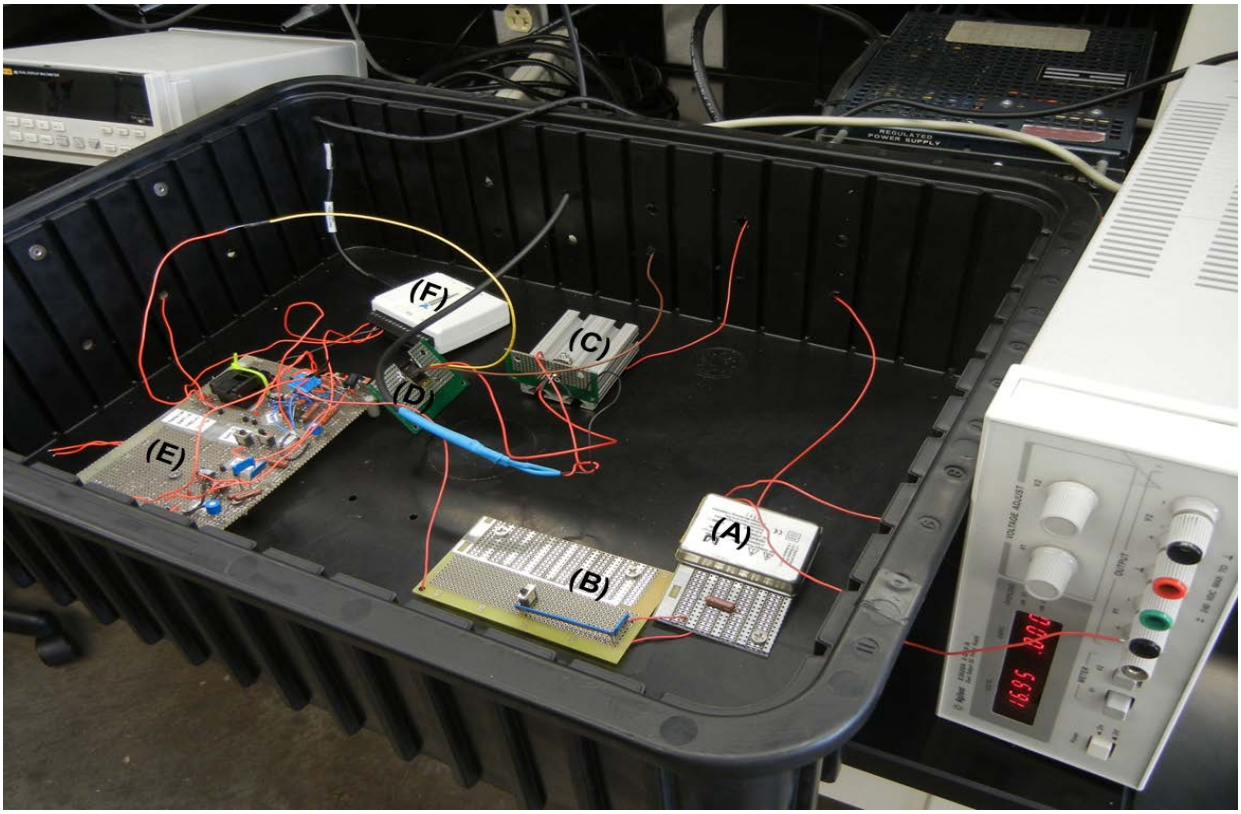
To validate the proposed test technique using the noise reduction scheme, we built a prototype test setup as shown in Figure 43. We have used a MOSFET driver with a 700V LDMOS as DUT to perform the test measurements. An UltraVolt source module was used to provide the high voltage DC signal. A function generator was used to provide the ATE clock pulse (~1 KHz), which also serves as the reference signal during signal processing. Modulation was performed using a 1 KV power MOSFET and the modulated pulse signal (test stimulus) was provided to the DUT. The response of the DUT was captured using a 12-bit analog-to-digital converter (ADC) and the digitized signal was acquired using a DAQ card. The acquired test response was processed using a homodyne receiver with a bandpass filter, and the DC component of the test measurement was retrieved after demodulation and subsequent filtering.

Figure 43. Block Diagram of Hardware Prototype Test Setup



The prototype test setup is as shown in Figure 44.

Figure 44. Prototype Test Setup: (A) Ultravolt 1KV Source Module, (B) Voltage Divider, (C) Power MOSFET, (D) DUT, (E) 12 Bit Analog-Digital Converter, (F) DAQ Card



5.1. Test Measurements using Noise-Reduction Scheme

Breakdown, thermal stress and drain leakage tests were performed on the MOSFET driver with a 700V LDMOS using the noise-reduction scheme. These results were then compared with the test simulation results to validate the electrical model and fault models developed in Chapter 3. The comparison of test simulation vs. hardware measurement is shown in Table 7.

Table 7. Comparison of Test Simulation vs. Hardware Measurements

Test Condition	**DUT Input Specifications {$I_d(V_{gs}, V_{ds})$}**	**Noise Reduction Scheme (Simulation)**	**Noise Reduction Scheme (Measurement)**
Fault-free	1 mA (12 V, 700 V)	6.89 V	6.92 V
Soft-breakdown	0 mA (17.7 V, 0 V)	2.78 V	3.07 V
Hard-breakdown	0 mA (19.5 V, 0 V)	0.89 V	0.70 V
Thermal Stress (R_{th} = 12 Ω @ 120 ^{0}C)	1 mA (10 V, 700 V)	6.19 V	6.38 V
Drain Leakage Test (I_{dl})	1 mA (0 V, 700 V)	6.83 nA	6.69 nA

From Table 7, we can infer that the test measurements are in very good correlation with simulation results, thereby validating the electrical and fault models discussed in Chapter 3. The following sections compare the noise-reduction scheme with conventional test methods. This comparison shows the advantages in terms of signal-to noise ratio that can be achieved using the noise-reduction scheme.

5.2. BREAKDOWN TEST

Conventional breakdown test is performed by grounding the drain and source terminals, applying gate voltage, and measure the output at the source. A fault-free device would give a zero output voltage. However, if a device has a gate-FOX breakdown, then there is a conduction path through the FOX insulation layer resulting in a higher output voltage. Due to the low magnitude of these measurements, they are generally subdued by power supply and ATE noise, which affects the accuracy of the test measurements. Four 700V devices (test vehicles) were

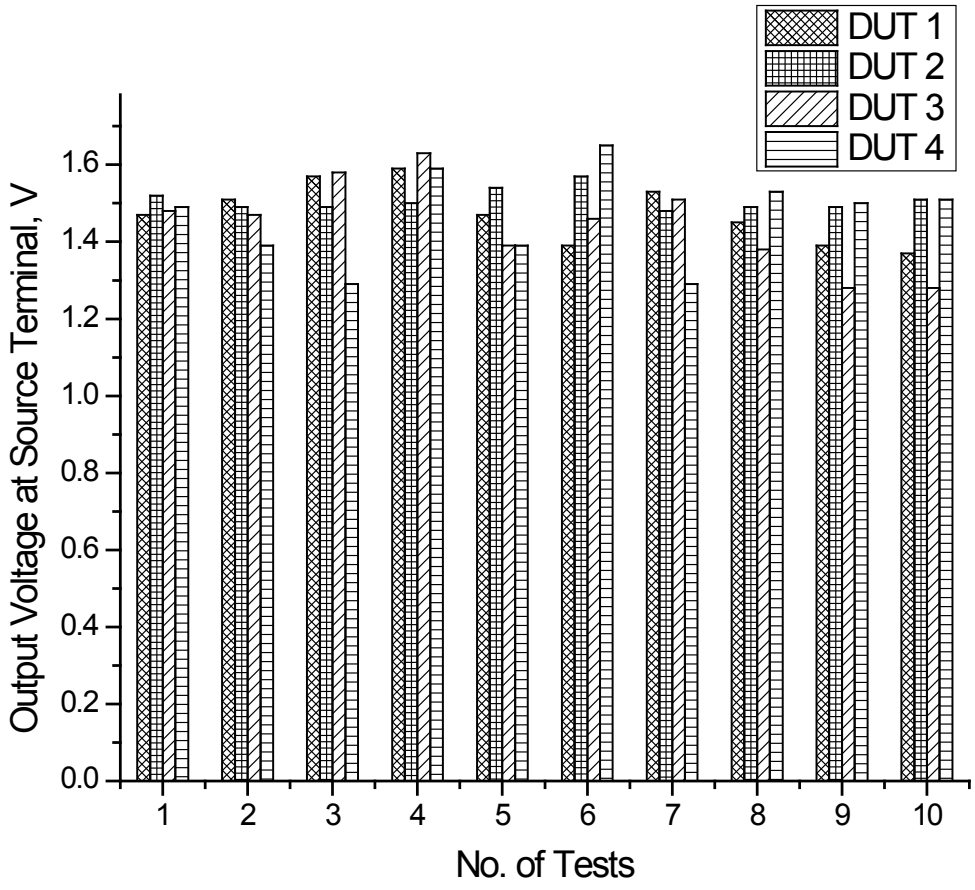
prepared by inducing breakdown in the FOX insulation layer, and were tested using both the noise-reduction scheme and conventional test method as shown in Table 8.

Table 8. Breakdown Test Measurement Results

Device Tested	**Conventional Test Method**	**Noise-Reduction Scheme**
DUT 1	0.84 V	1.47 V
DUT 2	1.36 V	1.52 V
DUT 3	1.48 V	1.48 V
DUT 4	0.93 V	1.49 V

From Table 8 we can infer that the noise-reduction scheme provides a higher signal-to-noise ratio and can make accurate test measurements when compared with conventional test methods. The accuracy of test measurements made using the noise-reduction scheme was obtained by making 10 repetitive test measurements on each test vehicle, and computing the standard deviation as shown in Figure 45.

Figure 45. Output Voltage at Source Terminal of Gate-FOX Breakdown Test



The standard deviation is very low for breakdown test using the noise-reduction scheme, and is 0.08 V for DUT 1, 0.03 V for DUT 2, 0.12 V for DUT 3 and 0.12 V for DUT 4. This shows that the noise-reduction scheme provides accurate breakdown test measurements in a highly noisy test environment.

5.3. POST-BREAKDOWN THERMAL STRESS TEST

The test vehicles with gate-FOX breakdown are used to perform post-breakdown thermal stress test. After gate-FOX breakdown occurs in the device, the dc on-resistance of the DUT

increases due to the parasitic thermal resistance. This causes attenuation of output voltage across the source, when the gate bias voltage (15 V) and high-voltage (700V) at the drain are provided. Four 700V devices (test vehicles) after gate-FOX breakdown are used to perform testing using both the noise-reduction scheme and conventional test method as shown in Table 9.

Table 9. Post-Breakdown Thermal Stress Test Measurement Results

Device Tested	**Conventional Test Method**	**Noise Reduction Scheme**
DUT 1	6.63 V	6.54 V
DUT 2	6.74 V	6.65 V
DUT 3	6.59 V	6.41 V
DUT 4	6.67 V	6.61 V

Since the magnitudes of these measurements are high they are not affected by power supply noise or ATE noise. From Table 9 we can infer that both the noise-reduction scheme and conventional test method provide similar test measurements.

5.4. LEAKAGE CURRENT TEST

Conventional leakage test is performed by using the following two steps. The first step is removing the DUT thereby, creating an open circuit and measuring the current (i_1) at the high-voltage rail. The second step is to place the DUT and measure the current (i_2) at the high-voltage rail. The difference between these two currents $(i_1 - i_2)$ would be the leakage current into the DUT. The leakage currents are of extremely low magnitude of the order of nano amperes (nA) for a fault-free device. In order to measure this low magnitude leakage current in a highly noisy test environment some additional circuitry, such as sub-nano amplifiers have been incorporated.

The noise-reduction scheme is capable of measuring extremely low magnitude currents in a highly noisy test environment using a modulated test stimulus, and demodulation of DUT response with a homodyne receiver. This enabled us to achieve accurate test measurements without using additional test circuitry. Two sets of three 700V devices (test vehicles) were prepared by inducing leakage into the device by applying negative voltages of -2.5 V and -0.85 V to the gate terminal. These devices were then tested to measure the leakage current using both the conventional test method and the noise reduction scheme is shown in Table 10.

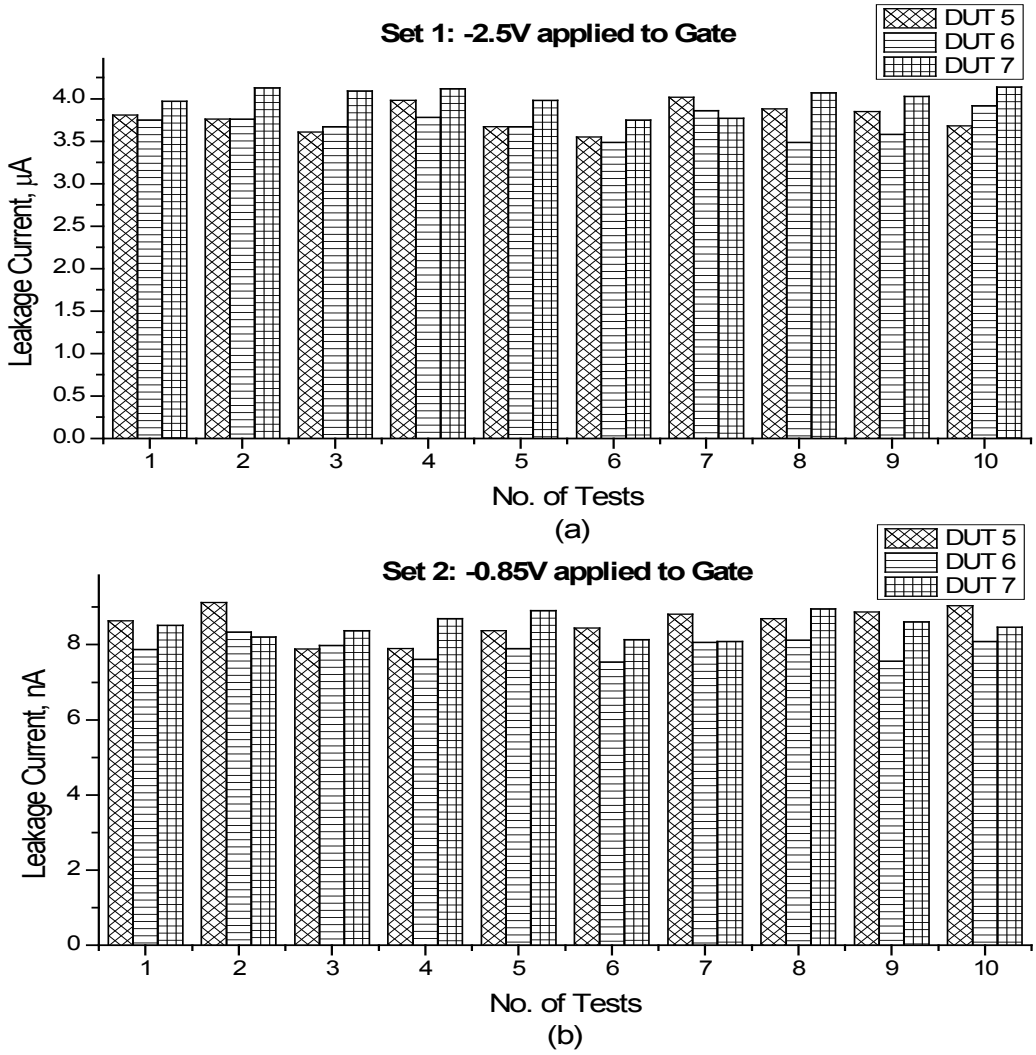
Table 10. Leakage Current Test Measurement Results

Device Tested	**Conventional Test Method**	**Noise Reduction Scheme**
Set 1 (-2.5 V applied to gate for inducing leakage)		
DUT 5	3.62 µA	3.89 µA
DUT 6	3.52 µA	3.75 µA
DUT 7	3.84 µA	3.97 µA
Set 2 (-0.85 V applied to gate for inducing leakage)		
DUT 8	0 µA	8.64 nA
DUT 9	0 µA	7.87 nA
DUT 10	0 µA	8.52 nA

From Table 10 we can infer that for set 1 when the leakage current in the DUT is higher both the noise-reduction scheme based test technique and conventional test method show similar results. However, for set 2, when the leakage current in the DUT is extremely low in the order of nA, the conventional test method gives a zero output while the noise reduction scheme accurately measures the leakage current. The accuracy of test measurements made using the

noise-reduction scheme was obtained by making 10 repetitive test measurements on each test vehicle, and computing the standard deviation as shown in Figure 46.

Figure 46. Drain Leakage Current of Leakage Test (a) -2.5V applied to Gate, (b) -0.85V applied to Gate



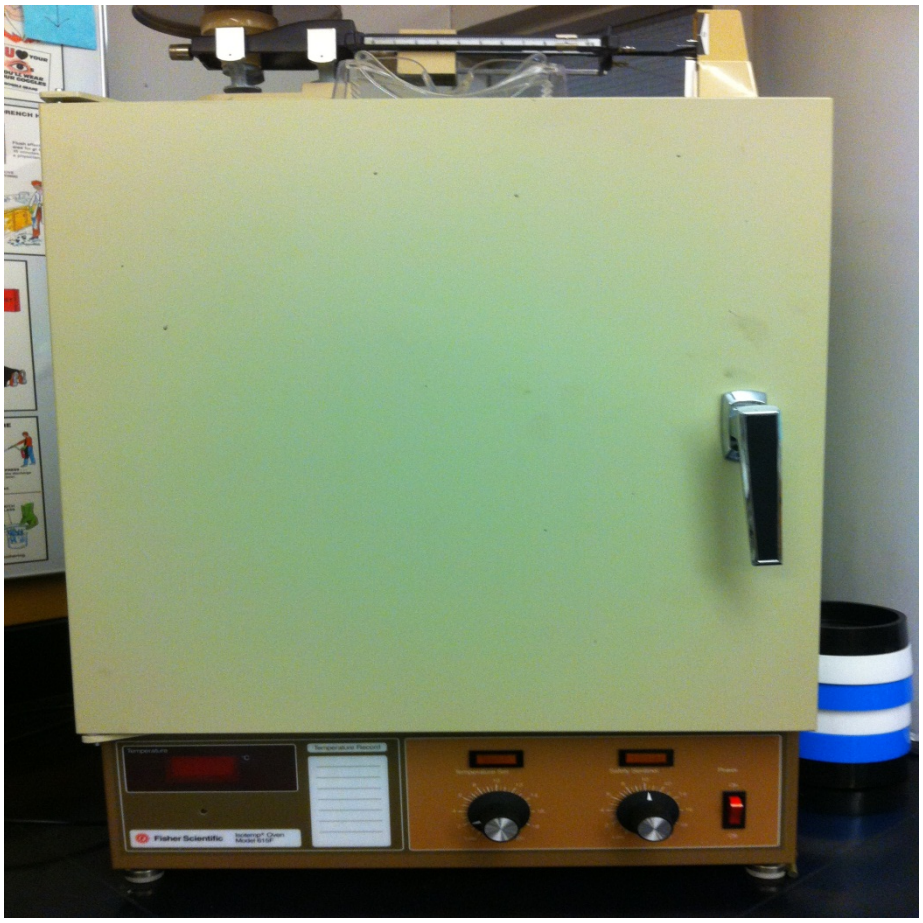
The standard deviation is very low for leakage test using the noise-reduction scheme, and is 0.16 µA for DUT 5, 0.15 µA for DUT 6, 0.14 µA for DUT 7, 0.43 nA for DUT 8, 0.26 nA for DUT 9 and 0.30 nA for DUT 10. This shows that the noise-reduction scheme provides accurate

leakage test measurements in a highly noisy test environment. Using the fault models and the test setup developed, we are able to detect soft-breakdown, hard-breakdown, thermal stress, and drain leakage structural defects in HV-LDMOS.

5.5. POST-THERMAL CYCLING LEAKAGE TEST

During continuous operation HV-LDMOSs dissipate power, which has a thermal cycling effect on the transistor commonly known as "thermal fatigue" [55]. The thermal fatigue is caused by different thermal expansion coefficients between the silicon and insulator interface leading to mechanical stress. A varying degree of mechanical stress increases the gate-induced leakage current in the device, leading to device failure. Typically, HV-LDMOS used in automotive and motor drive applications have very stringent thermal fatigue requirements. For example, an automobile radio output stage may require the device to withstand a total of 5000 cycles of 55^0C case-temperature over a period of five years. Therefore, it is extremely important to test these devices by subjecting them to thermal cycling to ensure high reliability [55].

Figure 47. Thermal Cycling Setup



Thermal cycling was performed on the MOSFET driver with a 700V LDMOS device by subjecting it to temperatures ranging from 30^0C to 200^0C, and measuring the leakage current. A furnace was used to perform thermal cycling as shown in Figure 47. The temperature was varied from 30^0C to 200^0C with increasing step size, and a settling time of 30 minutes before each leakage current measurement was made. The noise-reduction technique was used to measure the leakage current as shown in Table 11.

Table 11. Post-Thermal Cycling Leakage Test Measurements

Temperature (^{0}C)	**Leakage Current**
30^{0}C	2.5 μA
50^{0}C	5.17 μA
75^{0}C	9.83 μA
100^{0}C	17.67 μA
150^{0}C	21.54 μA
200^{0}C	25.12 μA

As shown in Table 11, we can observe that the leakage current increases with rise in temperature due to thermal fatigue. The leakage current increases from 2.5 μA at room temperature to extremely high value of 25.12 μA at 200^{0}C. Such high leakage current will invariably lead to device failure. Thermal fatigue analysis is extremely critical when HV-LDMOS is used in high power dissipating environments. To mitigate this issue, the device design can be modified, and the materials with similar co-efficient of thermal expansion can be used for fabrication.

CHAPTER 6

DEVELOPMENT OF NEW TEST TECHNIQUE FOR LDMOS USING LOW-VOLTAGE

Testing high-voltage devices on the production floor creates unsafe work environment for personnel who perform testing. . Performing conventional breakdown and leakage tests on these devices requires the use of source modules, which can generate voltage signals from 600 V up to several kilo-volts. These source modules or high-voltage generation circuits increase the test cost, time to test an IC chip, and is a potential hazard to the test engineer handling the ATE. Alternate test techniques for testing high-voltage devices using non-conventional low-voltage stimulus, such as impulses and wavelets is currently being explored. However, researchers face an extremely difficult task of developing a test technique that can successfully excite the high-voltage device to its maximum limits using a low-voltage stimulus. HV-LDMOS is a non-linear device hence, any efforts to perform scaling from a test perspective would be futile.

Reliability testing is one of the key design requirements performed during semiconductor product development. Reliability testing involves performing tests and simulations on devices, by subjecting them ESD stress to predict the region of failure, and design protection circuits. This guarantees device performance for an extended period of time under harsh ESD conditions [56]. ESD simulations involve applying transmission line pulses to the gate of the transistor, and measuring the drain current by sweeping the drain voltage. We have incorporated the device

physics fundamentals and reliability test principles, to develop an alternate test technique that can test high-voltage devices using low-voltage stimulus. The physical behavior of HV-LDMOS has been previously presented in Chapter 3.

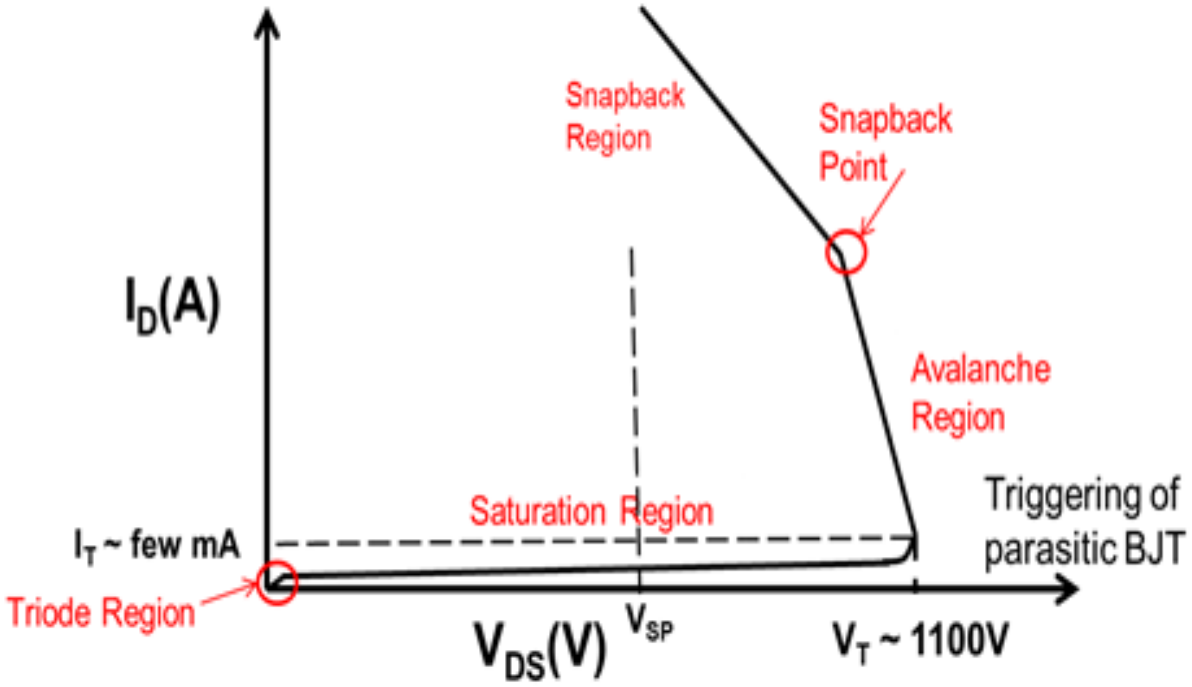
6.1. HV-LDMOS RELIABILITY TEST PRINCIPLES

Under ESD stress conditions, HV-LDMOS structures undergo avalanche and snapback breakdown, due to negative differential resistance [57]. Snapback breakdown of HV-LDMOS is due to the activation of the parasitic bipolar junction transistor, which is triggered ON by the voltage drop in the substrate due to the substrate current (I_{sub}) generation at high reverse bias. This substrate current is a function of the junction tunneling current (I_{tunnel}) and is given by,

$$I_{sub} = (M-1)I_{ch} + M\left(I_0 + I_{tunnel}\right) \quad \text{Eq(16)}$$

where, M is the impact ionization multiplication factor, I_0 is the reverse bias p-n junction leakage current, and I_{ch} is the channel current. However, it is extremely difficult to measure M experimentally as I_{tunnel} can neither be measured separately nor neglected. Hence, the multiplication factor, M is obtained by a combination of modeling and curve fitting parameters. To perform modeling under ESD conditions, the HV-LDMOS has to be subjected to a high electrostatic stress than when compared with regular operating conditions [58, 59, 60, and 61]. The different operating regions of HV-LDMOS under ESD condition is shown in Figure 48.

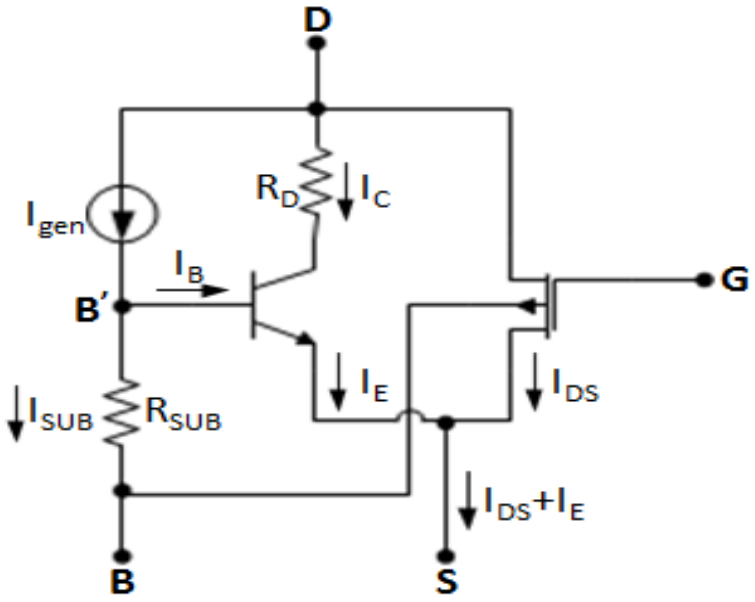
Figure 48. Generic I-V curve of HV-LDMOS under ESD Stress



Triode and saturation regions are governed by standard MOS equations. Avalanche breakdown occurs, when the drain voltage is much greater than the maximum drain voltage the device can accommodate. Finally, snapback occurs when the parasitic BJT turns on thereby, inducing Kirk effect and resulting in device failure or breakdown of the HV-LDMOS [58].

The parasitic BJT turns ON when the voltage drop in the substrate is greater than 0.7 V [62, 63]. The parasitic model of HV-LDMOS under ESD conditions is shown in Figure 49.

Figure 49. Parasitic HV-LDMOS Model under ESD Stress



The avalanche multiplication factor is a function of the impact ionization coefficient [64, 65] and the drain voltage applied, and is given by

$$M = \frac{1}{1 - C_1 \cdot \exp\left[-\frac{C_2}{\left(V_{DD} - V_{dsat}\right)}\right]} \qquad \text{Eq(17)}$$

where, C_1 and C_2 are curve fitting parameters and V_{dsat} is given by

$$V_{dsat} = \frac{V_G - V_{TH}}{a_1 + b_1\left(V_G - V_{TH}\right)} \qquad \text{Eq(18)}$$

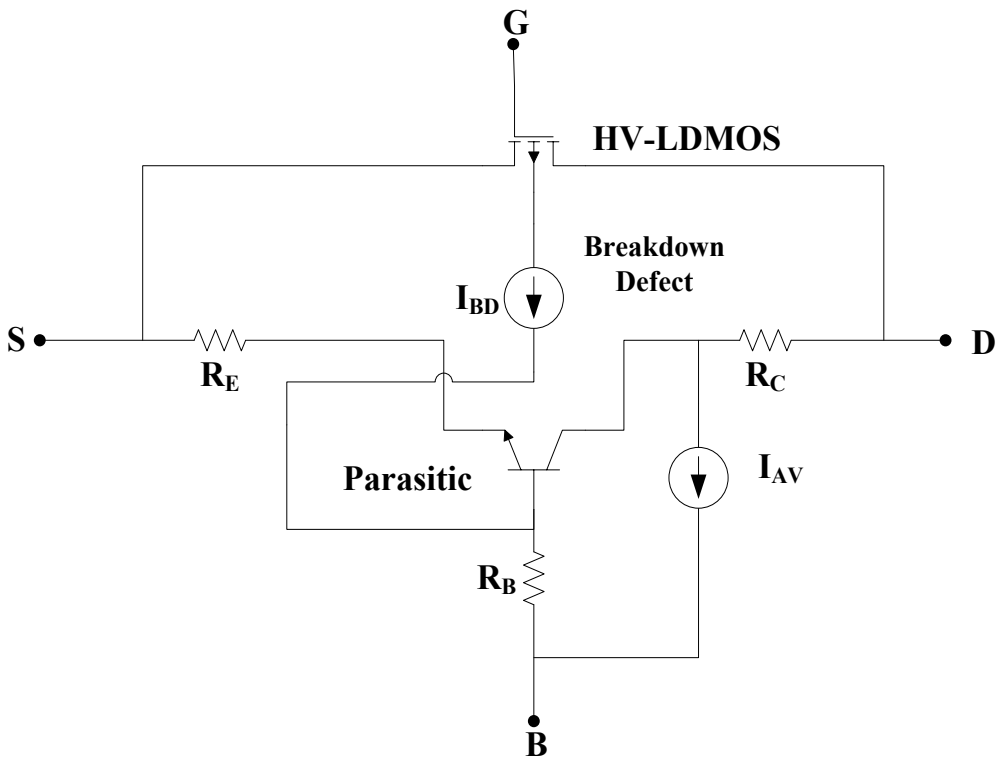
Avalanche breakdown depends on the magnitude of the gate voltage with respect to ground (V_G). When V_G is higher than V_{TH}, then the avalanche breakdown occurs at lower multiplication factor, and results in snapback breakdown occurring at a lower drain voltage.

6.2. HV-LDMOS Model with Gate-FOX Breakdown Defect under ESD Stress

Under fault-free case the HV-LDMOS has a parasitic BJT which is turned ON only when there is a voltage drop of 0.7 V in the substrate, which is represented by the avalanche current I_{av}. The HV-LDMOS model with gate-FOX breakdown structural defect is shown in Figure 50.

However, when the HV-LDMOS has a gate-FOX breakdown defect then there is an additional conducting channel from the gate to the substrate of the HV-LDMOS. This additional conducting channel adds to the avalanche current. The resultant current is sufficient to turn ON the parasitic BJT, and results in avalanche breakdown occurring at a lower drain voltage. If the ESD stress is sustained, then it eventually leads to snapback breakdown.

Figure 50. HV-LDMOS Model with Gate-FOX Breakdown Defect

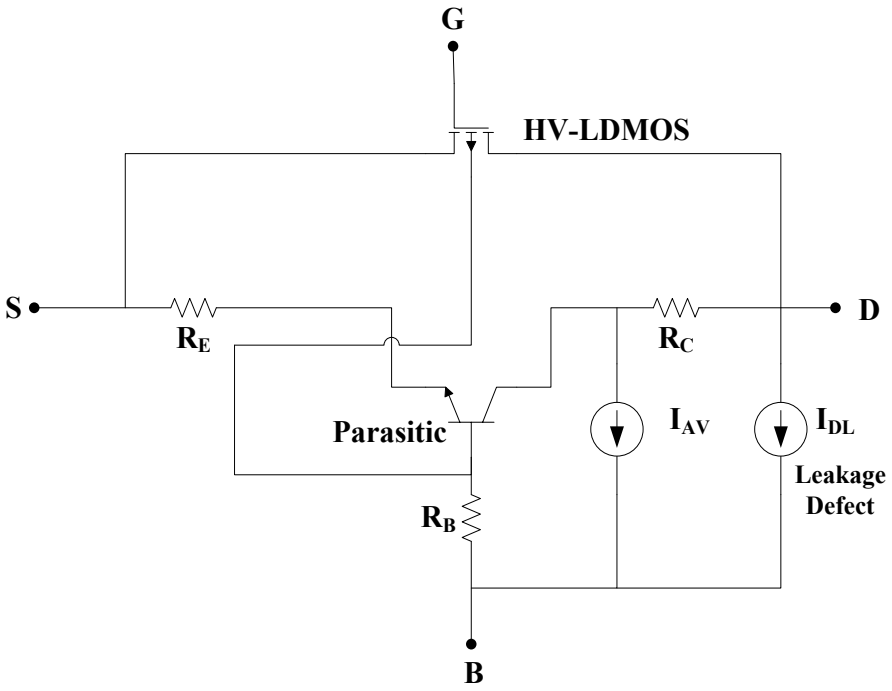


6.3. HV-LDMOS Model with Drain Leakage Defect under ESD Stress

The HV-LDMOS model with drain leakage structural defect is shown in Figure 51. Under ESD stress conditions, when there is a drain leakage defect in HV-LDMOS then it is represented by a current source I_{dl}, which is in parallel with the avalanche current I_{av}.

The two current conducting paths are internally connected to the base of the parasitic BJT, and turn it ON at a lower drain voltage. This results in avalanche and snapback breakdowns at lower drain voltages. Using these models we can test HV-LDMOS using low-voltage stimulus by subjecting it to ESD stress.

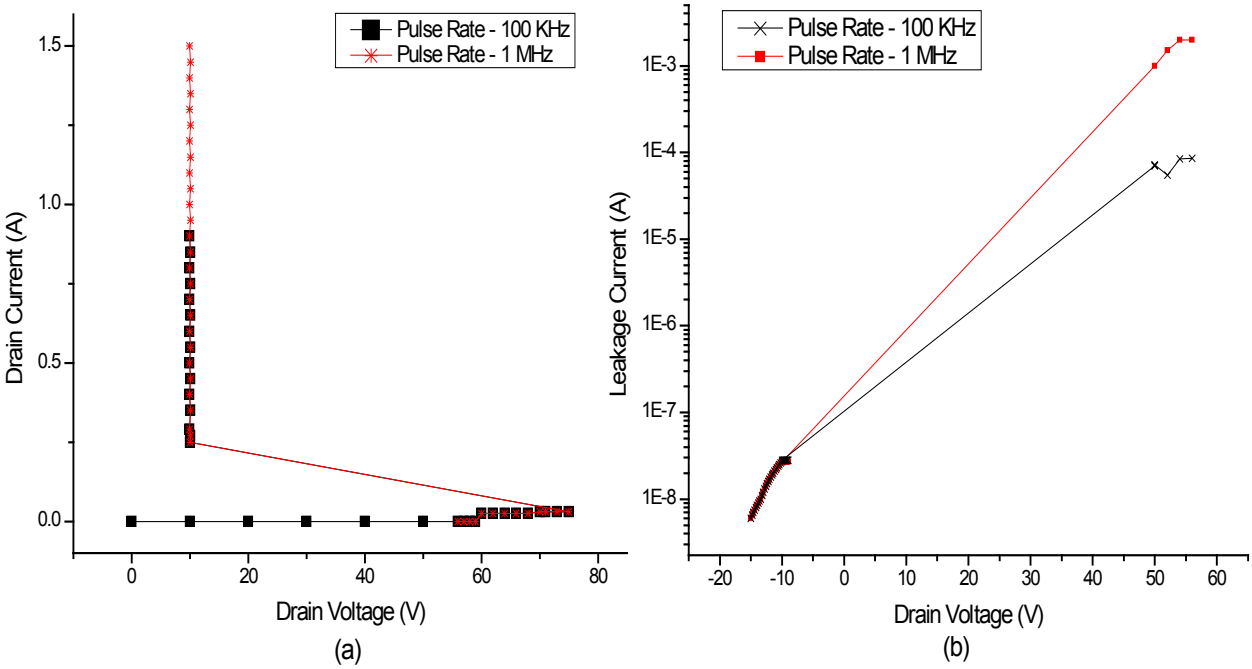
Figure 51. HV-LDMOS Model with Drain Leakage Defect



When snapback breakdown occurs due to the drain leakage defect the parasitic NPN is triggered ON, resulting in the accumulation of charge carriers in the FOX region. This charge

accumulation decreases the breakdown voltage levels as shown in Figure 52 (a), and results in the increase of leakage current. The breakdown voltage is dependent on the magnitude of the pulses and not the pulse rate; hence there is no change in the breakdown voltage when the pulse rate is increased from 100 KHz to 1 MHz. If HV-LDMOS is stressed with multiple transmission line pulses, then the device degradation due to trapped charge accumulation causes an increase in leakage current as shown in Figure 52 (b).

Figure 52. Transmission Line Pulse Simulation of HV-LDMOS with Drain Leakage Defect (a) Snapback Breakdown, (b) Leakage Current vs. Drain Voltage

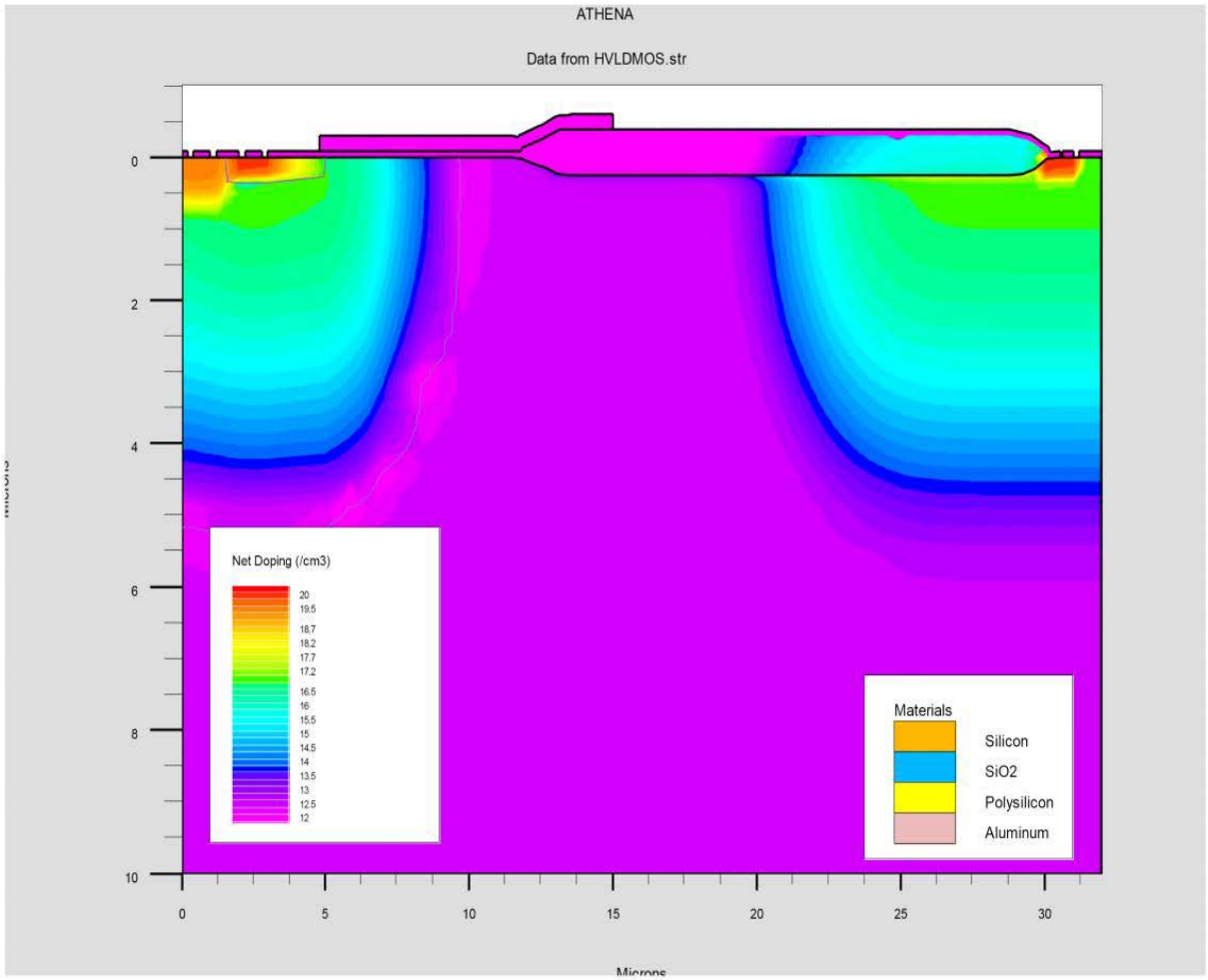


6.4. TEST SIMULATIONS

The models developed in the previous section were used to perform test simulations on HV-LDMOS using low-voltage stimulus. The gate of the HV-LDMOS was subjected to ESD

stress by using transmission line pulses. The curve fitting parameters required to compute the multiplication factor for LDMOS, was obtained by performing device simulation on ATHENA and ATLAS platforms. HV-LDMOS was built on ATHENA platform as shown in Figure 53.

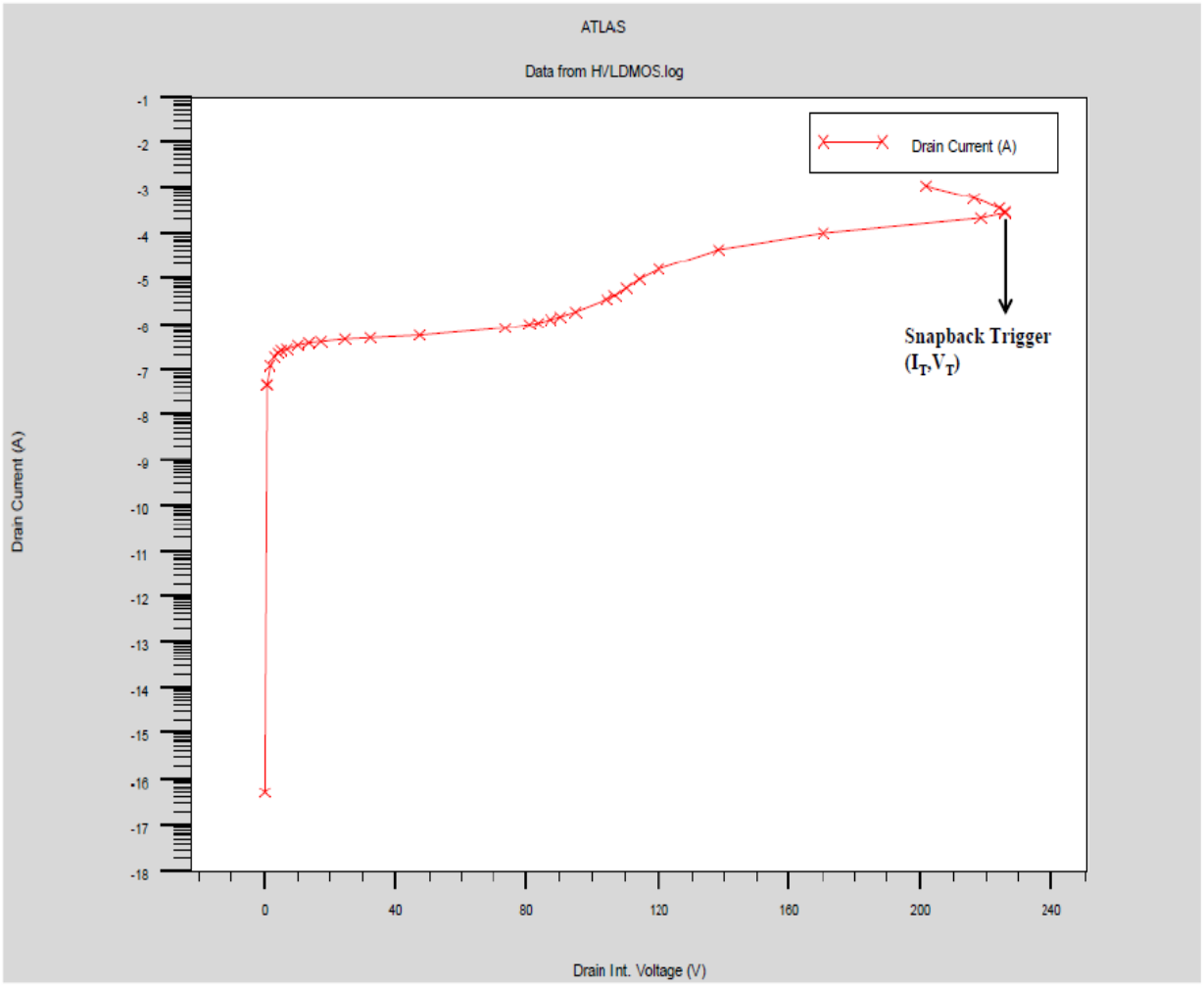
Figure 53. HV-LDMOS Structure using ATHENA



The different doping concentrations representing the device structure are shown in Figure 53. The purple area represents the p-type substrate with a doping concentration of $12/cm^3$, and the blue and green areas represent the drift region with a doping concentration of $16/cm^3$. The doping concentration of the drift region is much lower than that of the drain terminal. The drain

terminal is represented by the red region which has a doping concentration of $20/cm^3$. ATLAS simulation of the device was performed to obtain the curve fitting parameters, and the simulation result is shown in Figure 54.

Figure 54. ATLAS Simulation for HV-LDMOS



The curve fitting parameters were extracted from the ATLAS simulation, and used to compute avalanche current which is a function of the multiplication factor. The test simulations were performed using an analytical solution on MATLAB, and the results are shown in Table 12.

Table 12. HV-LDMOS Testing using Low-Voltage Stimulus

Test Condition	**Snapback Trigger (I_T,V_T)**
Fault Free	(88.46 mA, 892.32 V)
Soft-Breakdown	(45.64 mA, 450.73 V)
Hard-Breakdown	(16.3 mA, 170.46 V)
Drain Leakage (I_{dl} = 5 μA)	(7.34 mA, 16.83 V)

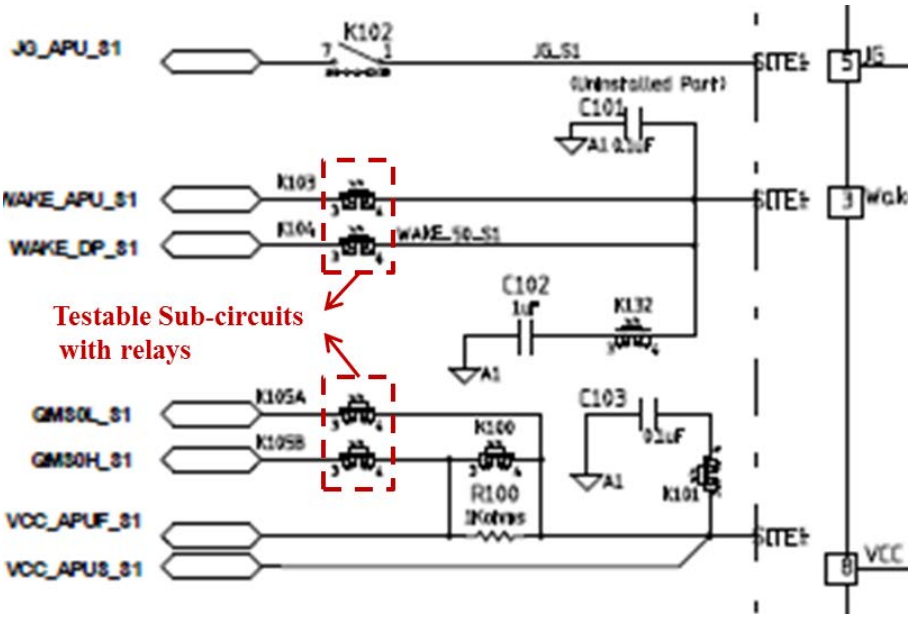
From Table 12, we can infer that the snapback trigger voltage (V_T) is very high for a fault-free HV-LDMOS. The snapback trigger voltage reduces to 450.73 V when there is a soft-breakdown in the gate-FOX of the HV-LDMOS, and decreases further for a hard-breakdown defect. When the leakage current in the device increases to 5 μA, the snapback breakdown occurs at a very low-voltage of 16.83 V. Hence, by subjecting the HV-LDMOS under ESD stress, we can detect structural defects by performing transmission line pulse simulations, and compute the trigger limits for snapback breakdown. The drain voltage can be further reduced, by increasing the magnitude of the transmission line pulses applied at gate voltage, and also varying the pulse rate and duration. This technique eliminates the use of high-voltage at the drain and ensures the safety of the person handling the ATE.

CHAPTER 7

CHARGE EXTRACTION AND TESTING HIGH-VOLTAGE DEVICE INTERFACE BOARDS

High-voltage DIBs (HV-DIBs) act as an interface between the ATE and DUT, facilitating in providing test stimulus to the DUT, and capturing the response. HV-DIBs are an intricate part of the test hardware, and it is extremely important to perform testing of HV-DIBs without the DUT in socket to verify its functionality. HV-DIBs essentially consist of high-voltage relays, which are automatically tested using the relay path module of HVPro. A typical HV-DIB with multiple relay circuits is shown in Figure 55.

Figure 55. Typical HV-DIB with testable relay circuits



HV-DIB testing is performed without the HV-LDMOS in the DUT socket, and the testable circuits are classified as circuits with relays by HVPro. These circuits are tested by turning the relays ON or OFF, and the pseudocode obtained for testing these high-voltage relays is shown in Figure 56.

Figure 56. Pseudocode for High-Voltage Relay Testing

```
*** NO EVEREST-DUT IN SOCKET ***


*** TEST ON CIRCUIT WITH RELAY ***
RELAY ON (RELAY BLOCK :K102)
FCMV (forced current = 300 mA, Force High Pin = P113_F2, Sense High Pin = P113_E2, Force Low Pin = A1,
Sense Low Pin = A1, )
COMPARE_LIMITS (lower limit = 0.92 V, upper limit = 1.14 V, nominal value = 1 V)
RELAY OFF (RELAY BLOCK :K102)
*** TEST ON CIRCUIT WITH RELAY ***
RELAY ON (RELAY BLOCK :K103)
FCMV (forced current = 300 mA, Force High Pin = P113_H9, Sense High Pin = P113_G9, Force Low Pin = A1,
Sense Low Pin = A1, )
COMPARE_LIMITS (lower limit = 0.92 V, upper limit = 1.14 V, nominal value = 1 V)
RELAY OFF (RELAY BLOCK :K103)
*** TEST ON CIRCUIT WITH RELAY ***
RELAY ON (RELAY BLOCK :K104)
FCMV (forced current = 300 mA, Force High Pin = P114_J5, Sense High Pin = A1, , Force Low Pin = A1, Sense
Low Pin = A1)
COMPARE_LIMITS (lower limit = 0.92 V, upper limit = 1.14 V, nominal value = 1 V)
RELAY OFF (RELAY BLOCK :K104)
```

The relays are capable of handling very high voltages, typically ranging from 700V to 1100 V. Since, the HV-DIBs consist of a large number of interconnects to facilitate signal transmission, the discharge time associated with these interconnects is a major issue that has to be addressed to ensure safety of engineers handling the test equipment. Electrostatic Discharge (ESD) has become one of the most critical reliability issues in testing integrated circuits (ICs),

and their corresponding DIBs. ESD related issues lead to test equipment damage; hence efficient protection techniques play a very critical role in testing both the high-voltage devices, and their DIBs. It is extremely important to design an ESD protection circuit for HV-LDMOS which not only protects the device, but will also provide an alternate discharge path to remove the high-voltage from the DIB at a faster rate. SCRs are traditionally used as ESD protection devices over a wide range of process technologies due to their superior ESD behavior [66, 67, and 68].

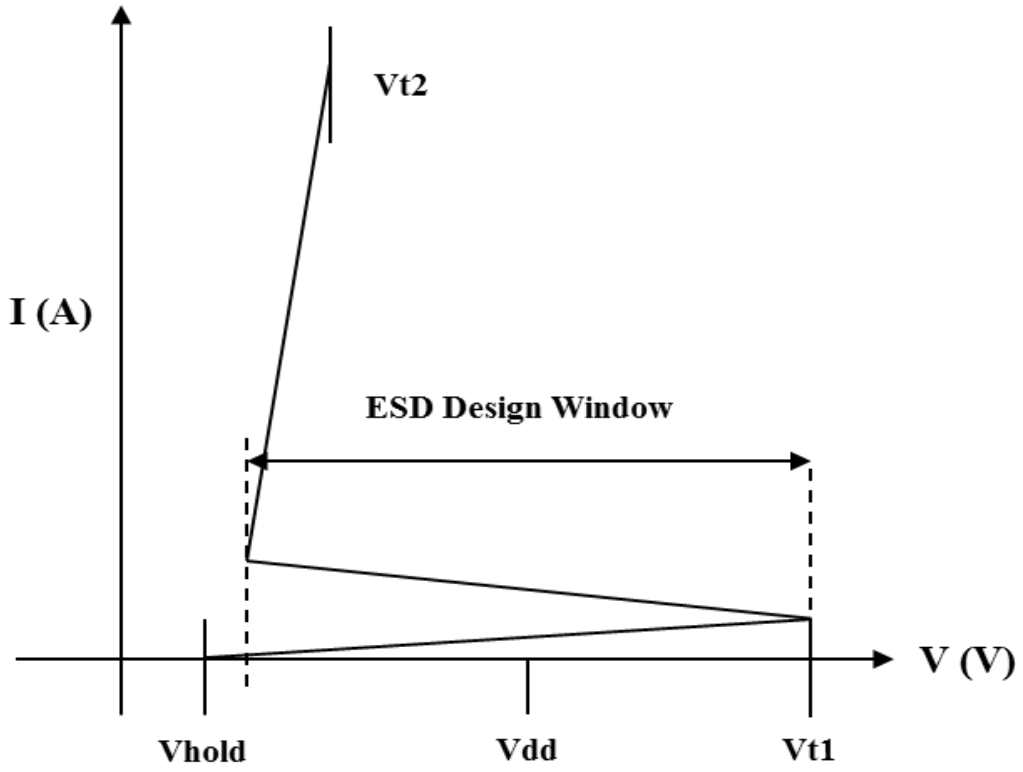
7.1. Electrostatic Discharge (ESD) Issues in HV-LDMOS

ESD protection for HV-LDMOS is extremely difficult due to the very low current capabilities of the parasitic NPN in the snapback mode. In conventional low voltage transistors, grounded gate n-MOS (GGNMOS) is used along with SCRs for ESD protection due to its straightforward implementation. However, in HV-LDMOS the variable resistance of the n-drift region at the drain terminal which allows high breakdown voltage levels, makes ESD protection a very tedious task. The different ESD related issues in HV-LDMOS are snapback breakdown, triggering non-uniform multi-finger structure, and intrinsic HV-LDMOS reliability [69].

7.1.1. Snapback Breakdown

The drain terminal is surrounded by a lightly doped n-drift region. The n-drift region acts as a variable resistance, which reduces the breakdown level and enables the transistor to withstand high voltages. The n-drift region has a doping concentration much lower than the drain terminal, and strongly affects the snapback behavior. Figure 57 shows the traditional snapback breakdown characteristic curve for HV-LDMOS.

Figure 57. Snapback Breakdown Characteristics of LDMOS [69]



The snapback triggering voltage (V_{t1}) for HV-LDMOS is much higher than the high voltage applied at the drain terminal. However, the snapback holding voltage (V_{hold}) still occurs at relatively low voltages, due to the Kirk effect appearing in the high current bipolar mode. This causes the avalanche breakdown region to shift, from the lightly doped n-drift region to the highly doped drain terminal in a fully conducting bipolar mode. The shift in avalanche breakdown region results in a large intrinsic avalanche field, and sustains the parasitic NPN operation at low holding voltages. If the Kirk effect is exhibited at increased bipolar current levels, then this avalanche region transition is accompanied by a double snapback breakdown [68].

7.1.2. TRIGGERING NON-UNIFORM MULTI-FINGER STRUCTURE

During multi-finger triggering, the uniformity condition that the trigger voltage is lesser than the failure voltage has to be maintained. In HV-LDMOS it is extremely difficult to maintain this uniformity condition. Adding ballast resistance to each finger cannot solve the huge voltage gap to be bridged. Conventional static gate biasing schemes for reducing the trigger voltage (V_{t1}) cannot be applied, as the maximum supply (high) voltage at the drain terminal is too high when compared with the holding voltage (V_{hold}). Other transient biasing schemes, such as capacitive gate coupling interferes with the normal circuit operation, and cannot be used to improve the ESD robustness of HV-LDMOS.

7.1.3. INTRINSIC HV-LDMOS RELIABILITY

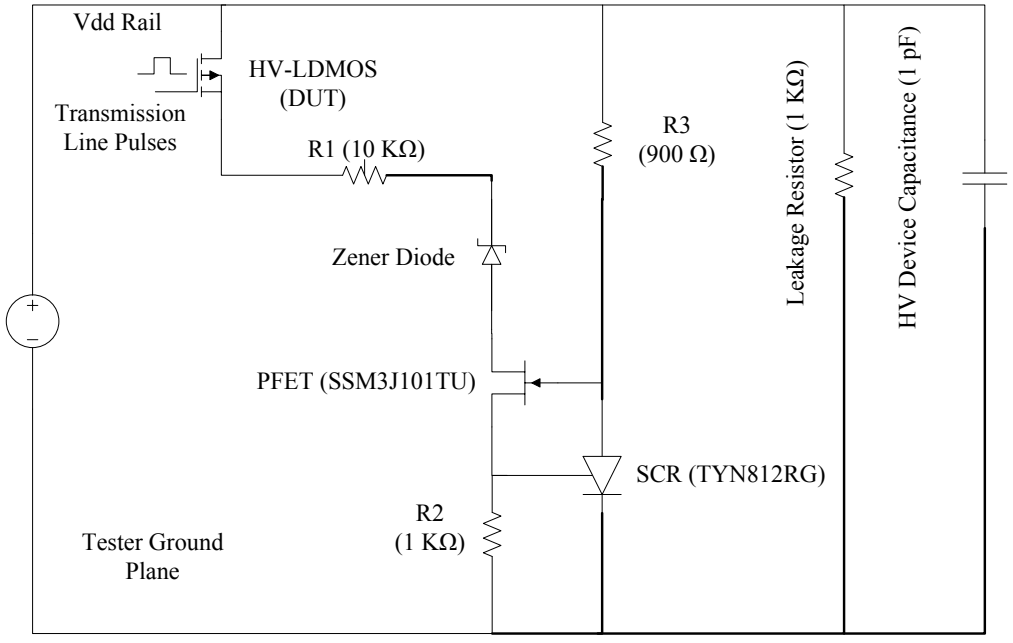
In HV-LDMOS, at the FOX bound active layers a serious device reliability problem occurs. During snapback breakdown the parasitic NPN transistor is triggered ON, resulting in the accumulation of charge carriers in the FOX region. This charge accumulation decreases the local breakdown voltage levels, and results in the increase of leakage current. If HV-LDMOS is stressed with multiple transmission line pulses, then the device degradation due to trapped charge accumulation causes an increase in leakage current [69]. This is done to identify the real failure current level.

7.2. NOVEL SCR BASED PROTECTION SCHEME FOR HV-LDMOS

Traditionally, transient voltage suppressors (TVSs) or back to back connected Zener diodes are used as ESD protection circuits for high voltage devices. TVSs are similar in

functionality to Zener diodes, and are designed to manage transient events related to power. TVSs for HV-LDMOS protection have a voltage rating as high as 1.5 KV, a stray capacitance of 1 nF and a maximum leakage current of 1 μA. However, TVSs are large in size and need to dissipate the accumulated voltage transients as heat energy. This requires heat sinks, which make the protection circuit large and cumbersome when used in HV-DIBs. SCRs are used as protection circuits mainly because of their superior ESD behavior, such as large failure currents, and low dynamic on-resistances. In SCRs, an ideal ESD performance by scaling the transistor width can be accomplished using the regenerative conduction mechanism with double current injection [70, 71].

Figure 58. PFET Triggering SCR Protection Circuit for 300 V HV-LDMOS [70]

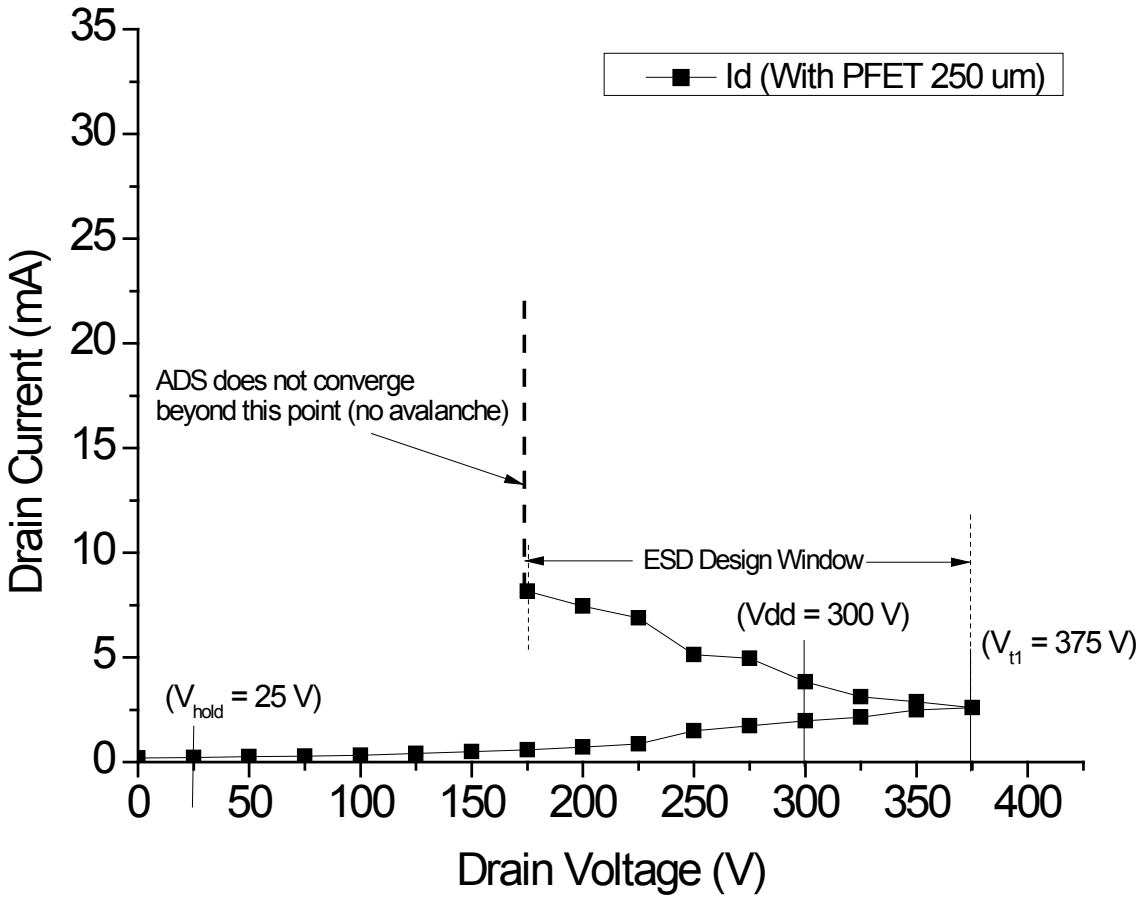


We have developed a novel SCR protection circuit for HV-LDMOS using a PFET triggered SCR. Most of the HV-LDMOS are designed for high voltage and low current ratings,

such as 1 mA. Therefore, using high holding current SCRs is not necessary. We can limit the output current by using a current limiting resistor (R1) on the DUT terminal, and then trigger the SCR using a PFET. The protection circuit is shown in Figure 58. The SCR is triggered when the PFET has a voltage drop of 0.7 V.

When an ESD stress event occurs between the DUT pin and the ground plane of the ATE, the SCR triggers immediately because the high voltage at the VDD makes the gate of the PFET float, and it is easy to forward bias the PFET. The Vdd line is capacitively coupled to the Vss through the chip capacitance.

Figure 59. Transmission Line Pulse Simulation Results for 300V HV-LDMOS [69]



During the ESD stress event, the current through the PFET is amplified, and it creates a voltage drop of 0.7 V over the resistor (R2). The SCR latches into a holding state and protect the HV-LDMOS. The width of the PFET affects the voltage drop across resistor (R2), and invariably the triggering action of the SCR [72]. The value of resistor (R2) is chosen to be large enough, so that the low current in the HV-LDMOS can still achieve the triggering action of the SCR. TLPs simulations of HV-LDMOS were performed with different PFET widths for the ESD protection scheme, and the simulation result is shown in Figure 59. From Figure 59, we can infer that a 200 V ESD design window can be achieved using this novel ESD protection scheme. The PFET width can be controlled to increase the ESD design window. SCRs have excellent clamping behavior which ensures that the HV-LDMOS remains protected. The novel ESD protection scheme protects the DUT, ATE, and also provides an alternate discharge path for safely removing the high-voltage from the DIB through the leakage resistor.

CHAPTER 8

CONCLUSION AND FUTURE DIRECTIONS

Two automatic test program generation tools for verification of DIBs used for IC testing have been presented in this dissertation. The first software tool (RADPro) is capable of generating test programs for RF-DIBs over various tester platforms. The challenge of test generation by manual inspection of schematics has been addressed using RADPro. RADPro automatically generates test instructions using the schematic information of the DIB, and the test generation is independent of the tester platform. RADPro automatically assigns the channel types to the pogo pins, and classifies the high and low sides of the circuit as one single testable sub-circuit. A novel test technique for testing embedded passive RF components was presented. This involves the use of a multi-tone dithered test stimulus and computing the peak-to-average ratio to identify process-related defects. RADPro induces faults in all testable passive components, and performs test simulations. The results of the test simulations are stored in a fault dictionary, and are matched with the ATE results to identify process-related defects. RADPro has been tested on mixed signal DIBs and ETS-DIBs to generate pseudocodes, which carry the generic test instructions to the ATE. It reduces test development time from several weeks to days, and reduces the time taken to market the IC.

The second software tool (HVPro) is capable of generating test programs for HV-DIBs, and performs functional testing of HV-LDMOS. The principles of RADPro were leveraged to develop HVPro, which is capable of performing both board and device level testing. Hybrid MOS-π model was developed to test HV-LDMOS. Fault models for structural defects were developed by inducing the physical defects into the hybrid MOS-π model. A low-cost test technique for testing HV-LDMOS was presented. This test technique uses the noise-reduction scheme to accurately make test measurements by overcoming the power supply and ATE noise. Experimental measurements were made on a MOSFET driver with a 700V LDMOS device to validate the test technique. The test technique was automated using HVPro, and pseudocodes were generated for both board and device level testing.

Charge extraction in HV-DIBs was addressed by developing a novel ESD protection scheme using SCR. The ESD protection scheme also provides an additional discharge path through the leakage resistor. This ensures the safety of personnel handling the ATE by. An alternate test technique to test HV-LDMOS using low-voltage stimulus was also presented. This test technique used transmission line pulses to induce ESD stress in the HV-LDMOS, and measure the snapback breakdown.

Development efforts are currently in progress to build a test setup, and make test measurements to validate the alternate test technique. Also work is in progress for developing bridge software, which will translate the pseudocode into the native language of the ATE.

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APPENDIX A

Model File Generation for ETS DIBs:

1. Model name:

   Model name of the component as it appears in the Bill of Materials

2. Power Pins: PWR <Pin numbers separated by commas>

   If there is no power nodes use “NA”.

3. Terminals of the component: PINS<list of inputs and outputs separated by commas>

   This is a list of one set of input and output separated by “|”.

4. Disregarded nodes: DISREGARD <Pin numbers separated by commas>

   Pins that is not included in any of the above categories.

5. Component Reference Designator: COMP<Ref Designator>

The following is the list of reference designators used for different components.

a. Relay: K
b. Resistor: R
c. Capacitor: C
d. Inductor: L
e. IC: U
f. Diode/ LED: D
g. Jumper/ SMA: J
h. Transistor: Q
i. RF Resistive Trace: RFR
j. RF Balun Transformer: RFB
k. RF Passive Filter: RFP

Model file example for an ETS DIB:

```
08051C103JAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
08055A150JAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
08055C104JAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
0805YA103JAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
0805ZC105KAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
12101C104KAT2A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
ECE-V2AA4R7UP PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
T491D225K050AS PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
199D104X9050AA1 PWR<NA> PINS<1,2> DISREGARD<NA> COMP<C>
1N914 PWR<NA> PINS<1,2> DISREGARD<NA> COMP<D>
1N5819 PWR<NA> PINS<1,2> DISREGARD<NA> COMP<D>
STPS1H100A PWR<NA> PINS<1,2> DISREGARD<NA> COMP<D>
SN74AS1034AD PWR<14,7> PINS<1,2|3,4|5,6|9,8|11,10|13,12> DISREGARD<NA> COMP<U>
IRF1607 PWR<NA> PINS<1,2,3> DISREGARD<NA> COMP<Q>
AD8561AN PWR<1,6|4,6> PINS<2,3,7|2,3,8> DISREGARD<5> COMP<U>
CAT24C04LI-G PWR<8,4> PINS<1,2,3,6,7,5> DISREGARD<NA> COMP<U>
OP27EZ PWR<7,4> PINS<1,2,6> DISREGARD<1,8,5> COMP<U>
JUMPER PWR<NA> PINS<1,2> DISREGARD<NA> COMP<J>
SML-LX1206GC-TR PWR<NA> PINS<1,2> DISREGARD<NA> COMP<D>
FBR51ND12-W1 PWR<NA> PINS<1,3> DISREGARD<4,2,5> COMP<K>
2911-12-321 PWR<NA> PINS<1,4|8,5> DISREGARD<2,3,6,7> COMP<K>
CRCW12062490F PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
TNPW12061503BT PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
CRCW12101002F PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
CRCW12104991F PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
ERA-6YEB102V PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
ERA-6YEB104V PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
ERA-6YEB392V PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
MP9100-50 PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
RES0805 PWR<NA> PINS<1,2> DISREGARD<NA> COMP<R>
AD8052ARM PWR<4,15|8,-15> PINS<3,2,1|5,6,7> DISREGARD<NA> COMP<U_T>
AD8605ART PWR<1,2> PINS<4,3,1> DISREGARD<5,7> COMP<U_T>
THS4012ID PWR<8,15|4,12> PINS<2,3,1|6,5,7> DISREGARD<NA> COMP<U_T>
2332-12-020 PWR<NA> PINS<1,4|8,5> DISREGARD<1,2,4,7,8> COMP<K>
AGN200A4H PWR<1,2> PINS<3,2,4|6,7,5> DISREGARD<2,3> COMP<U>
AD8051ART PWR<1> PINS<4,3,1> DISREGARD<3> COMP<U>
AD9631AR PWR<1> PINS<2,3,6> DISREGARD<3> COMP<U>
OP4177ARU PWR<1> PINS<2,3,1|6,5,7|13,12,14|9,10,8> DISREGARD<3> COMP<U>
RF303YZ-12 PWR<1> PINS<2,3,4|8,6,7> DISREGARD<3> COMP<K>
9852-05-00 PWR<NA> PINS<6,3,5> DISREGARD<NA> COMP<K>
SN74LVC1G125DBV PWR<NA> PINS<2,4> DISREGARD<NA> COMP<U>
SN74LVC1G32DBV PWR<NA> PINS<1,2,4> DISREGARD<NA> COMP<U>
SN75468D PWR<NA> PINS<1,2,3,4,5,6,7,10,11,12,13,14,15,16> DISREGARD<NA> COMP<U_NT>
AGN200A12 PWR<1> PINS<3,2,4|6,7,5> DISREGARD<3> COMP<U>
RC1206USERDEF PWR<1> PINS<1000000000> DISREGARD<NA> COMP<R>
TC32-1002BXT1 PWR<10> PINS<10000> DISREGARD<NA> COMP<R>
S102K1K200.01% PWR<1> PINS<10000> DISREGARD<NA> COMP<R>
RES-SMT0402_UNINSTALLED PWR<1> PINS<19.99> COMP<R>
RES0402(UN) PWR<21> PINS<1G> COMP<R>
CAP-SMT1206-UNINSTALLED PWR<12> PINS<100000> COMP<C>
CAP-SMT0402-UNINSTALLED PWR<12> PINS<1p> DISREGARD<2> COMP<C>
```

APPENDIX B

Input Files for ETS DIB:

Parts List and Netlist:

PARTS LIST

```
08051C103JAT2A  08051C103JAT2A  C412   C115   C107
08051C103JAT2A  08051C103JAT2A  C109   C116   C207
08051C103JAT2A  08051C103JAT2A  C209   C212   C112
08051C103JAT2A  08051C103JAT2A  C415   C216   C409
08051C103JAT2A  08051C103JAT2A  C407   C416   C316
08051C103JAT2A  08051C103JAT2A  C307   C309   C315
08051C103JAT2A  08051C103JAT2A  C312   C215

08055A150JAT2A  08055A150JAT2A  C417   C317   C217
08055A150JAT2A  08055A150JAT2A  C117

08055C104JAT2A  08055C104JAT2A  C401   C301   C201
08055C104JAT2A  08055C104JAT2A  C101

0805YA103JAT2A  0805YA103JAT2A  C306   C106   C406
0805YA103JAT2A  0805YA103JAT2A  C206

0805ZC105KAT2A  0805ZC105KAT2A  C211   C108   C111
0805ZC105KAT2A  0805ZC105KAT2A  C213   C110   C114
0805ZC105KAT2A  0805ZC105KAT2A  C208   C410   C313
0805ZC105KAT2A  0805ZC105KAT2A  C210   C411   C308
0805ZC105KAT2A  0805ZC105KAT2A  C310   C113   C311
0805ZC105KAT2A  0805ZC105KAT2A  C214   C408   C314
0805ZC105KAT2A  0805ZC105KAT2A  C414   C413

12101C104KAT2A  12101C104KAT2A  C405   C205   C105
12101C104KAT2A  12101C104KAT2A  C305

199D104X9050AA1 199D104X9050AA1 C99

1N5819      1N5819      SD103  SD203  SD303
1N5819      1N5819      SD403

1N914       1N914       D209   D211   D207
1N914       1N914       D206   D204   D216
1N914       1N914       D202   D100   D201
1N914       1N914       D200   D101   D210
1N914       1N914       D408   D203   D110
1N914       1N914       D102   D306   D304
1N914       1N914       D416   D112   D118
1N914       1N914       D104   D106   D413
1N914       1N914       D412   D117   D113
1N914       1N914       D116   D111

2911-12-321   2911-12-321   K_CAL2_S3K_CAL1_S3K_RT_S3
2911-12-321   2911-12-321   K_MPUS2PH_S3K_CAL4_S3K_CP2SRV_S3
2911-12-321   2911-12-321   K_CAL3_S3K_CAL2_S3K_CAL3_S1
2911-12-321   2911-12-321   K_CP2SRV_S3K_CP2VS_S3K_SRV1X_S4
2911-12-321   2911-12-321   K_CP2VS_S3K_CAL3_S3K_SRVCAL_S3
2911-12-321   2911-12-321   K_CAL2_S1K_DIV_S3 K_SRVCAL_S4
AD8561AN      AD8561AN      U302   U402   U202
AD8561AN      AD8561AN      U102

B66.20.06.00.19 B66.20.06.00.19 SITE2  SITE3  SITE1
B66.20.06.00.19 B66.20.06.00.19 SITE4
```

CAT24C04LI-G CAT24C04LI-G U99

CRCW06034021F CRCW06034021F R235 R435 R135
CRCW06034021F CRCW06034021F R335

CRCW0805000Z CRCW0805000Z R331 R328 R128
CRCW0805000Z CRCW0805000Z R219 R217 R216
CRCW0805000Z CRCW0805000Z R215 R214 R231
CRCW0805000Z CRCW0805000Z R101 R301 R114
CRCW0805000Z CRCW0805000Z R228 R119 R131
CRCW0805000Z CRCW0805000Z R117 R116 R115
CRCW0805000Z CRCW0805000Z R201 R417 R319
CRCW0805000Z CRCW0805000Z R401 R431 R428
CRCW0805000Z CRCW0805000Z R317 R316 R315
CRCW0805000Z CRCW0805000Z R414 R415 R416
CRCW0805000Z CRCW0805000Z R419 R314

CRCW08051000F CRCW08051000F R312 R412 R200
CRCW08051000F CRCW08051000F R100 R300 R112
CRCW08051000F CRCW08051000F R400 R212

CRCW080510R0F CRCW080510R0F R438 R440 R439
CRCW080510R0F CRCW080510R0F R437

CRCW08051502F CRCW08051502F R403 R203 R303
CRCW08051502F CRCW08051502F R103

CRCW080540R2F CRCW080540R2F R118 R318 R418
CRCW080540R2F CRCW080540R2F R218

CRCW12061002F CRCW12061002F R320 R420 R120
CRCW12061002F CRCW12061002F R220

CRCW120610R0F CRCW120610R0F R324 R224 R124
CRCW120610R0F CRCW120610R0F R424

CRCW12062211F CRCW12062211F R98 R99

CRCW12065111F CRCW12065111F R311 R411 R111
CRCW12065111F CRCW12065111F R211

CRCW12066490F CRCW12066490F R91

CRCW12067500F CRCW12067500F R93 R90

CRCW12101002F CRCW12101002F R108 R308 R408
CRCW12101002F CRCW12101002F R208

CRCW12104991F CRCW12104991F R107 R407 R307
CRCW12104991F CRCW12104991F R207

ECE-V2AA4R7UP ECE-V2AA4R7UP C204 C304 C104
ECE-V2AA4R7UP ECE-V2AA4R7UP C404

ERA-6YEB102V ERA-6YEB102V R329 R229 R129
ERA-6YEB102V ERA-6YEB102V R429

ERA-6YEB104V ERA-6YEB104V R204 R404 R304
ERA-6YEB104V ERA-6YEB104V R104

ERA-6YEB392V ERA-6YEB392V R432 R132 R332
ERA-6YEB392V ERA-6YEB392V R232

ETS600-POGO_143P ETS600-POGO_143P P111 P106 P111
ETS600-POGO_143P ETS600-POGO_143P P106 P114 P106

ETS600-POGO_143P ETS600-POGO_143P P114 P106 P114
ETS600-POGO_143P ETS600-POGO_143P P106 P111 P114
ETS600-POGO_143P ETS600-POGO_143P P111 P106 P114
ETS600-POGO_143P ETS600-POGO_143P P111 P114 P111
ETS600-POGO_143P ETS600-POGO_143P P214 P103 P214
ETS600-POGO_143P ETS600-POGO_143P P103 P214 P106
ETS600-POGO_143P ETS600-POGO_143P P214 P103 P214
ETS600-POGO_143P ETS600-POGO_143P P103 P214 P103
ETS600-POGO_143P ETS600-POGO_143P P214 P103 P214
ETS600-POGO_143P ETS600-POGO_143P P103 P214 P103
ETS600-POGO_143P ETS600-POGO_143P P214 P106 P214
ETS600-POGO_143P ETS600-POGO_143P P106 P114 P106
ETS600-POGO_143P ETS600-POGO_143P P114 P106 P103
ETS600-POGO_143P ETS600-POGO_143P P106 P214 P106
ETS600-POGO_143P ETS600-POGO_143P P103 P106 P103
ETS600-POGO_143P ETS600-POGO_143P P214 P103 P214
ETS600-POGO_143P ETS600-POGO_143P P206 P214 P206

NET LIST

NODENAME 12V $
K_SRV1X_S1 1 D111 1 D105 1 K_CAL4_S1 1 $
D112 1 D405 1 K_CAL2_S1 1 $
D402 1 K_SRV1X_S4 1 K_CAL1_S4 1 $
K_RT_S4 1 K_RT_S2 1 K_DIV_S1 1 $
D113 1 D202 1 K_CAL3_S1 1 $
D116 1 P114 B5 D403 1 $
C91 1 D401 1 K_CBULK_S4 1 $
K_CBULK_S2 1 K_BOOT_S2 1 K_CAL3_S4 1 $
D416 1 D108 1 K_CAL2_S4 1 $
K_SRVCAL_S1 1 D411 1 D210 1 $
D200 1 K_DIV_S4 1 D409 1 $
D207 1 D203 1 D404 1 $
K_CP2SRV_S4 1 D407 1 K_MPUS2PH_S4 1 $
D408 1 D412 1 D201 1 $
K_SRVCAL_S4 1 K_CP2VS_S4 1 D406 1 $
K_CAL4_S4 1 K_EN2G_S4 1 D413 1 $
D217 1 D117 1 D318 1 $
K_CP2SRV_S3 1 D309 1 K_MPUS2PH_S3 1 $
K_SP2BT_S3 1 D317 1 D311 1 $
K_CAL2_S3 1 K_CAL4_S2 1 K_SP2PH_S2 1 $
D307 1 K_SP2BT_S2 1 R91 1 $
D316 1 K_CAL3_S3 1 D212 1 $
D313 1 K_DIV_S3 1 K_SP2PH_S1 1 $
K_MPUF2PH_S3 5 K_DIV_S2 1 K_BOOT_S4 1 $
K_SP2BT_S1 1 K_CAL4_S3 1 D218 1 $
K_SRV1X_S2 1 D208 1 D107 1 $
K_MPUF2PH_S4 5 K_MPUF2PH_S2 5 K_MPUF2PH_S1 5 $
D310 1 D300 1 K_BOOT_S3 1 $
K_SRVCAL_S2 1 D301 1 K_CBULK_S3 1 $
K_SP2PH_S3 1 K_RT_S3 1 D312 1 $
D205 1 D303 1 K_SP2PH_S4 1 $
D418 1 K_CAL1_S3 1 K_SP2BT_S4 1 $
D417 1 D304 1 D306 1 $
K_CP2VS_S3 1 K_EN2G_S2 1 D302 1 $
D204 1 K_RT_S1 1 D103 1 $
D213 1 K_CP2VS_S2 1 D118 1 $
D104 1 D106 1 K_CP2VS_S1 1 $
D102 1 P103 B5 K_CAL1_S1 1 $
K_CP2SRV_S1 1 P111 B5 K_CAL1_S2 1 $
D410 1 D109 1 K_MPUS2PH_S1 1 $
P106 B5 D400 1 D206 1 $
K_MPUS2PH_S2 1 D110 1 K_EN2G_S3 1 $
K_CAL3_S2 1 D305 1 K_SRV1X_S3 1 $
D216 1 K_SRVCAL_S3 1 K_CAL2_S2 1 $

D308 1 D211 1 D209 1 $
K_CP2SRV_S2 1 K_CBULK_S1 1 D101 1 $
D100 1 K_BOOT_S1 1 K_EN2G_S1 1
NODENAME 15V $
C90 1 R222 1 P103 G3 R122 1 $
R422 1 P103 G4 P103 F2 $
P103 F3 R322 1 R90 1
NODENAME 24V $
P103 H3 P103 I4 P103 H2 P103 I3 $
C94 1
NODENAME 5V $
U203 14 C214 1 C215 1 U303 14 $
C314 1 C315 1 R440 1 $
R439 1 C115 1 P111 B9 $
R437 1 P106 B9 U99 8 $
P114 B7 R92 1 P111 B7 $
C114 1 P106 B7 U103 14 $
U403 14 C414 1 C415 1 $
R438 1 C92_4 1 P103 B9 $
P114 B9 R99 1 C92_3 1 $
C92_1 1 P103 B7 C99 1 $
C92_2 1 R98 1
NODENAME 12V1 $
P103 C3 P103 C4 C97 2
NODENAME 15V1 $
R223 1 P103 E3 P103 D2 R123 1 $
R323 1 C93 2 P103 E4 $
R423 1 R93 1 P103 D3
NODENAME 24V1 $
P103 J2 C95 2 P103 J3
NODENAME 52V $
P106 B11 P114 B11 P103 B11 P111 B11 $
C96 2
NODENAME AGND1 $
C105 2 SITE1 9F SITE1 9S P113 D10 $
P113 C3 P113 D3 R103 1 $
P113 C10 P113 E7 P113 F7 $
J101 1 SD102 2 C104 2
NODENAME AGND2 $
C205 2 P112 F9 C204 2 R203 1 $
P112 E9 J201 1 P112 C12 $
SD202 2 P112 D12 P112 D5 $
P112 C5 SITE2 9S SITE2 9F
NODENAME AGND3 $
P105 F7 P105 C3 P105 D3 P105 C10 $
P105 D10 R303 1 C304 2 $
C305 2 P105 E7 SD302 2 $
SITE3 9S J301 1 SITE3 9F
NODENAME AGND4 $
P104 F9 P104 D12 SD402 2 P104 E9 $
C405 2 P104 C5 P104 D5 $
P104 C12 SITE4 9S R403 1 $
J401 1 C404 2 SITE4 9F
NODENAME BOOTS1 $
SITE1 1S SITE1 1F SD101 1 R101 1 $
K_BOOT_S1 5
NODENAME BOOTS2 $
SITE2 1S SITE2 1F K_BOOT_S2 5 SD201 1 $
R201 1
NODENAME BOOTS3 $
K_BOOT_S3 5 SD301 1 SITE3 1S SITE3 1F $
R301 1
NODENAME BOOTS4 $
SITE4 1F SD401 1 SITE4 1S R401 1 $
K_BOOT_S4 5

NODENAME BTSRCS1 $
K_SP2BT_S1 5 K_BOOT_S1 8 P113 H2 P113 G2 $
SD101 2
NODENAME BTSRCS2 $
SD201 2 K_SP2BT_S2 5 P112 G7 P112 H7 $
K_BOOT_S2 8
NODENAME BTSRCS3 $
P105 G2 K_SP2BT_S3 5 P105 H2 SD301 2 $
K_BOOT_S3 8
NODENAME BTSRCS4 $
K_BOOT_S4 8 P104 G7 P104 H7 K_SP2BT_S4 5 $
SD401 2
NODENAME CALS1 $
K_CAL1_S1 5 K_CAL2_S1 8
NODENAME CALS2 $
K_CAL2_S2 8 K_CAL1_S2 5
NODENAME CALS3 $
K_CAL2_S3 8 K_CAL1_S3 5
NODENAME CALS4 $
K_CAL2_S4 8 K_CAL1_S4 5

Bill of Materials:

ITEM	QTY	MFG	MFG PART#	REF DES	DESCRIPTION	VALUE or FUNCTION
		MILLENNIUM (TKY)				
REF	NONE REQUESTED	6486024B	-		ASSEMBLY	-
REF	-	6486024C	-		SCHEMATIC	-
1	NONE REQUESTED	6486024B	-		FABRICATION	-
REF	-	6486024B	-		ARTWORK	-
1	1	NEWARK	6437988		"HARDWARE KIT, EAGLE ETS-364/ETS-600 HIB"	
2	20	AVX	08051C103JAT2A	"C107, C109, C112, C115, C116, C207, C209, C212, C215, C216, C307, C309, C312, C315, C316, C407, C409, C412, C415, C416"	"CAP,SMT,0805"	"CAPACITOR,SMT,0805,CERAMIC,0.01uF,100V,5%,X7R"
3	4	AVX	08055A150JAT2A	"C117, C217, C317, C417"	"CAP,SMT,0805"	"CAPACITOR,SMT,0805,CERAMIC,50V,5%, 15pF,COG(NPO)"
4	4	AVX	08055C104JAT2A	"C101, C201, C301, C401"	"CAP,SMT,0805"	"CAPACITOR,SMT,0805,CERAMIC,0.1uF,50v,5%,X7R"
5	4	AVX	0805YA103JAT2A	"C106, C206, C306, C406"	"CAP,SMT,0805"	"CAPACITOR,SMT,0805,CERAMIC,16V,5%, 0.01uF,COG(NPO)"
6	20	AVX	0805ZC105KAT2A	"C108, C110, C111, C113, C114, C208, C210, C211, C213, C214, C308, C310, C311, C313, C314, C408, C410, C411, C413, C414"	"CAP,SMT,0805"	"CAPACITOR,SMT,0805,CERAMIC,1.0uF,10V,10%,X7R"
7	4	AVX	12101C104KAT2A	"C105, C205, C305, C405"	"CAP,SMT,1210"	"CER,CAP,SMT,0.1uF,100nF,100V,10%,X7R"
8	4	PANASONIC	ECE-V2AA4R7UP	"C104, C204, C304, C404"	"CAP,SMT,ELEC"	"CAP,SMT,ELE,RAD,VS SERIES,20%,100V, 4.7uF"
9	11	KEMET	T491D225K050AS	"C90, C91, C93, C94, C95, C96, C97, C92_1, C92_2, C92_3, C92_4"	"CAP,SMT,TAN,CASE-D"	"CAP,SMT,TAN,2.2uF,50V,10%,ESR-2.5ohm@100K"

10 1 VISHAY / SPRAGUE 199D104X9050AA1 C99 "CAPACITOR,THU,2P" "CAPACITOR,THU,2P,TANTALUM,0.1uF,50V,10%"

11 4 MULTITEST B66.20.06.00.19 "SITE1, SITE2, SITE3, SITE4" CONTACTOR CUSTOMER INSTALL

12 68 1N914 "D100, D101, D102, D103, D104, D105, D106, D107, D108, D109, D110, D111, D112, D113, D116, D117, D118, D200, D201, D202, D203, D204, D205, D206, D207, D208, D209, D210, D211, D212, D213, D216, D217, D218, D300, D301, D302, D303, D304, D305, D306, D307," "DIODE,1N914" "DIODE,1N914"

"D308, D309, D310, D311, D312, D313, D316, D317, D318, D400, D401, D402, D403, D404, D405, D406, D407, D408, D409, D410, D411, D412, D413, D416, D417, D418"

13 8 ST MICRO STPS1H100A "SD101, SD102, SD201, SD202, SD301, SD302, SD401, SD402" "DIODE,SMT,SMA" "SCHOTTKY RECTIFIERS,SMT,100V,1A"

14 4 DIODES INC 1N5819 "SD103, SD203, SD303, SD403" "DIODE,THU,2P" SCHOTTKEY DIODE

15 4 TI SN74AS1034AD "U103, U203, U303, U403" "IC,SMT,SOIC-14N" "HEX DRIVERS, RoHS"

16 8 INTERNATIONAL RECTIFIER IRF1607 "M101, M102, M201, M202, M301, M302, M401, M402" "IC,THU,3P,TO220AB" "POWER MOSFET,N-CHAN,75V,142A,0.0075 OHM,380W"

17 4 ANALOG DEVICES AD8561AN "U102, U202, U302, U402" "IC,THU,DIP-8" ULTRAFAST 7ns SINGLE SUPPLY COMPARATOR

18 1 CATALYST SEMICONDUCTOR CAT24C04LI-G U99 "IC,THU,DIP-8" "4-Kb CMOS SERIAL EEPROM,1.8~5.5V,DIP-8,NiPdAu"

19 4 ANALOG OP27EZ "U101, U201, U301, U401" "IC,THU,DIP-8W,300MIL" "LOW NOISE, HIGH SPEED PREC. OPAMP"

20 4 ANY wire jumper "J101, J201, J301, J401" JUMPER INSTALLED ANY BRAND 2PIN THU JUMPER

21 4 LUMEX SML-LX1206GC-TR "LED1, LED2, LED3, LED4" "LED,SMT" "GREEN,SMT,20mA"

22 4 FUJITSU FBR51ND12-W1 "K_MPUF2PH_S1, K_MPUF2PH_S2, K_MPUF2PH_S3, K_MPUF2PH_S4" "RELAY,THU,5P" "RELAY,THU,5P,EMR,SPDT,1FC,12V,25A,240R COIL,W1 OPTION"

23 64 *COTO TECHNOLOGY 2911-12-321 "K_CP2SRV_S1, K_CP2SRV_S2, K_CP2SRV_S3, K_CP2SRV_S4, K_CP2VS_S1, K_CP2VS_S2, K_CP2VS_S3, K_CP2VS_S4, K_CBULK_S1, K_CBULK_S2, K_CBULK_S3, K_CBULK_S4, K_RT_S1, K_RT_S2, K_RT_S3, K_RT_S4, K_CAL1_S1, K_CAL1_S2, K_CAL1_S3, K_CAL1_S4, K_CAL3_S1, K_CAL3_S2," "RELAY,THU,7P" "RELAY,THU,7P,RR,SPDT,1FC,12V,0.25A,1.5K COIL,COAXIAL SHIELD"

"K_CAL3_S3, K_CAL3_S4, K_CAL2_S1, K_CAL2_S2, K_CAL2_S3, K_CAL2_S4, K_BOOT_S1, K_BOOT_S2, K_BOOT_S3, K_BOOT_S4, K_MPUS2PH_S1, K_MPUS2PH_S2, K_MPUS2PH_S3, K_MPUS2PH_S4, K_CAL4_S1, K_CAL4_S2, K_CAL4_S3, K_CAL4_S4, K_DIV_S1, K_DIV_S2, K_DIV_S3, K_DIV_S4,"

"K_EN2G_S1, K_EN2G_S2, K_EN2G_S3, K_EN2G_S4, K_SRV1X_S1, K_SRV1X_S2, K_SRV1X_S3, K_SRV1X_S4, K_SRVCAL_S1, K_SRVCAL_S2, K_SRVCAL_S3, K_SRVCAL_S4, K_SP2BT_S1, K_SP2BT_S2, K_SP2BT_S3, K_SP2BT_S4, K_SP2PH_S1, K_SP2PH_S2, K_SP2PH_S3, K_SP2PH_S4"

24 4 VISHAY CRCW06034021F "R135, R235, R335, R435" "RES,SMT,0603" "RESISTOR,SMT,0603,1%,1/10W,4.02K"

25 32 VISHAY CRCW0805000Z "R101, R114, R115, R116, R117, R119, R128, R131, R201, R214, R215, R216, R217, R219, R228, R231, R301, R314, R315, R316, R317, R319, R328, R331, R401, R414, R415, R416, R417, R419, R428, R431" "RES,SMT,0805" "RESISTOR,SMT,0805,THICK FILM,0 OHM,1/8W"

26 8 VISHAY CRCW08051000F "R100, R112, R200, R212, R300, R312, R400, R412" "RES,SMT,0805" "RESISTER,SMT,0805,THICK FILM,1%,1/8W,100 OHM"

27 4 VISHAY CRCW080510R0F "R437, R438, R439, R440" "RES,SMT,0805" "RESISTER,SMT,0805,THICK FILM,1%,1/8W,10.0 OHM"

28 4 VISHAY CRCW08051502F "R103, R203, R303, R403" "RES,SMT,0805" "RESISTER,SMT,0805,THICK FILM,1%,1/8W,15.0K"

29 4 VISHAY CRCW080540R2F "R118, R218, R318, R418" "RES,SMT,0805" "RESISTER,SMT,0805,THICK FILM,1%,1/8W,40.2 OHM"

30 4 VISHAY CRCW12061002F "R120, R220, R320, R420" "RES,SMT,1206" "RESISTOR,SMT,1206,10K,1%,1/4W"

31 4 VISHAY CRCW120610R0F "R124, R224, R324, R424" "RES,SMT,1206" "RESISTOR,SMT,1206,10 OHM,1%,1/4W"

32 2 VISHAY CRCW12062211F "R98, R99" "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,2.21K"

33 8 VISHAY CRCW12062261F "R126, R134, R226, R234, R326, R334, R426, R434" "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,2.26K"

34 1 VISHAY CRCW12062490F R92 "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,249 OHM"

35 8 VISHAY CRCW12064990F "R109, R110, R209, R210, R309, R310, R409, R410" "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,499 OHM"

36 16 VISHAY CRCW120649R9F "R106, R122, R123, R127, R206, R222, R223, R227, R306, R322, R323, R327, R406, R422, R423, R427" "RES,SMT,1206" "RESISTOR,SMT,1206,49.9 OHM,1%,1/4W"

37 8 VISHAY CRCW120649R9FK "R105, R113, R205, R213, R305, R313, R405, R413" "RES,SMT,1206" "THICK FILM RESIST0R,SMT,1206,49.9 OHM,1%,1/4W,100ppm"

38 4 VISHAY CRCW12065111F "R111, R211, R311, R411" "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,5.11K"

39 1 VISHAY CRCW12066490F R91 "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,649 OHM"

40 2 VISHAY CRCW12067500F "R90, R93" "RES,SMT,1206" "RESISTOR,SMT,1206,1%,1/4W,750 OHM"

41 4 VISHAY TNPW12061503BT9 "R121, R221, R321, R421" "RES,SMT,1206" "RESISTOR,SMT,1206,150K,0.1%,1/8W,25ppm,T9"

42 4 VISHAY CRCW12101002F "R108, R208, R308, R408" "RES,SMT,1210" "RESISTOR,SMT,1210,1%,1/3W,10.0K OHM"

43 4 VISHAY CRCW12104991F "R107, R207, R307, R407" "RES,SMT,1210" "RESISTOR,SMT,1210,1%,1/3W,4.99K OHM"

44 4 PANASONIC ERA-6YEB102V "R129, R229, R329, R429" "RES,SMT,2P" "RESISTOR,SMT,0805,1.0K,0.1%,1/10W,25ppm"

45 4 PANASONIC ERA-6YEB104V "R104, R204, R304, R404" "RES,SMT,2P" "RESISTOR,SMT,0805,100K,0.1%,1/10W,25ppm"

46 4 PANASONIC ERA-6YEB392V "R132, R232, R332, R432" "RES,SMT,2P" "RESISTOR,SMT,0805,3.9K,0.1%,1/10W,25ppm"

47 8 CADDOCK MP9100-50.0-1% "R125, R133, R225, R233, R325, R333, R425, R433" "RESISTOR,THU,TO247-2" "RESISTOR,THU,TO247-2,POWER FILM,50.0 OHM,1%,100W"

48 4 NOT INSTALLED RES0805(UN) "R130, R230, R330, R430" "UNINSTALLED RES,SMT,0805" "UNINSTALLED,RESISTOR,SMT, 0805"

49 16 PEM KFS2-M2.5 SITE1-SITE4 PEM NUTS INSTALL FIRST (MANUALLY CALCULATE THE QTY)

50 16 HEAVY METAL 6447013 SITE1-SITE4 "QFN THUMSCREWS, MT9918" (MANUALLY CALCULATE THE QTY)

51 520 TYCO 147444-1 "K_BOOT_S1-K_BOOT_S4, K_CAL1_S1-K_CAL1_S4, K_CAL2_S1-K_CAL2_S4, K_CAL3_S1-K_CAL3_S4, K_CAL4_S1-K_CAL4_S4, K_CBULK_S1-K_CBULK_S4, K_CP2VS_S1-K_CP2VS_S4, K_CP2SRV_S1-K_CP2SRV_S4, K_DIV_S1-K_DIV_S4, K_EN2G_S1-K_EN2G_S4, K_MPUS2PH_S1-K_MPUS2PH_S4," SOCKET PIN - INSTALL 1ST "DIA_038, PIN_013-020, EXP_208, B187"

"K_RT_S1-K_RT_S4, K_SP2BT_S1-K_SP2BT_S4, K_SP2PH_S1-K_SP2PH_S4, K_SRV1X_S1-K_SRV1X_S4, K_SRVCAL_S1-K_SRVCAL_S4, U99, U101, U102, U201, U202, U301, U302, U401, U402"

52 20 MILL-MAX 0355-0-15-01-02-27-10-0 K_MPUF2PH_S1-K_MPUF2PH_S4 SOCKET PIN - INSTALL 1ST "DIA_100, PIN_040-050, EXP_274"

SPECIAL NOTES AND INSTRUCTIONS

1. OK to subsitute Fijitsu FBR51-ND12-W1 for FBR51-ND12-W

"2. If FBR51-ND12-W1 is loose fitting in MIL-MAX 355 socket pin, apply solder to FB51-ND12_W1 socket pins to tighten fit"

END OF BOM

Non-Testable List

SN74AS1034AD
AD8561AN
CAT24C04LI-G
OP27EZ
CASTLE_1.1IN_2COL
KA330/254EEFB21TAH
2506-2-00-50-00-00-07-0
OPC-125-G-D-A
CASTLE_179GHH
SMTPOGO3
1929173
VLCTPOGO8
TSW-107-07-G-S
ADT1-1WT
TEST POINT BLACK
CASTLE_208GGW
69190-403
H1102
ECX-5564-35.328M
CASTLE_324GDW
SN74CB3Q3257DGVR
SN75469D
IRLR8203
HZ_0603_A_102_R
CASTLE_2.4IN_2COL
ADS5410IPFB
1PS74SB43
THS5651AIPW

Pinmap File

REF	PIN	VALUE	Channel Type
P104	C4	NC	No Connection
P104	C5	APU48-55SL	Ground
P104	C6	APU54S	Sense
P104	C7	APU50S	Sense
P104	D1	MPU88FLA	Force Low A

P104	D10	NC	No Connection
P104	D11	NC	No Connection
P104	D12	APU56-63FL	Ground
P104	D13	APU62F	Force
P104	D14	APU58F	Force
P104	D2	MPU88FHA	Force High A
P104	D3	MPUFH88	ETSNC
P104	D4	NC	No Connection
P104	D5	APU48-55FL	Ground
P104	D6	APU54F	Force
P104	D7	APU50F	Force
P104	E1	MPU88FLA	Force Low A
P104	E10	NC	No Connection
P104	E11	BBUS56-63S	ETSNC
P104	E12	NC	No Connection
P104	E13	APU61S	Sense
P104	E14	APU57S	Sense
P104	E2	MPU88FHA	Force High A

Embedded Passive RF Input List

RFR1	D410	50Ohms	L=433.972mils W=20.69mils H=10mils Er=3.9
RFR2	C214	100Ohms	L=456.85mils W=4.85mils H=10mils Er=3.9
RFR3	U303	37.5Ohms	L=400.576mils W=25.961mils H=10mils Er=3.9
RFB1	R439	70.7Ohms	L1=700mils L2=2100mils W1=10.2mils W2=8mils H1=10mils H2=8mils SPL1L2=10mils SP12L1=10mils SPL1=30mils

APPENDIX C

Induce RF Component into Netlist:

```
#:... Induce the RF component in Netlist :
  open(DAT,"test4.txt") || die("ERROR : Could not open RF file!");
  open(TAD,"netlist.txt") || die("ERROR : Could not open RF file!");
  foreach $line (<DAT>)
                {
               chomp($line);
               my @field = split (' ',$line);
               my $Component1_Type    = $field[0]; # Component Type
                              my $Component1_Number  = $field[1]; # Place after this component in netlist
                              my $Component2_Type    = $field[2]; # Component Type
                              my $Component2_Number  = $field[3]; # Place after this component in netlist
                              my $Component3_Type    = $field[4]; # Component Type
                              my $Component3_Number  = $field[5]; # Place after this component in netlist
                              my $Component4_Type    = $field[6]; # Component Type
                              my $Component4_Number  = $field[7]; # Place after this component in netlist
  foreach $line (<TAD>)
                {
               chomp($line);
               my @field = split (' ',$line);
               my $Cmp1_Num    = $field[0]; # Component Number
                              my $Node1_Num   = $field[1]; # Node Number
                              my $Cmp2_Num    = $field[2]; # Component Number
                              my $Node2_Num   = $field[3]; # Node Number
                              my $Cmp3_Num    = $field[4]; # Component Number
                              my $Node3_Num   = $field[5]; # Node Number
                              my $Cmp4_Num    = $field[6]; # Component Number
                              my $Node4_Num   = $field[7]; # Node Number
                              my $Cmp5_Num    = $field[8]; # Component Number
                              my $Node5_Num   = $field[9]; # Node Number
my $Node_Num = "1";
if ($Component1_Number eq $Cmp1_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Cmp2_Num;
    $Node3_Num = $Node2_Num;
    $Cmp2_Num = $Component1_Type;
    $Node2_Num = $Node_Num;
} elsif ($Component1_Number eq $Cmp2_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Component1_Type;
    $Node3_Num = $Node_Num;
} elsif ($Component1_Number eq $Cmp3_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Component1_Type;
    $Node4_Num = $Node_Num;
} elsif ($Component1_Number eq $Cmp4_Num) {
    $Cmp5_Num = $Component1_Type;
    $Node5_Num = $Node_Num;
} elsif ($Component2_Number eq $Cmp1_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Cmp2_Num;
    $Node3_Num = $Node2_Num;
    $Cmp2_Num = $Component2_Type;
```

```
    $Node2_Num = $Node_Num;
} elsif ($Component2_Number eq $Cmp2_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Component2_Type;
    $Node3_Num = $Node_Num;
} elsif ($Component2_Number eq $Cmp3_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Component2_Type;
    $Node4_Num = $Node_Num;
} elsif ($Component2_Number eq $Cmp4_Num) {
    $Cmp5_Num = $Component2_Type;
    $Node5_Num = $Node_Num;
} elsif ($Component3_Number eq $Cmp1_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Cmp2_Num;
    $Node3_Num = $Node2_Num;
    $Cmp2_Num = $Component3_Type;
    $Node2_Num = $Node_Num;
} elsif ($Component3_Number eq $Cmp2_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Component3_Type;
    $Node3_Num = $Node_Num;
} elsif ($Component3_Number eq $Cmp3_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Component3_Type;
    $Node4_Num = $Node_Num;
} elsif ($Component3_Number eq $Cmp4_Num) {
    $Cmp5_Num = $Component3_Type;
    $Node5_Num = $Node_Num;
} elsif ($Component4_Number eq $Cmp1_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Cmp2_Num;
    $Node3_Num = $Node2_Num;
    $Cmp2_Num = $Component4_Type;
    $Node2_Num = $Node_Num;
} elsif ($Component4_Number eq $Cmp2_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Cmp3_Num;
    $Node4_Num = $Node3_Num;
    $Cmp3_Num = $Component4_Type;
    $Node3_Num = $Node_Num;
} elsif ($Component4_Number eq $Cmp3_Num) {
    $Cmp5_Num = $Cmp4_Num;
    $Node5_Num = $Node4_Num;
    $Cmp4_Num = $Component4_Type;
    $Node4_Num = $Node_Num;
} elsif ($Component4_Number eq $Cmp4_Num) {
    $Cmp5_Num = $Component4_Type;
    $Node5_Num = $Node_Num;
}
```

```
   print "$Cmp1_Num\n";
   print "$Node1_Num\n";
   print "$Cmp2_Num\n";
   print "$Node2_Num\n";
   print "$Cmp3_Num\n";
   print "$Node3_Num\n";
   print "$Cmp4_Num\n";
   print "$Node4_Num\n";
   print "$Cmp5_Num\n";
   print "$Node5_Num\n";
}
}
exit 0;
```

Induce RF Component into Parts List:

```
#:... Induce the RF component in Netlist :
 open(DAT,"test3.txt") || die("ERROR : Could not open RF file!");
 open(TAD,"partslist.txt") || die("ERROR : Could not open RF file!");
 foreach $line (<DAT>)
              {
            chomp($line);
            my @field = split (' ',$line);
            my $Component_Type    = $field[0]; # Component Type
 foreach $line (<TAD>)
              {
            chomp($line);
            my @field = split (' ',$line);
            my $Cmp_Typ    = $field[0]; # Model Number
                        my $Cmp_Typ1   = $field[1]; # Model Number
                        my $Cmp1_Num    = $field[2]; # Component Number
                        my $Cmp2_Num   = $field[3]; # Component Number
                        my $Cmp3_Num    = $field[4]; # Component Number
   print "$Cmp_Typ\n";
   print "$Cmp_Typ1\n";
   print "$Cmp1_Num\n";
   print "$Cmp2_Num\n";
   print "$Cmp3_Num\n";
   }
my $Cmp_Typ = "Embedded Passive";
my $Cmp_Typ1 = "Embedded Passive";
$Cmp1_Num = $Component_Type;
print "$Cmp_Typ\n";
print "$Cmp_Typ1\n";
print "$Cmp1_Num\n";
}
exit 0;
```

Fault Dictionary:

```
 #:... Open the Build ciruit module results :
 open(DAT,"test1.txt") || die("ERROR : Could not open BOM file!");
 foreach $line (<DAT>)
              {
            chomp($line);
            my @field = split (' ',$line);
            my $Component_Num    = $field[0]; # Item number field
                        my $Component_Type   = $field[2]; # Number of ref designators by line
                        my $Value            = $field[3]; # Model field
            my $Limit           = $field[4]; # Model field
   my $Resistor = "COMPONENT:R";
   my $Capacitor = "COMPONENT:C";
   my $inductor = "COMPONENT:L";
```

```
    my $Fal_valr = "VALUE:1e+009";
    if ($Component_Type eq $Resistor) {
    $Value = $Fal_valr;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    }
    my $Fal_valc = "VALUE:1e-018";
    if ($Component_Type eq $Capacitor) {
    $Value = $Fal_valc;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    }
    my $Fal_vall = "VALUE:1e+009";
    if ($Component_Type eq $Inductor) {
    $Value = $Fal_vall;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    }
    }
exit 0;
  #:... Open the Build ciruit module results :
  open(DAT,"test1.txt") || die("ERROR : Could not open BOM file!");
  foreach $line (<DAT>)
                {
              chomp($line);
              my @field = split (' ',$line);
              my $Component_Num    = $field[0]; # Item number field
                          my $Component_Type   = $field[2]; # Number of ref designators by line
                          my $Value            = $field[3]; # Model field
              my $Limit            = $field[4]; # Model field
    my $Resistor = "COMPONENT:R";
    my $Capacitor = "COMPONENT:C";
    my $inductor = "COMPONENT:L";
    my $Fal_vall = "VALUE:0.001";
    if ($Component_Type eq $Inductor) {
    $Value = $Fal_vall;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
```

```
    print "$Limit\n";
    }
    my $Fal_valc = "VALUE:1e-006";
    if ($Component_Type eq $Capacitor) {
    $Value = $Fal_valc;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    }
    my $Fal_vall = "VALUE:0.001";
    if ($Component_Type eq $Inductor) {
    $Value = $Fal_vall;
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    } else {
    print "$Component_Num\n";
    print "$Component_Type\n";
    print "$Value\n";
    print "$Limit\n";
    }
    }
exit 0;
#:... Open the Build ciruit module results :
  open(DAT,"test2.txt") || die("ERROR : Could not open BOM file!");
  foreach $line (<DAT>)
                {
              chomp($line);
              my @field = split (' ',$line);
              my $f1   = $field[0]; # Item number field
                          my $f2   = $field[1]; # Number of ref designators by line
                          my $f3   = $field[2]; # Model field
              my $f4   = $field[3]; # Model field
              my $f5   = $field[4]; # Model field
              my $f6   = $field[5]; # Model field
              my $f7   = $field[6]; # Model field
 my $f8   = $field[7]; # Model field
 my $replf = ":[T->1";
 my $newf = ":[T->0";
 my $sa1 = "0";
 my $news1 = "";
 if ($f4 eq $replf) {
    $f4 = $newf;
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
  print "$f7\n";
 } elsif ($f1 eq $sa1) {
    $f1 = $news1;
    $f2 = $news1;
    $f3 = $news1;
    $f4 = $news1;
    $f5 = $news1;
    print "$f1\n";
    print "$f2\n";
```

```
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
print "$f7\n"
}
else {
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
print "$f7\n";
}
}
exit 0;
#:... Open the Build ciruit module results :
  open(DAT,"test2.txt") || die("ERROR : Could not open BOM file!");
  foreach $line (<DAT>)
                {
               chomp($line);
               my @field = split (' ',$line);
               my $f1   = $field[0]; # Item number field
                           my $f2   = $field[1]; # Number of ref designators by line
                           my $f3   = $field[2]; # Model field
               my $f4   = $field[3]; # Model field
               my $f5   = $field[4]; # Model field
               my $f6   = $field[5]; # Model field
               my $f7   = $field[6]; # Model field
my $f8   = $field[7]; # Model field
my $replf = ":[T->0";
my $newf = ":[T->1";
my $sa1 = "1";
my $sa2 = "2";
my $sa3 = "3";
my $news1 = "";
if ($f4 eq $replf) {
    $f4 = $newf;
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
 print "$f7\n";
}
elsif ($f1 eq $sa1) {
    $f1 = $news1;
    $f2 = $news1;
    $f3 = $news1;
    $f4 = $news1;
    $f5 = $news1;
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
print "$f7\n";
}
elsif ($f1 eq $sa2) {
    $f1 = $news1;
    $f2 = $news1;
    $f3 = $news1;
```

```
    $f4 = $news1;
    $f5 = $news1;
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
    print "$f7\n";
}
elsif ($f1 eq $sa3) {
    $f1 = $news1;
    $f2 = $news1;
    $f3 = $news1;
    $f4 = $news1;
    $f5 = $news1;
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
    print "$f7\n";
}
else {
    print "$f1\n";
    print "$f2\n";
    print "$f3\n";
    print "$f4\n";
    print "$f5\n";
    print "$f6\n";
print "$f7\n";
}
}
exit 0;
```

Look-up Table:

```
#:... Open the Pseudocode :
  open(DAT,"pseu.txt") || die("ERROR : Could not open pseudocode file!");
  open(DAT1,"pseuopen.txt") || die("ERROR : Could not open pseudocode file!");
  open(DAT2,"pseushort.txt") || die("ERROR : Could not open pseudocode file!");
  open OUTPUT, ">output.txt";
  print OUTPUT "Part_Num    Fault Type     Lo Limit    Up Limit    Actual Value\n";
  foreach $line (<DAT>)
                {
              chomp($line);
              my @field = split (' ',$line);
              my $Component_Num    = $field[0]; # Item number field
                          my $Component_Type   = $field[2]; # Number of ref designators by line
                          my $Value            = $field[3]; # Model field
              my $Limit            = $field[4]; # Model field
              my $Value1     = $field[8]; # Upper Limit
              my $Limit1     = $field[9]; # Upper Limit
              my $Value2     = $field[13]; # Upper Limit
              my $Limit2     = $field[14]; # Upper Limit
              my $passcomp         = $field[17]; # Passive Component
              my $pascmpval        = $field[22]; # Passive Component Value
    my $Comp_Typ = "CONDITION(VERIFY";
    my $Comp_Lim = "COMPARE_LIMITS(lower";
    my $Part_Num = "";
    my $Fault_Type = "Fault Free";
    my $SMDC1 = "*****SMA";
    my $SMDC2 = "*****DIRECT";
```

```
my $test = "tested";
my $Part_Num = "";
if ($Component_Num eq $SMDC1) {
$Part_Num = "SMA      ";
print OUTPUT "$Part_Num";
} elsif ($Component_Num eq $SMDC2) {
$Part_Num = "DirConnec";
print OUTPUT "$Part_Num";
} elsif (($Limit2 eq $test) && ($Component_Num eq $Comp_Lim)) {
$Part_Num = $passcomp;
print OUTPUT "$Part_Num";
print OUTPUT "      $Fault_Type     $Value$Limit      $Value1$Limit1      $pascmpval\n";
} elsif ($Component_Num eq $Comp_Typ) {
$Part_Num = $Value;
print OUTPUT "$Part_Num";
} elsif ($Component_Num eq $Comp_Lim) {
print OUTPUT "   $Fault_Type     $Value$Limit      $Value1$Limit1      $Value2$Limit2\n";
}
}
foreach $line (<DAT1>)
          {
          chomp($line);
          my @field1 = split (' ',$line);
          my $Component_Num1    = $field1[0]; # Item number field
                    my $Component_Type1   = $field1[2]; # Number of ref designators by line
                    my $Value1            = $field1[3]; # Model field
          my $Limit1            = $field1[4]; # Model field
          my $Value11                   = $field1[8]; # Upper Limit
          my $Limit11                   = $field1[9]; # Upper Limit
          my $Value21                   = $field1[13]; # Upper Limit
          my $Limit21                   = $field1[14]; # Upper Limit
          my $passcomp1         = $field1[17]; # Passive Component
          my $pascmpval1        = $field1[22]; # Passive Component Value
my $Comp_Typ1 = "CONDITION(VERIFY";
my $Comp_Lim1 = "COMPARE_LIMITS(lower";
my $Part_Num1 = "";
my $Fault_Type1 = "Open Fault";
my $test1 = "tested";
my $Part_Num1 = "";
if (($Limit21 eq $test1) && ($Component_Num1 eq $Comp_Lim1)) {
$Part_Num1 = $passcomp1;
print OUTPUT "$Part_Num1";
print OUTPUT "      $Fault_Type1      $Value1$Limit1      $Value11$Limit11      $pascmpval1\n";
} elsif ($Component_Num1 eq $Comp_Typ1) {
$Part_Num1 = $Value1;
print OUTPUT "$Part_Num1";
} elsif ($Component_Num1 eq $Comp_Lim1) {
print OUTPUT "   $Fault_Type1      $Value1$Limit1      $Value11$Limit11      $Value21$Limit21\n";
}
}
foreach $line (<DAT2>)
          {
          chomp($line);
          my @field = split (' ',$line);
          my $Component_Num     = $field[0]; # Item number field
                    my $Component_Type    = $field[2]; # Number of ref designators by line
                    my $Value             = $field[3]; # Model field
          my $Limit             = $field[4]; # Model field
          my $Value1      = $field[8]; # Upper Limit
          my $Limit1      = $field[9]; # Upper Limit
          my $Value2      = $field[13]; # Upper Limit
          my $Limit2      = $field[14]; # Upper Limit
          my $passcomp          = $field[17]; # Passive Component
          my $pascmpval         = $field[22]; # Passive Component Value
my $Comp_Typ = "CONDITION(VERIFY";
```

```
    my $Comp_Lim = "COMPARE_LIMITS(lower";
    my $Part_Num = "";
    my $Fault_Type = "Short Fault";
    my $SMDC1 = "*****SMA";
    my $SMDC2 = "*****DIRECT";
    my $test = "tested";
    my $Part_Num = "";
    if ($Component_Num eq $SMDC1) {
    $Part_Num = "SMA      ";
    print OUTPUT "$Part_Num";
    } elsif ($Component_Num eq $SMDC2) {
    $Part_Num = "DirConnec";
    print OUTPUT "$Part_Num";
    } elsif (($Limit2 eq $test) && ($Component_Num eq $Comp_Lim)) {
    $Part_Num = $passcomp;
    print OUTPUT "$Part_Num";
    print OUTPUT "      $Fault_Type     $Value$Limit      $Value1$Limit1      $pascmpval\n";
    } elsif ($Component_Num eq $Comp_Typ) {
    $Part_Num = $Value;
    print OUTPUT "$Part_Num";
    } elsif ($Component_Num eq $Comp_Lim) {
    print OUTPUT "   $Fault_Type     $Value$Limit      $Value1$Limit1      $Value2$Limit2\n";
    }
    }
exit 0;
```

APPENDIX D

HV-DIB Input Files:

PARTS LIST

08051C104KAZ2A 08051C104KAZ2A C311 C112 C411
08051C104KAZ2A 08051C104KAZ2A C111 C412 C408
08051C104KAZ2A 08051C104KAZ2A C312 C208 C109
08051C104KAZ2A 08051C104KAZ2A C209 C409 C308
08051C104KAZ2A 08051C104KAZ2A C211 C212 C309
08051C104KAZ2A 08051C104KAZ2A C108

08053C104JAT2A(UN)08053C104JAT2A(UN)C203 C304 C404
08053C104JAT2A(UN)08053C104JAT2A(UN)C103 C403 C201
08053C104JAT2A(UN)08053C104JAT2A(UN)C204 C205 C405
08053C104JAT2A(UN)08053C104JAT2A(UN)C401 C301 C105
08053C104JAT2A(UN)08053C104JAT2A(UN)C305 C104 C101
08053C104JAT2A(UN)08053C104JAT2A(UN)C303

104-1-A-12/2D 104-1-A-12/2D K420A K421A K420B
104-1-A-12/2D 104-1-A-12/2D K421B K422B K418A
104-1-A-12/2D 104-1-A-12/2D K418B K417 K419B
104-1-A-12/2D 104-1-A-12/2D K319B K419A K319A
104-1-A-12/2D 104-1-A-12/2D K202 K322A K320A
104-1-A-12/2D 104-1-A-12/2D K317 K320B K422A
104-1-A-12/2D 104-1-A-12/2D K321B K322B K318A
104-1-A-12/2D 104-1-A-12/2D K118A K318B K302
104-1-A-12/2D 104-1-A-12/2D K321A K417 K102
104-1-A-12/2D 104-1-A-12/2D K318B K319A K319B
104-1-A-12/2D 104-1-A-12/2D K320A K320B K321A
104-1-A-12/2D 104-1-A-12/2D K321B K322A K317
104-1-A-12/2D 104-1-A-12/2D K402 K302 K418A
104-1-A-12/2D 104-1-A-12/2D K418B K419A K419B
104-1-A-12/2D 104-1-A-12/2D K420A K420B K421A
104-1-A-12/2D 104-1-A-12/2D K421B K422A K422B
104-1-A-12/2D 104-1-A-12/2D K322B K122B K217
104-1-A-12/2D 104-1-A-12/2D K117 K221A K118B
104-1-A-12/2D 104-1-A-12/2D K119A K119B K120A
104-1-A-12/2D 104-1-A-12/2D K120B K121A K318A
104-1-A-12/2D 104-1-A-12/2D K122A K402 K202
104-1-A-12/2D 104-1-A-12/2D K217 K218A K218B
104-1-A-12/2D 104-1-A-12/2D K219A K219B K220A
104-1-A-12/2D 104-1-A-12/2D K220B K221B K222B
104-1-A-12/2D 104-1-A-12/2D K121B K119A K121B
104-1-A-12/2D 104-1-A-12/2D K219A K122B K118A
104-1-A-12/2D 104-1-A-12/2D K118B K222A K102
104-1-A-12/2D 104-1-A-12/2D K219B K117 K220A
104-1-A-12/2D 104-1-A-12/2D K221A K218B K120A
104-1-A-12/2D 104-1-A-12/2D K121A K220B K119B
104-1-A-12/2D 104-1-A-12/2D K120B K122A K218A
104-1-A-12/2D 104-1-A-12/2D K222B K221B K222A

CRCW08051001F CRCW08051001F R320 R321 R420
CRCW08051001F CRCW08051001F R233 R138 R238
CRCW08051001F CRCW08051001F R237 R236 R235
CRCW08051001F CRCW08051001F R234 R327 R428
CRCW08051001F CRCW08051001F R433 R434 R435
CRCW08051001F CRCW08051001F R436 R437 R322
CRCW08051001F CRCW08051001F R323 R438 R338
CRCW08051001F CRCW08051001F R324 R325 R300
CRCW08051001F CRCW08051001F R100 R421 R328
CRCW08051001F CRCW08051001F R333 R427 R426
CRCW08051001F CRCW08051001F R425 R424 R423
CRCW08051001F CRCW08051001F R422 R334 R335

CRCW08051001F CRCW08051001F R336 R337 R400
CRCW08051001F CRCW08051001F R326 R122 R133
CRCW08051001F CRCW08051001F R128 R127 R126
CRCW08051001F CRCW08051001F R125 R134 R123
CRCW08051001F CRCW08051001F R139 R121 R120
CRCW08051001F CRCW08051001F R200 R228 R239
CRCW08051001F CRCW08051001F R439 R124 R222
CRCW08051001F CRCW08051001F R135 R339 R227
CRCW08051001F CRCW08051001F R226 R223 R221
CRCW08051001F CRCW08051001F R220 R224 R225
CRCW08051001F CRCW08051001F R136 R137

CRCW08051002F CRCW08051002F R410 R110 R103
CRCW08051002F CRCW08051002F R210 R403 R310
CRCW08051002F CRCW08051002F R303 R203

CRCW12060000F CRCW12060000F R417 R317 R416
CRCW12060000F CRCW12060000F R216 R316 R1
CRCW12060000F CRCW12060000F R117 R116 R217

CRCW12062211F CRCW12062211F R99 R98

CRCW20102490F CRCW20102490F R92

CRCW20106040F CRCW20106040F R91 R2

CRCW20107500F CRCW20107500F R93 R90

ERJ-6ENF49R9V ERJ-6ENF49R9V R411 R413 R404
ERJ-6ENF49R9V ERJ-6ENF49R9V R406 R105 R312
ERJ-6ENF49R9V ERJ-6ENF49R9V R305 R306 R204
ERJ-6ENF49R9V ERJ-6ENF49R9V R304 R206 R313
ERJ-6ENF49R9V ERJ-6ENF49R9V R112 R213 R412
ERJ-6ENF49R9V ERJ-6ENF49R9V R212 R311 R106
ERJ-6ENF49R9V ERJ-6ENF49R9V R405 R104 R205
ERJ-6ENF49R9V ERJ-6ENF49R9V R211 R111 R113

ETS600-POGO_143P ETS600-POGO_143P P203 P206 P203
ETS600-POGO_143P ETS600-POGO_143P P206 P203 P206
NET LIST

NODENAME 12V $
K102 3 C220 1 K228B 3 R91 1 $
P103 B5 P106 B5 R136 2 $
K228A 3 P114 B5 K49 3 $
K223B 3 P111 B5 R439 2 $
K223A 3 K229A 3 R339 2 $
R139 2 R220 2 C120 1 $
K56 3 K230A 3 C420 1 $
K229B 3 C320 1 C91 1 $
R239 2 K230B 3 K202 3 $
R320 2 R234 2 R235 2 $
K53 3 K44 3 R236 2 $
R120 2 K225 3 K326A 3 $
K323B 3 R322 2 K330B 3 $
K330A 3 K329B 3 K329A 3 $
K328B 3 K328A 3 K327B 3 $
K327A 3 K60 3 K323A 3 $
K218A 3 K57 3 K218B 3 $
K45 3 K129B 3 R333 2 $
R328 2 K130A 3 R228 2 $
R327 2 R321 2 R233 2 $
K123A 3 R326 2 K130B 3 $
R325 2 K41 3 R324 2 $
K123B 3 R323 2 K217 3 $

K322B 3 K61 3 R125 2 $
K62 3 K58 3 K54 3 $
R237 2 R334 2 R138 2 $
R122 2 R123 2 K326B 3 $
R124 2 K59 3 R126 2 $
R127 2 R128 2 R133 2 $
R134 2 R2 1 R135 2 $
K48 3 K52 3 R238 2 $
K317 3 K322A 3 K321B 3 $
K321A 3 K320B 3 K320A 3 $
K319B 3 K319A 3 K318B 3 $
K40 3 K51 3 K318A 3 $
K55 3 R121 2 K325 3 $
K302 3 K47 3 K43 3 $
K46 3 K42 3 K63 3 $
R335 2 R137 2 K221B 3 $
R424 2 R423 2 R422 2 $
R421 2 K50 3 R420 2 $
K222A 3 K125 3 R227 2 $
K118A 3 R426 2 K118B 3 $
K423A 3 K423B 3 K430B 3 $
K430A 3 K429B 3 K429A 3 $
K428B 3 K428A 3 K117 3 $
R437 2 K227B 3 R338 2 $
K227A 3 R222 2 K226B 3 $
R438 2 K226A 3 R223 2 $
K64 2 R226 2 K222B 3 $
R425 2 R436 2 R435 2 $
R224 2 R434 2 R433 2 $
R225 2 R428 2 R427 2 $
K427B 3 D2 1 K126B 3 $
K402 3 K119A 3 K119B 3 $
K120A 3 K120B 3 K121A 3 $
K121B 3 K122A 3 K417 3 $
K126A 3 K418A 3 K127A 3 $
K127B 3 K128A 3 R337 2 $
K128B 3 R336 2 K219B 3 $
K129A 3 R221 2 K122B 3 $
K421A 3 K426A 3 K422A 3 $
K425 3 K426B 3 K221A 3 $
K220A 3 K422B 3 K220B 3 $
K421B 3 K420B 3 K420A 3 $
K419B 3 K419A 3 K219A 3 $
K418B 3 K427A 3
NODENAME 15V $
U202 7 C111 2 U102 7 C108 2 $
U101 7 C208 2 C211 2 $
P103 F2 R90 1 C311 2 $
U201 7 C411 2 C90 1 $
U402 7 P103 G4 P103 G3 $
U301 7 U302 7 U401 7 $
P103 F3 C408 2 C308 2

BILL OF MATERIALS

"ETS-364,HIB,SN27700,QUAD SITE, 16PIN"

6553443

A5

2126224

ITEM QTY VALUE or FUNCTION REF DES MFG PART# DESCRIPTION

REF	-	-	6553443A ASSEMBLY
REF	-	-	6553443A SCHEMATIC
1	-	-	6553443A FABRICATION
REF	-	-	6553443A ARTWORK

1	1			6437988	"HARDWARE KIT, EAGLE ETS-364/ETS-600 HIB"			
2	16	"CAPACITOR,SMT,0805,CERAMIC,0.1uF,100V,10%"	"C108, C109, C111, C112, C208, C209, C211, C212, C308, C309, C311, C312, C408, C409, C411, C412"	08051C104KAZ2A	"CAP,SMT,0805"			
3	16	(Uninstalled Part)	"C101, C103, C104, C105, C201, C203, C204, C205, C301, C303, C304, C305, C401, C403, C404, C405"	08053C104JAT2A(UN)	"CAP,SMT,0805"			
4	24	"CAPACITOR,SMT,1206,CERAMIC,0.001uF,100V,5%"	"C110, C113, C114, C115, C116, C117, C210, C213, C214, C215, C216, C217, C310, C313, C314, C315, C316, C317, C410, C413, C414, C415, C416, C417"	12061C102JATMA	"CAP,SMT,1206"			
5	4	"CAPACITOR,SMT,1206,CERAMIC,1uF,25V,-20~+80%"	"C102, C202, C302, C402"	12063G105ZATRA	"CAP,SMT,1206"			
6	4	"CAP,SMT,TAN,2.2uF,50V,10%,ESR-2.5ohm@100K"	"C94, C95, C96, C97"	T491D225K050AS	"CAP,SMT,TAN,CASE-D"			
7	4	"CAPACITOR,THRU,2P,ELECTROLYTIC,16V,20%,10uF"	"C120, C220, C320, C420"	2222	123	15109	"CAPACITOR,AXL,ELECTRO"	
8	4	"CAPACITOR,THRU,2P,TANTALUM,2.2uF,35V,10%"	"C90, C91, C92, C93"	199D225X9035BA1	"CAPACITOR,RAD,TANTALUM"			
9	1	"CAPACITOR,THRU,2P,TANTALUM,0.1uF,50V,10%"	C99	199D104X9050AA1	"CAPACITOR,THRU,2P"			
10	1	MICRO B USB RECEPTACLE R/A SMT TYPE	J1	UUSB-B-S-S-SM-TR	"CONN,SMT,5P"			
11	2	SOLDER WITH FLANGE FLUSH AGAINST DUT SIDE	"B1, B2"	20054	"CONN,THRU,1P"			
12	4	CUSTOMER INSTALL	"SITE1, SITE2, SITE3, SITE4"	KEX04_SSOP300_1.27_28_DW	CUSTOMER INSTALL			
13	1	"DIODE SMALL SIGNAL, SMT, SOD-323"	D2	1N4148WS	"DIODE, SMT,SOD323-2"			
14	8	SCHOTTKEY DIODE	"D100, D101, D200, D201, D300, D301, D400, D401"	1N5711WS	"DIODE,SMT,2P"			
15	8	"400W POWER ZENER TRANSIENT VOLTAGE SUPPRESSOR, 15V"	"D166, D167, D266, D267, D366, D367, D466, D467"	1SMA15CAT3	"DIODE,SMT,SMA-2"			
16	100	"600W TRANSIENT VOLTAGE SUPPRESSOR,BI-DIR,12V"	"D110, D115, D116, D117, D118, D119, D120, D121, D122, D123, D124, D125, D130, D131, D132, D133, D134, D135, D136, D137, D138, D139, D140, D141, D142, D210, D215, D216, D217, D218, D219, D220, D221, D222, D223, D224, D225, D230, D231, D232, D233, D234,"	SMBJ12CA	"DIODE,SMT,SMB"			
			"D235, D236, D237, D238, D239, D240, D241, D242, D310, D315, D316, D317, D318, D319, D320, D321, D322, D323, D324, D325, D330, D331, D332, D333, D334, D335, D336, D337, D338, D339, D340, D341, D342, D410, D415, D416, D417, D418, D419, D420, D421, D422,"					
			"D423, D424, D425, D430, D431, D432, D433, D434, D435, D436, D437, D438, D439, D440, D441, D442"					

17 9 "600W TRANSIENT VOLTAGE SUPPRESSOR,BI-DIR,100V,5%" "D4, D164, D165, D264, D265, D364, D365, D464, D465" SMBJ100CA "DIODE,SMT,SMB-J"

18 8 "250mA,HS_BUFFER,SMT" "U101, U102, U201, U202, U301, U302, U401, U402" BUF634U "IC,SMT,SOIC-8"

19 1 "4-Kb CMOS SERIAL EEPROM,1.8~5.5V,DIP-8,NiPdAu" U99 CAT24C04LI-G "IC,THU,DIP-8"

20 4 INSTALLED JUMPER 0805 FOOTPRINT "J100, J200, J300, J400" JUMPER-0805 "JUMPER,SMT0805"

21 1 ASSEMBLE WITH LED INSIDE HOLE D1 HSMC-C265 "LED,SMT"

22 4 "GREEN,SMT,20mA" "D90, D91, D92, D93" SML-LX1206GC-TR "LED,SMT"

23 64 "RELAY,SMT,4P,SSR,PhotoMOS,SSOP-4,SPST-NO,40V,300mA,RSD1.0R" "K100, K101, K103, K104, K112, K113, K114, K131, K132, K133, K200, K201, K203, K204, K212, K213, K214, K231, K232, K233, K300, K301, K303, K304, K312, K313, K314, K331, K332, K333, K400, K401, K403, K404, K412, K413, K414, K431, K432, K433, K105A, K105B," G3VM-41LR5 "RELAY,SMT,SSOP-4"

"K106A, K106B, K107A, K107B, K205A, K205B, K206A, K206B, K207A, K207B, K305A, K305B, K306A, K306B, K307A, K307B, K405A, K405B, K406A, K406B, K407A, K407B"

24 48 "RELAY,THRU,4P,RR,SPST,1FA,N0,12V,1.0A,1K5 COIL,DIODE,10W" "K102, K117, K202, K217, K302, K317, K402, K417, K118A, K118B, K119A, K119B, K120A, K120B, K121A, K121B, K122A, K122B, K218A, K218B, K219A, K219B, K220A, K220B, K221A, K221B, K222A, K222B, K318A, K318B, K319A, K319B, K320A, K320B, K321A, K321B, K322A," 104-1-A-12/2D "RELAY,THRU,4P"

"K322B, K418A, K418B, K419A, K419B, K420A, K420B, K421A, K421B, K422A, K422B"

25 76 "RELAY,THRU,6P,RR,DPST,2FA,12V,0.5A,10W,750R COIL,DIODE" "K40, K41, K42, K43, K44, K45, K46, K47, K48, K49, K50, K51, K52, K53, K54, K55, K56, K57, K58, K59, K60, K61, K62, K63, K125, K225, K325, K425, K123A, K123B, K126A, K126B, K127A, K127B, K128A, K128B, K129A, K129B, K130A, K130B, K223A, K223B, K226A," 104-2-A-12/2D "RELAY,THRU,6P"

"K226B, K227A, K227B, K228A, K228B, K229A, K229B, K230A, K230B, K323A, K323B, K326A, K326B, K327A, K327B, K328A, K328B, K329A, K329B, K330A, K330B, K423A, K423B, K426A, K426B, K427A, K427B, K428A, K428B, K429A, K429B, K430A, K430B"

26 1 "3PST,3FA,0.5A,12V,1K OHM COIL,NON SHIELD" K64 2333-12-000 "RELAY,THRU,8P"

27 68 "RESISTER,SMT,0805,THICK FILM,1%,1/8W,1.00K" "R100, R120, R121, R122, R123, R124, R125, R126, R127, R128, R133, R134, R135, R136, R137, R138, R139, R200, R220, R221, R222, R223, R224, R225, R226, R227, R228, R233, R234, R235, R236, R237, R238, R239, R300, R320, R321, R322, R323, R324, R325, R326," CRCW08051001F "RES,SMT,0805"

"R327, R328, R333, R334, R335, R336, R337, R338, R339, R400, R420, R421, R422, R423, R424, R425, R426, R427, R428, R433, R434, R435, R436, R437, R438, R439"

28 8 "RESISTOR,SMT,0805,THICK FILM,1%,1/8W,10.0K" "R103, R110, R203, R210, R303, R310, R403, R410" CRCW08051002F "RES,SMT,0805"

29 24 "RESISTOR,SMT,0805,THICK FILM,1%,1/8W, 49.9 OHM" "R104, R105, R106, R111, R112, R113, R204, R205, R206, R211, R212, R213, R304, R305, R306, R311, R312, R313, R404, R405, R406, R411, R412, R413" ERJ-6ENF49R9V "RES,SMT,0805"

30 9 "RESISTOR,SMT,1206,0 OHM,1%,1/4W (Same as CRCW12060000F)" "R1, R116, R117, R216, R217, R316, R317, R416, R417" CRCW12060000F "RES,SMT,1206"

31 2 "RESISTOR,SMT,1206,1%,1/4W,2.21K" "R98, R99" CRCW12062211F "RES,SMT,1206"

32 1 "RESISTOR,SMT,2010,THICK FILM,1%,3/4W,249 OHM" R92 CRCW20102490F "RES,SMT,2010"

33 2 "RESISTOR,SMT,2010,THICK FILM,1%,3/4W,604 OHM" "R2, R91" CRCW20106040F "RES,SMT,2010"

34 2 "RESISTOR,SMT,2010,THICK FILM,1%,3/4W,750 OHM" "R90, R93" CRCW20107500F "RES,SMT,2010"

35 12 "RESISTOR,SMT,2P,THICK FILM,1M,HV,1W,1%,RoHS" "R101, R102, R109, R201, R202, R209, R301, R302, R309, R401, R402, R409" MC102821004JE "RES,SMT,2P"

36 1 "RESISTOR,SMT,2P,THICK FILM,10M,HV,1W,1%,RoHS" R3 MC102821005JE "RES,SMT,2P"

37 44 "400W POWER ZENER TRANSIENT VOLTAGE SUPPRESSOR, 28V" "D152, D153, D155, D156, D159, D160, D161, D162, D163, D168, D169, D252, D253, D255, D256, D259, D260, D261, D262, D263, D268, D269, D352, D353, D355, D356, D359, D360, D361, D362, D363, D368, D369, D452, D453, D455, D456, D459, D460, D461, D462, D463," 1SMA28CAT3 "ZENER DIODE,SMT,SMA"

"D468, D469"

38 16 INSTALL FIRST (MANUALLY CALCULATE THE QTY) SITE1-SITE4 KFS2-M2.5 PEM NUTS

39 16 (MANUALLY CALCULATE THE QTY) SITE1-SITE4 4152296 "DIL THUMBSCREWS, MT9918"

40 16 "DIA_038, PIN_013-020, EXP_208, B187" "K64, U99" 147444-1 SOCKET PIN - INSTALL 1ST

41 76 "K40-K63, K123A, K123B, K125, K126B, K126A, K127B, K127A, K128B, K128A, K129B, K129A, K130B, K130A, K223B, K223A, K225, K226A, K226B, K227A, K227B, K228A, K228B, K229A, K229B, K230A, K230B, K323A, K323B, K325, K326A, K326B, K327A, K327B, K328B, K328A," S890-93-006-30-25220 SMT/THRU RELAY FOR HIGH VOLTAGE APP

"K329B, K329A, K330A, K330B, K423A, K423B, K425, K426A, K426B, K427A, K427B, K428A, K428B, K429A, K429B, K430A, K430B"

42 48 104-1-A-12/2D "K102, K117, K118A, K118B, K119A, K119B, K120A, K120B, K121A, K121B, K122A, K122B, K202, K217, K218A, K218B, K219A, K219B, K220A, K220B, K221A, K221B, K222A, K222B, K302, K317, K318A, K318B, K319A, K319B, K320A, K320B, K321A, K321B, K322A, K322B, K402," S890-93-004-30-250200 SMT RELAY RECEPTACLE

"K417, K418A, K418B, K419A, K419B, K420A, K420B, K421A, K421B, K422A, K422B"

END OF BOM