DESIGN AND SELF-CALIBRATION SCHEME FOR RF CIRCUITS USING MEMS IN 3D PACKAGES

by

NAGA SAI SHRAVAN EVANA

A THESIS

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ABSTRACT

This thesis presents a novel on-chip testing and self-calibration methodology of a 5 GHz Low Noise Amplifier (LNA) with micro electro-mechanical switches (MEMS) using three dimensional (3D) through-silicon via (TSV) packaging technology. The LNA can self-calibrate its gain and noise figure (NF). On-chip testing is performed using a peak detector and a digital signal processor (DSP). A low-cost self-calibration scheme is proposed which utilizes a tuning circuit consisting of an inductor and capacitor bank and a MEMS switch matrix. The MEMS switch matrix and the analog circuitry are fabricated on two separate dies and stacked using TSV.

With increasing demand for integrating analog, digital and RF circuits on a single chip, 3D packaging is the best way to realize this. The utilization of 3D-TSV technology in this work optimized the usage of real estate without compromising on the signal integrity of the complete circuit. MEMS switches provided high isolation and lesser parasitic effects than conventional transistor based switches. Most of the parametric variations within the LNA were identified by the testing circuit. The self-calibration circuit is capable of correcting these variations. The testing and self-calibration circuits successfully accomplished the task of keeping the gain of the LNA > 8 dB, noise figure < 2 dB and stability factor > 1.

LIST OF ABBREVIATIONS AND SYMBOLS

RF	Radio Frequency
DUT	Device Under Test
LNA	Low Noise Amplifier
NF	Noise Figure
SF	Stability Factor
MEMS	Micro Electro Mechanical System
TSV	Through Silicon Via
SNR	System to Noise Ratio
DSP	Digital Signal Processor
ADC	Analog-to-Digital convertor
LUT	Look-Up Table
ADS	Advanced Design System
VLCT	Very Low Cost Tester
SoC	System on Chip
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

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CHAPTER 1

INTRODUCTION

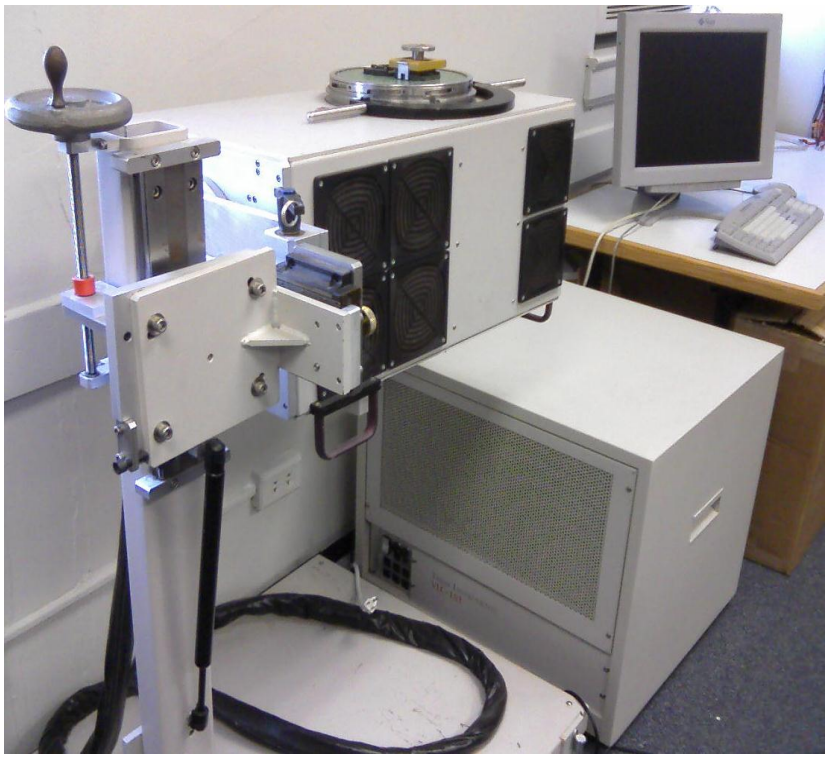
Modern day communication systems require the presence of the complete radio frequency (RF) system on a single chip. CMOS technology is widely considered to be the best option to meet this demand. Designing the RF system based on CMOS technology has the advantage of providing high level of functionality at low cost on the same chip. However, as the CMOS technology shrinks to nanometer dimensions, the sensitivity of process variations causes degradation in the performance of the RF circuit. This makes the design of sensitive RF circuits extremely difficult. Also, the extraction of parasitics of the passive devices becomes increasingly difficult due to the higher operating frequencies and smaller interconnects spacing. These problems lead to a significant loss in parametric yield. Hence, testing the fabricated chip for process variations is very essential.

Current Chip Testing Techniques

Testing of chips is an important aspect of the IC production cycle and comes in line after the design and fabrications stages. It occupies a major fraction of the total cost and time involved in producing the chips. In order to test the chips, specialized equipment called Automatic Test Equipment (ATE) is used. Several tests like the continuity test, the leakage test, etc. are run on the chip to validate its performance. Test programs are written and executed on a PC workstation

which is interfaced to the actual tester by a controller. The controller, in accordance with the written program, activates the respective circuits in the tester head to commence the testing process.

Figure 1. Texas Instruments' VLCT



Before commencing the testing process, a certain tolerance window is defined for the parameters of the device-under-test (DUT). This window defines the acceptable percentage of offset from the ideal operating point; also known as the fault tolerance window. If after testing the parameters are found to be outside this range, then the chip is termed as defective and discarded; else, it is accepted as defect-free. For example, if a tolerance of + or – 10% is defined for the DUT and the parametric yield is found to be at 11%, then the chip is discarded, whereas if the yield is at 9%, the chip is accepted.

But discarding the chip that is in the vicinity of the fault tolerance window might not be a feasible idea. From the above mentioned example, if we discard a chip that is 11% faulty along with one that is 40% faulty, that is not a cost-effective idea. Hence, there is need for a technique to detect and correct these defects and get the chip in to the fault tolerance window.

After testing, however, it is not guaranteed that the chip will remain within the defined tolerance limit forever. Once the chip is implanted into the device, with an increase in time and usage, there is a good probability for component variations to occur within the chip (David Orenstein, 2008). The factors that drive these variations are thermal fatigue, mechanical shock, self-heating, electromigration, etc. At this point, recalling the chips to the company for testing is not a feasible idea. There is a necessity for the process of being able to detect the component variations within the device and automatically self-calibrate it back into its acceptable tolerance window. A self-calibration methodology that can cater to both process variations and time-degraded variations is proposed in this thesis.

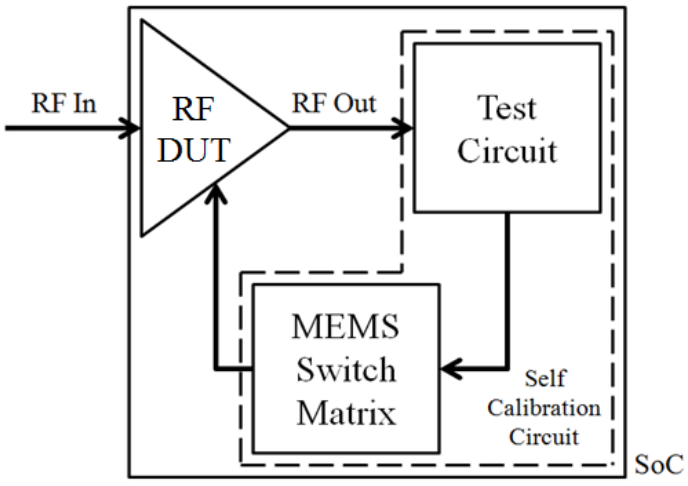
Proposed Chip Testing Idea

After the testing stage, faulty chips are either debugged and re-processed to nullify the defects or discarded depending on the level of the defects (P. Chiang, 2007). This process takes a lot of time and effort and requires specialized equipment to precisely correct the faults on the chip. Several on-chip techniques to detect and correct the defects have been previously proposed (S. Cherubal, 2004) but they utilize complex hardware external to the chip and are not cost-effective. Hence, there is a need for testing and on-chip calibration methodologies which are not only simple and inexpensive, but also accurate enough.

The most ideal way to achieve this would be to design the RF, testing and self-calibration circuits on the same chip. In order to reduce the chip area used to accommodate the circuitry and to eradicate the complexity of fabricating multiple technologies on a single silicon substrate, designing them on different dies and stacking these dies together in a three dimensional (3D) manner would be ideal. If a digital circuit and an RF circuit are to be designed on the same substrate, it requires complicated fabrication processes and additional hardware. Use of the through silicon via (TSV) technology for stacking of dies is more convenient and optimal because it allows dies fabricated on different technologies to be interconnected without compromising on signal and power integrity of the chip. TSV technology is highly advantageous in comparison to the conventional wire bond technology in this regard.

The block diagram of the complete system-on-chip (SoC) architecture is shown in Figure 2.

Figure 2. System-on-Chip Architecture of the test and self-calibration circuitry.



The reference RF circuit chosen in this thesis is a low noise amplifier (LNA).

Thesis Outline

This thesis is organized as follows: Chapter 2 talks about the design of the low noise amplifier. This chapter gives a brief introduction about the different parameters of the LNA and mentions the specifications of the designed LNA. Chapter 3 gives details of the proposed test methodology. It talks about the peak detector and how it is used to perform testing. Chapter 4 elaborates on the proposed self-calibration methodology by detailing on the tuning circuit and the MEMS switch. Chapter 5 gives insight into the proposed packaging solution of the complete test and self-calibration setup with the LNA using TSV. Chapter 6 discusses the results and effectiveness of the proposed schemes. Chapter 7 gives an overall summary of the work with conclusion and future work.

CHAPTER 2

LOW NOISE AMPLIFIER

Introduction

Among the most important blocks of an RF receiver front-end like mixer, band pass filter (BPF), etc. lays the low noise amplifier (LNA). An LNA is generally the first stage of the RF receiver system. Its performance is crucial to the complete system considering the fact that it amplifies the received low power signal to just the amount required to be given to the next stage. Ideally an LNA is supposed to suppress all of the externally acquired noise and amplify the signal. In practical terms, however, the LNA reduces the received signal noise by a considerable amount and in the pursuit adds its own noise to the signal (M. Edwall, 2008). Hence, the design of the LNA is very important and requires a painstaking effort.

The requirements of the ideal LNA are high gain, low noise, stability, high linearity, perfect input-output match and low power consumption. Impedance matching is one of the most important considerations of the design of an LNA. The input reflection coefficient (S_{11}) determines the input match. S_{11} is crucial as it also relates to the forward gain (S_{21}) of the LNA. Parametric variations sometimes cause a shift in the operating frequency of the LNA and this

leads to a change in S_{11} and S_{21} parameters (R. M. Ayadi, 2010). This causes an impedance mismatch between the LNA and the following stages leading to signal attenuation.

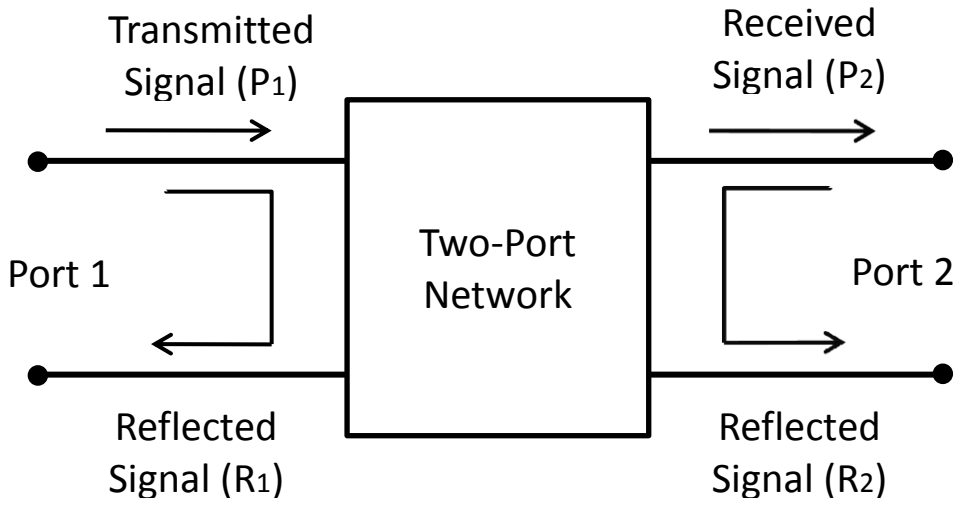
To avoid the above mentioned problems, it is desirable to detect deviations from the LNA's optimal performance using on-chip testing techniques and tune it back close to its optimal operating point using self-calibration schemes.

Scattering Parameters

The performance of the LNA can be analyzed by calculating its scattering parameters (S-Parameters). Important parameters like gain, stability factor and input and output match can be derived from its S-parameters. S-parameters are generally measured in dB.

For a two-port network, S-parameters are defined as follows.

Figure 3. Two-Port Network.



Signal power transmitted from port 1 to port 2 is represented by S_{12} and is given by,

$$S_{12} = \frac{P_2}{P_1} \qquad (1)$$

S_{12} is also called as the reverse transducer power gain.

Signal power reflected back to port 1 is represented by S_{11} and is given by

$$S_{11} = \frac{R_1}{P_1} \qquad (2)$$

S_{11} is also called as the input reflection coefficient.

Signal power transmitted from port 2 to port 1 is represented by S_{21} and is given by,

$$S_{21} = \frac{P_1}{P_2} \qquad (3)$$

S_{21} is also called as the forward transducer power gain.

Signal power reflected back to port 2 is represented by S_{22} and is given by,

$$S_{22} = \frac{R_2}{P_2} \qquad (4)$$

S_{22} is also called as the output reflection coefficient.

Gain

The gain of the LNA is its ability to amplify the power of the input signal (T. H. Lee, 1998). It is given by the ratio of power of the output signal to that of the input signal and is measured in decibels (dB). Forward power gain of the LNA is given by the scattering parameter S_{21}.

$$\text{Power Gain of LNA (dB)} = S_{21}\text{ (dB)} = 10 \times Log\{\frac{P_2}{P_1}\} \qquad (5)$$

The LNA will attain its maximum power gain when the output impedance equals the complex conjugate of the input impedance. The LNA in this work is designed for a gain of 8.8 dB.

Noise Figure

The fundamental noise performance parameter of the LNA is the Noise Figure or Noise Factor (NF). Noise figure of the LNA is defined as the ratio of the total output noise power to the input noise power. It is calculated from the signal-to-noise ratio (SNR). Hence, it is also represented as a measure of the extent of SNR degradation. It is measured in dB

Signal-to-noise ratio is given by,

$$\text{SNR} = \frac{P_{signal}}{P_{noise}} \qquad (6)$$

Noise figure can be calculated as the ratio of input SNR and the output SNR.

$$\text{NF} = 10 \times Log\{\frac{SNR_{in}}{SNR_{out}}\}\ \text{dB} \qquad (7)$$

The LNA in this thesis is designed for a noise figure of 0.9 dB.

Stability Factor

Stability of the LNA is defined as its resistance to oscillate (G. Gonzalez, 1944). It is a very important parameter and is given a high consideration in design. Stability factor (SF) or the

Rollet stability factor (K) can be measured from the S-parameters of the LNA. It is calculated as follows,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \times |S_{12} \times S_{21}|} \qquad (8)$$

$$\text{Where, } \Delta = S_{11} \times S_{22} - S_{12} \times S_{21}.$$

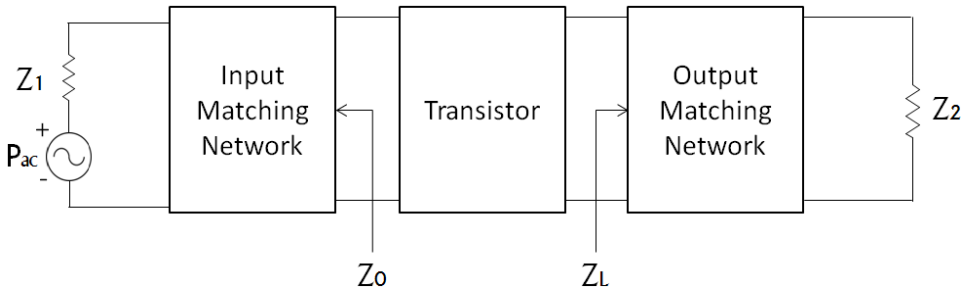
If K < 1, then the LNA is considered to be potentially unstable. In this case, there is a possibility of either the input or the output match returning a negative resistance and hence, paves way for oscillations.

If K > 1, then the LNA is considered to unconditionally stable. In this case, there are no oscillations observed. The LNA in this thesis is designed for K=2.3.

Impedance Matching Network

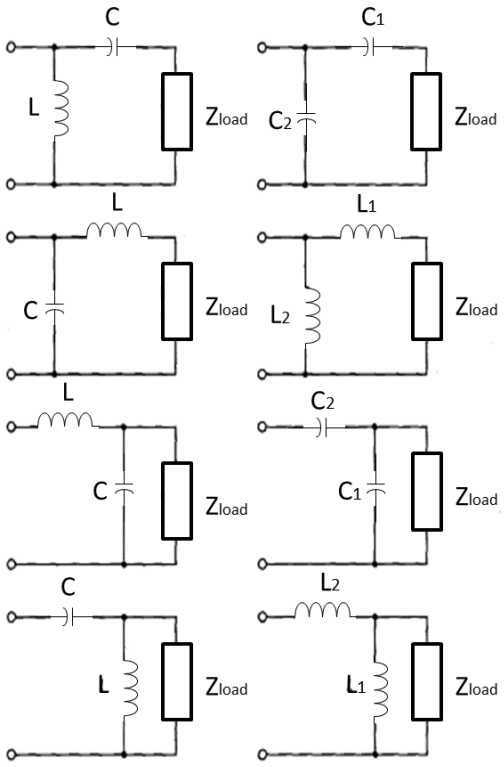
Impedance matching is one of the most important design constraints of LNA design. The input and output networks of the LNA need to be matched in a conjugate manner in order to ensure maximum power transfer to the load. Figure 4 shows the general convention of the matching network (D. Henkes, 2007).

*Figure 4.*Transistor matching network.



The magnitudes of the input and output impedances Z_0 and Z_L should be 50 Ω each to ensure a perfect match. Though this can be achieved by simply putting a 50 Ω resistor at the input and the output ports, the noise generated by the resistor shoots up the noise figure of the complete circuit, thereby necessitating the need for a circuit which is ideally free from resistors. For this reason, the matching networks mostly consist of other passive elements like inductors and capacitors. Since the inductors and capacitors exhibit resistance in the form of impedance, they can be used to form the matching networks at the input and output ports. Some of the typical input match configurations are shown in Figure 5 (G. Gonzalez, 1944).

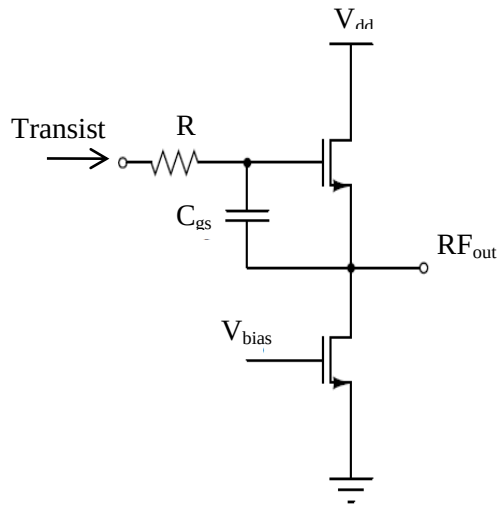
Figure 5. Typical input impedance match configurations.



Most of the input matching networks are completely passive, but some output matching networks often make use of transistors to deliver the necessary impedance (K. Jayaraman, 2009).

This is because when two devices are connected in series, the output of the first device might not be perfectly matched to the input of the second device. This leads to increase in reflections on the first device and a decrease in transmission of the signal to the second device. A transistor-based output matching network in a source follower configuration is shown in Figure 6.

Figure 6. Output matching network in source follower configuration.



Design of the LNA

A narrowband LNA (N-LNA) is used as the reference RF circuit in this thesis. It operates at a resonance frequency at which it has the highest gain. There are several reasons behind choosing an N-LNA instead a wideband LNA (W-LNA). A W-LNA consumes more power because it has a larger transistor width and bias voltage. Also, a bandpass filter structure should be designed to perform as the input impedance matching network for a W-LNA (R. Malmqvist, 2005). These result in use of additional passive devices in the circuit design and eventually lead to the increase in die area. Also, achieving simultaneous input impedance match and noise match for a W-LNA is cumbersome (Z. Y. Huang, 2008).

Designing an LNA, especially for high frequency applications, is challenging to even the most experiences circuit designers. Circuit design of the LNA is challenging for the following reasons (K. Jayaraman, 2009).

1. Transistor selection is the first and most important step in the LNA design. The LNA design trade-offs should be kept in mind while making the selection.
2. Simultaneous requirement of high gain, low noise figure, unconditional stability and good input and output match at the lowest possible current levels.
3. Interdependence of gain, stability, noise figure and input/output match is a design challenge.

Step 1:

In the first step of the design, the Atmel n-channel MOSFET based on 0.18 µm CMOS technology was chosen as the necessary transistor for designing the LNA. The specifications of the LNA are listed in Table 1.

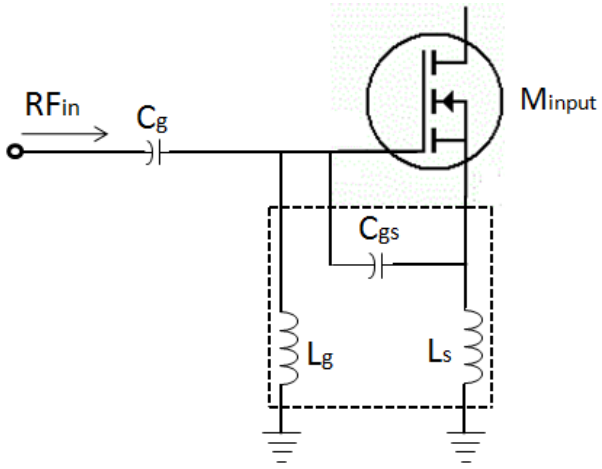
Table 1. LNA specifications.

Parameter	Symbol	Acceptable Range
Input Match	S_{11}	$\leq$ -15 dB
Forward Gain	S_{21}	$\geq$ 8 dB
Output Match	S_{22}	$\leq$ -10 dB
Noise Figure	NF	$\leq$ 2 dB
Stability Factor	K	$\geq$ 1

Step 2:

Second, the circuit for the input impedance match is formulated. Input match of the LNA is very crucial in determining its performance and its effects on the forward gain. The input match is determined by both the active and passive devices of the LNA input front-end (K. Jayaraman, 2009). From Figure 7 it is seen that at the resonance frequency of 5 GHz, the real part of the input impedance is determined by the transconductance g_m, of the MOSFET, the parasitic capacitance C_{gs} and the source inductance L_s. The resonant frequency is given by L_g, L_s and C_{gs} as shown below.

Figure 7. Resonant frequency determination.



$$\text{Resonant frequency, } \omega_0 = \{(L_g + L_s) \times C_{gs}\}^{\frac{-1}{2}} \qquad (9)$$

Noise factor (F) of the LNA is another important parameter. It is a measure of how the signal to noise ratio is degraded by the device.

$$\text{Noise Factor (F)} = SNR_{in}/SNR_{out} \qquad (10)$$

Noise figure is essentially the noise factor expressed in decibels.

$$\text{Noise Figure (NF)} = 10 \times \log (F) \qquad (11)$$

The LNA in this work is designed using the cascode topology with inductive source degeneration and its noise figure is given by the following expression (P. Chiang, 2007).

$$NF = 1 + \left(\frac{\omega_0}{\omega_T}\right)^2 \left(\frac{\gamma}{\alpha}\right)(g_m R_s) + \left(\frac{\omega_0}{\omega_T}\right)^2 \left(\frac{2\gamma}{\alpha\kappa}\right) + \left(\frac{\alpha\delta}{\kappa g_m R_s}\right). \quad (12)$$

Where,

ω_T = Unity current gain frequency,

g_m = Transconductance of the M_{input},

g_{d0} = Drain conductance with zero bias,

$\alpha = (g_m / g_{d0})$,

R_s = Source resistance,

γ = Coefficient of excess channel thermal noise,

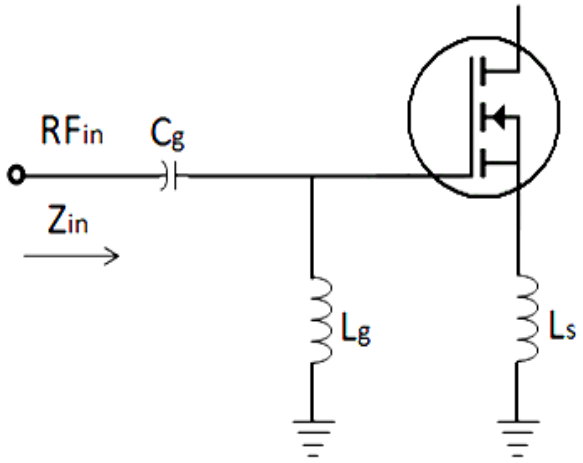
δ = Coefficient of gate noise,

κ = Coefficient of the drain noise and correlated part of the gater noise.

From the above expression of NF, it is evident that as ω_T increases, the drain noise contribution to the overall noise figure decreases for a constant ω_0. Also, the equation proves that there is a minimum value of NF, since, one term in NF is directly proportional to g_m whereas the other is inversely proportional to g_m. In reality, there is an optimum width of the transistor for a given current that will result in minimum NF (K. Jayaraman, 2009).

Figure 8 shows the input matching network used in this thesis. The DC blocking capacitor C_g is placed to prevent upsetting the gate-to-source bias of M_{input}. Its value is chosen to have a negligible reactance at the signal frequency.

Figure 8. Input match configuration.



The above input match topology uses inductive source degeneration (L_s is the degenerate inductor). The inductive source degeneration technique is widely used in MOS and MESFET amplifiers (D. K. Shaeffer, 1997) and is mainly useful in generating a real term in the input impedance. This topology is chosen because it achieves the best noise performance in any architecture and improves linearity by forming a negative series feedback (A. N. Karanicolas, 1996).

Step 3:

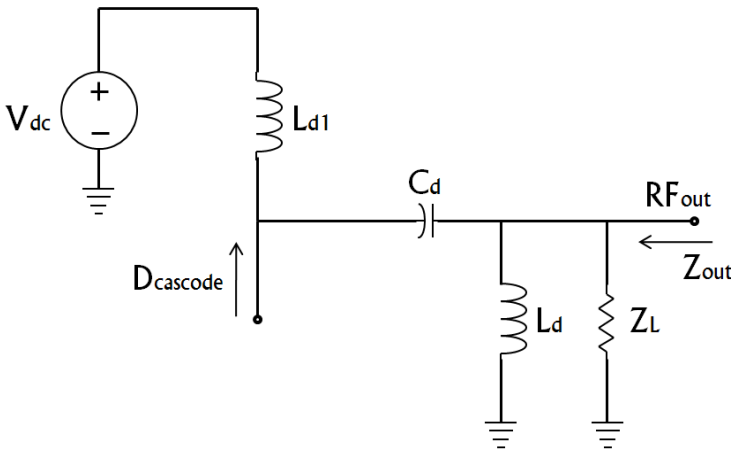
The step after finalizing the input match is to build the cascode stage of the LNA. Since, the input matching is done using a common source topology with inductive source degeneration; a common gate stage is added on top of it to make it a cascode topology. The cascode configuration is necessary to improve the gain and stability of the common source stage (H. H.

Hsieh, 2008). Also, the parasitic capacitance C_{gd} of the input transistor is shielded from the output node which is desired. The cascode transistor also reduces the Miller effect by ensuring a low impedance at the drain of the input transistor and hence, reducing degradation in the power gain and the input noise figure of the LNA (X. Fan, 2008). Additionally, the cascode stage improves the reverse isolation resulting in an increase in the stability of the LNA and reducing the influence of the output matching network over the input matching network (H. S. Kim, 1999). The LNA with the cascode transistor is shown in Figure 10.

Step 4:

The output match is the last step to complete the design of the LNA. The L-C-L architecture used is shown in Figure 9 (M. Kaynak, 2006). The drain of the cascode transistor is connected to the node joining L_{d1} and C_d and the RF_{out} is obtained across the drain inductor L_d.

Figure 9. Output match configuration.



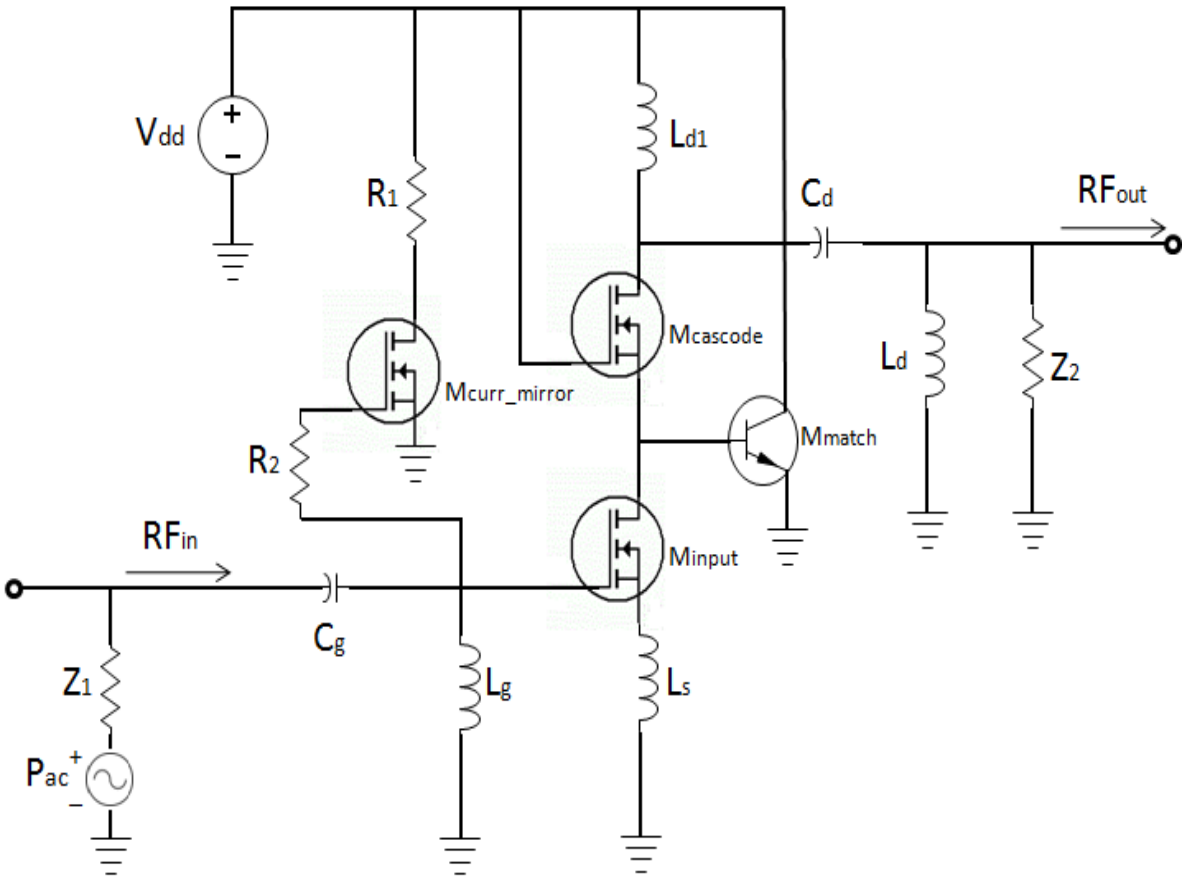
Maximum output is expected when the L_d-C_d resonant frequency matches that of L_g-C_g and the equivalent impedance of L_d-C_d equals the complex conjugate of that of L_g-C_g (D. Henkes, 2007).

The resulting LNA is shown in Figure 10. Transistor M_{curr_mirror} forms a current mirror with M_{input}. Its width is considered a small fraction of that of M_{input}'s in order to minimize the power overhead of the bias circuit (M. Chakraverty, 2010).The current through M_{curr_mirror} is set by the supply voltage V_{dd} and R_1 in conjunction with V_{gs} of M_{curr_mirror}. The resistor R_2 is chosen large enough so that its equivalent noise current is small enough to be ignored.

$M_{cascode}$ reduces the interaction of the tuned output with the tuned input and also reduces the effect of M_{input}'s C_{gd} on the output match. The total node capacitance at the drain of $M_{cascode}$ resonantes with L_{d1} to increase the gain at the center frequency (N. M. Noh, 2007). The input and output resonances are generally equal to each other but can drift with an offset from one another to yield a flatter and broader response if needed.

The M_{match} transistor is used to widen the gain response of the LNA around the center frequency in order to slightly decrease its sensitivity around the operating frequency range. This would lead to a better resistance against smaller variations in the component values of the LNA (K. H. K. Yau, 2007). The M_{match} transistor is chosen in such a way that its base-to-emitter capacitance C_{be} is equal to the average of the gate-to-source capacitance of $M_{cascode}$ and the gate-to-drain capacitance of M_{input}. This causes a slight reduction in the drain current and slightly causes the LNA gain to decrease, but achieves a much lesser input reflection coefficient and leaves the LNA less sensitive to minor parasitic additions (K. Jayaraman, 2009).

Figure 10. Schematic of the 5 GHz LNA.



The values of the components of the LNA are given in Table 2.

Table 2. LNA component values.

Component	Value	Purpose
C_g	280 fF	Input match
L_g	2.5 nH	Input match
L_s	0.48 nH	Input match
M_{input}	L=0.18µm, W=4.8µm	Amplification
$M_{cascode}$	L=0.18µm, W=4.8µm	Amplification
R_1	1 kΩ	DC Bias
R_2	50 kΩ	DC bias input reduction
M_{curr_mirror}	L=0.18µm, W=2.4µm	DC bias current mirror
C_d	340 fF	Output Match
L_d	2.8 nH	Output Match
L_{d1}	6.9 nH	Output Match
V_{dd}	1.8 V	Power Supply

CHAPTER 3

TESTING METHODOLOGY

Introduction

As discussed in Chapter 1, due to process-related and time-degraded variations, LNA parameters like gain, noise figure, stability factor and impedance match are affected. One of the main reasons behind loss of parametric yield is change in the component values of the LNA. Since, the variations affect the component values; we see an offset in the values of the LNA parameters. Hence, by closely observing the parametric changes, we can trace back to the identity of the exact components being affected. A cost-efficient and accurate on-chip testing procedure to identify the parametric variations in the LNA is described in this chapter.

For a perfectly matched LNA, there are an ideal set of values defined for the components in the circuit like the gate capacitance (C_g), source inductance (L_s), drain capacitance (C_d), etc. As mentioned before, if they are disturbed from ideality, the parameters of the LNA drift away from their ideal values. However, if these changes are within their pre-defined acceptable ranges of the LNA (refer Table 1), it is concluded that the LNA is in the operating region. But if the parametric values are outside their acceptable range, then the LNA is said to be faulty. Hence, if there is a way to spot the set of parameters that have varied, and trace

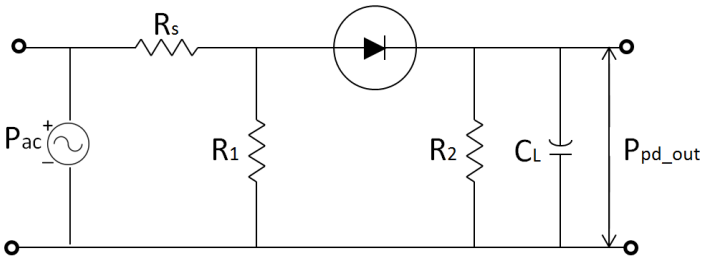
the cause of variation back by observing the drift in specific component values, faults can be detected and eventually corrected. This process of finding the specific components that have varied is referred to as “defect localization”.

For an LNA operational at 5 GHz, capturing the output requires high frequency meters. In order to remove the use of off-chip equipment, a circuit which can convert the high frequency signal at the output of the LNA to low frequency (ideally DC) is desirable. For this purpose, a peak detector circuit is chosen.

Peak detector

A peak detector or precision rectifier is a circuit which detects the peak value of the input signal. A conventional peak detector circuit that utilizes a high frequency diode is shown in Figure 11 below (T. Berenc, 2002).

Figure 11. Peak detector using a high frequency diode.



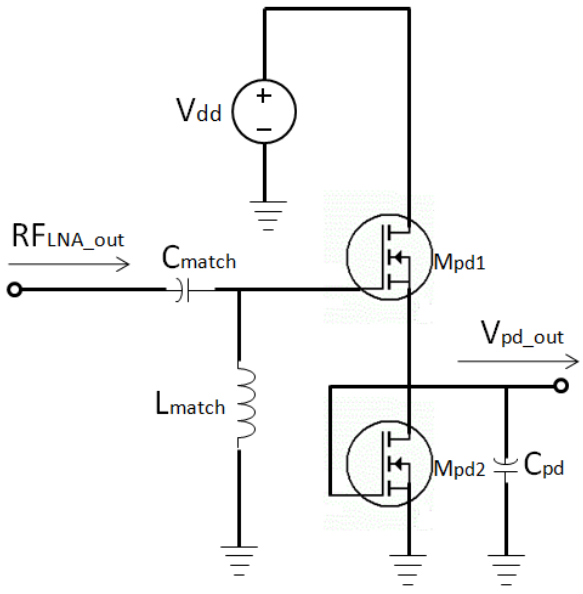
Resistor R_1 is to provide a continuous DC loop through the diode and resistor R_2. If this resistor is absent, then the peak detector circuit gets capacitively coupled to the input RF source and the load capacitor C_L will charge up to twice the maximum RF level and the diode stops conducting. Though this circuit still detects the presence of RF, it will not be able to follow the amplitude variations in the input.

The speed of detection of the circuit depends on the amount of leakage present in the capacitor C_L and is not physically controllable. The R_2C_L time constant determines the maximum frequency that can be received without distortion.

Since diodes are inherently high-impedance devices, such a detector circuit will be mismatched to the RF source. Hence, a resistor (R_s) of 50 Ω is used to appropriately match to the source. Peak detectors with diodes typically require voltage swings almost near 1V to be properly functional. Large LNA gain is required to amplify weak source signals up to the levels required by the detector.

Due to higher sensitivity of diode peak detectors to temperature variations, transistor-based peak detectors would be more preferable. Also since transistor-based peak detectors are more sensitive to parametric variations in the LNA, the output voltage, instead of power can be recorded with a higher precision. Figure 12 shows a source follower peak detector configuration used in this work (K. Jayaraman, 2009).

Figure 12. Source follower peak detector configuration.



Capacitor C_{pd} has to be chosen so that it matches the output of the LNA to the input of the peak detector. Care should be taken that C_{pd} is greater than C_{gs} in order to ensure maximum signal swing at the detector input. If its value is chosen to be very small, the divider will allow only a small part of the RF signal to reach the detector. Hence, its value should be chosen with utmost precision. C_{match} and L_{match} provide the necessary input impedance match to the peak detector and should be chosen in accordance with the output impedance match requirement of the LNA. This configuration consumes low power and is easy to integrate with the LNA.

Look-Up Table (LUT)

After the voltage V_{pd_out} is obtained, the next step in the testing process is to determine if the LNA is faulty or not. To do this, a digital verification procedure using an ADC and a signal processor is employed.

In this procedure, several component fault of the LNA are generated and their corresponding V_{pd_out}s recorded. Some of the faults are shown in Table 3 along with their respective V_{pd_out} value.

Figure 13. Peak detector output variations due to defects in LNA.

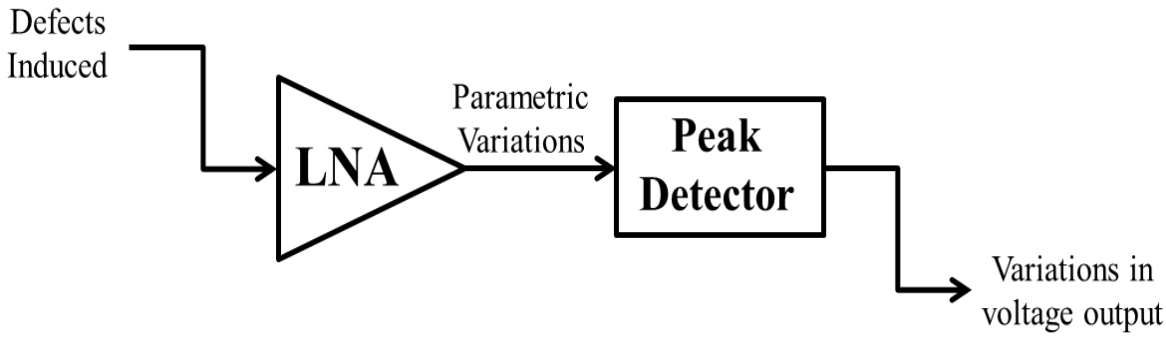


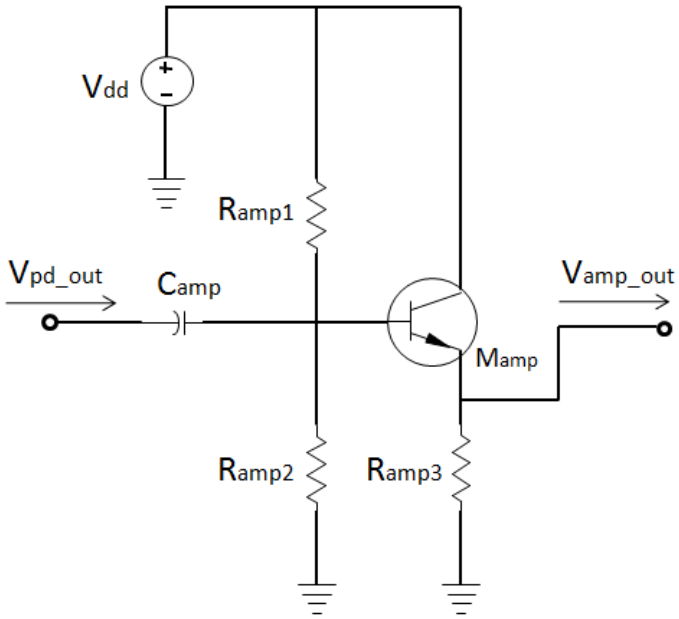
Table 3. Fault percentage of some components along with the LNA parameters affected and the respective peak detector output.

Faulty Component	Fault Percentage (%)	Parameter(s) of the LNA affected	V_{pd_out} (mV)
Cg	30 (decrease)	Gain	112
Lg	50 (decrease)	Gain, Noise Figure	57
Ls	60 (increase)	Gain, Noise Figure	100
Cd	65 (increase)	Gain	189
Ld	20 (decrease)	Gain	151

The output of the peak detector is given to a voltage amplifier which amplifies the value of V_{pd_out}. Amplification after detection is necessary because of the fact that the output of the peak detector is very small (typically in millivolts).

Figure 14 shows the voltage amplifier circuit (F. Najmabadi, 2006). The current going to the emitter of the M_{amp} transistor is controlled by the resistor divider bridge R_{amp1}-R_{amp2}. R_{amp2} is chosen to be approximately 10 times R_{amp1} to amplify the input signal by a factor of 6.

Figure 14. Voltage amplifier circuit.



The voltage amplifier output goes into an A/D converter (ADC) which generates a digital bit stream in accordance with its input (V_{v_amp}). If the output of the peak detector was to be directly given to the ADC, we would need an ADC with high sensitivity and large resolution which would be very hard to design given the operating constraints of the system. Next, the bit stream generated by the ADC is passed into a signal processing unit.

The signal processing unit consists of a logic unit, memory unit and a control unit. For each fault model, each V_{pd_out} has a corresponding V_{v_amp} value, which in turn, has a distinct bit stream generated by the ADC. This bit stream is read by the signal processor and stored in its memory under the variable $V_{test}(i)$, where i = [1, n], n being the fault number. In this way, all the faults and their respective V_{pd_out}s are individually assigned a $V_{test}(i)$ value in the processor memory and are stored in a tabular format to form a look-up table (LUT). The LUT is shown in Appendix C.

Testing Procedure

In the first step of determining the LNA integrity, the output of the LNA is detected by the peak detector, amplified by the voltage amplifier, digitized by the ADC and sent to the signal processor to be read. In the second step, the signal processor creates a variable V_{check} for the current detected value and compares this to all the $V_{test}(i)$s stored in the LUT. If V_{check} is equal to $V_{test}(1)$, which is the value when the LNA is fault-free, then it is concluded that there are no faults in the LNA and that it is operating in an ideal condition. If V_{check} is equal to any other $V_{test}(i)$ other than $V_{test}(1)$, that means the LNA is faulty and the corresponding fault is localized from the LUT. However, if V_{check} is not equal to any of the $V_{test}(i)$, then it is concluded that the fault is out of the test bounds or is not a component variation fault. In this case, it could be a catastrophic fault which means there is either a short circuit, open circuit, etc. in the LNA.

CHAPTER 4

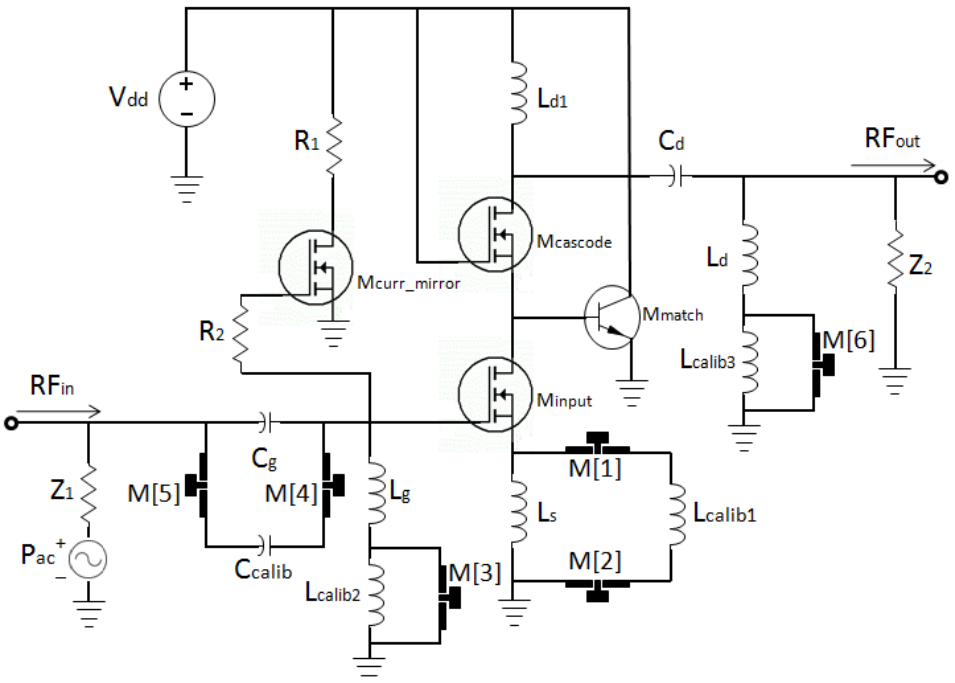
SELF-CALIBRATION METHODOLOGY

Tuning Circuit

If a defective RF circuit in the vicinity of the fault tolerance window can self-calibrate itself after testing, it would cut down the time and cost of debugging and re-designing it. In the previous chapter, the procedure for testing the LNA for faults is discussed. The requirement now is to have a technique that can automatically correct the observed defects and calibrate the LNA into the fault tolerance window. To cater to this requirement, a self-calibrating methodology is proposed. The proposed scheme consists of a self-calibrating or tuning circuit which is interfaced to the LNA by MEMS switches (S. S. Evana, 2011). Figure 15 shows the tuning circuit configuration.

The tuning circuit consists of a bank of inductors and a capacitor. Its components are connected to the LNA at specific locations considering the fact that input and output impedance match be retained even after calibration is performed.

Figure 15. Tuning circuit configuration.



The values of L_{calib1}, L_{calib2}, L_{calib3} and C_{calib} are determined by considering the level of sensitivity of the component which they respectively calibrate and have been adjusted considering the parasitics of the MEMS switches and TSV. Since the values of these tuning components are fixed, there is a fixed range up to which the LNA can self-calibrate itself. The range is carefully determined by keeping the input and output match in mind.

$$L_{calib1} = \frac{3L_s}{2} \qquad (29)$$

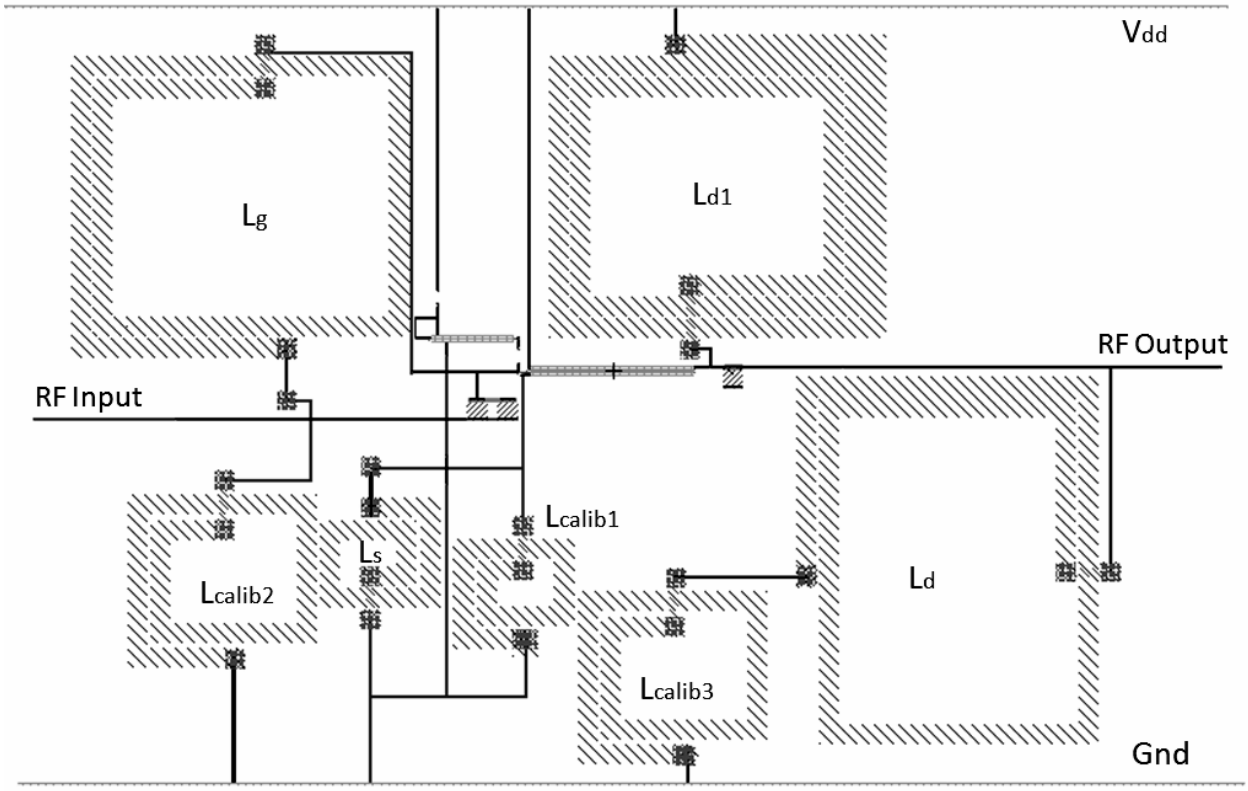
$$L_{calib2} = \frac{L_g}{2} \qquad (30)$$

$$L_{calib3} = \frac{L_d}{2} \qquad (31)$$

$$C_{calib} = \frac{14C_g}{5} \qquad (32)$$

The layout of the LNA with the tuning circuit is shown in Figure 16.

Figure 16. Layout of the LNA with the tuning circuit.



MEMS Switch

Micro-Electro-Mechanical Systems (MEMS) is a technology that in its most general form can be defined as miniaturized mechanical and electro-mechanical elements (i.e., devices and structures) that are made using the techniques of micro fabrication (Freescale Semiconductor, 2009). The physical dimensions of MEMS devices can vary from less than one micron to several millimeters. Likewise, the types of MEMS devices can vary from relatively simple structures having no moving elements, to extremely complex electromechanical systems with multiple

moving elements under the control of integrated microelectronics. Some of the functional elements of MEMS are miniaturized structures, sensors, actuators, and microelectronics. There are three distinct classes of MEMS depending on where and how the MEMS actuation is carried out relative to the RF circuit. The three classes are:

1) RF extrinsic: The MEMS structure is located outside the RF circuit, but actuates or controls other devices (usually micromechanical ones) in the circuit;

2) RF intrinsic: The MEMS structure is located inside the RF circuit and has the dual, but decoupled, roles of actuation and RF-circuit function; and

3) RF reactive: The MEMS structure is located inside the circuit where it has an RF function that is coupled to the actuation (Freescale Semiconductor, 2009).

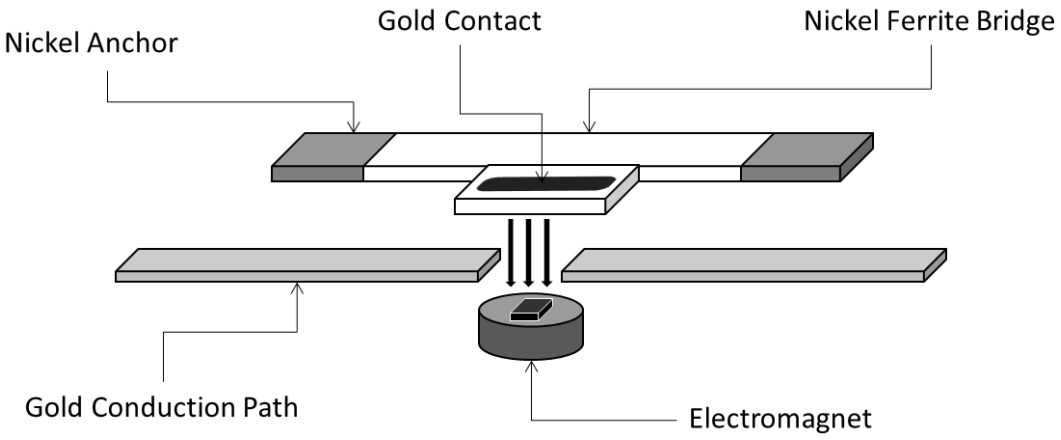
RF MEMS switches are used in high frequency electronic systems because of their high electro mechanical isolation. With MEMS switches, as opposed to the conventional solid state switches, the RF circuit does not leak or couple significantly to the actuation circuit. (E. R. Brown, 1988). RF MEMS switches can deliver high isolation levels of about – 55 dB at frequencies as high as 30 GHz (M. A. Llamas, 2009) which makes them ideal for use. The other advantages are low cost and ease of manufacturing. The disadvantages, however, are their switching speeds and the actuation voltages. MEMS switches have switching speeds between 1 μs and 10 μs (M. A. Llamas, 2009) whereas the transistor switches are faster at 50 ns to 200 ns. Though their switching speeds are comparably lower, the isolation levels of the MEMS switches make them stand out as a clear winner in comparison to the transistor switches. The actuation voltages for MEMS switches range from 5 V to several tens of volts for high frequency applications. Extensive research is being carried out by researchers all over the world in reducing the actuation voltage by optimizing the MEMS switch design on basis of its parameters like

material composition, spring constant, etc. The three ways in which the actuation voltage can be reduced are as follows (S. P. Pacheco, 2000): (1) by increasing the area of actuation, (2) by diminishing the gap between the switch and bottom electrode, and (3) by designing a structure with low spring constant. In the first case, the area can by increased only by so much before the compactness becomes an issue. In the second case, the return loss associated with the RF signal restricts the value of the gap. The third case offers much better flexibility that the first two, since the design of the springs does not impact the size, weight or RF circuit performance considerably. The MEMS switch designed for use in this work is magnetically actuated and has a low spring constant (B. Kim, 2007).

Design of the MEMS Switch

The design consists of a bridge structure which is preferred over the conventional cantilever beam type because of its robustness in high stress environments and overall stability (S. S. Evana, 2011). The bridge structure is composed of nickel ferrite and is 1000µm long, 200µm wide and 4µm thick. It has the ability to bend in the presence of a magnetic field. The plan-view of the magnetic MEMS switch is shown in Figure 17.

Figure 17. Magnetic MEMS switch plan-view.



An arm is connected to the bridge, which closes the circuit through a conduction path. A permanent magnet is placed outside the device structure to actuate the beam and hence closes the switch by default. A coil is used to open the switch by creating a magnetic field equal and opposite to the field produced by the permanent magnet, which restores the beam due to spring force and thereby creating a dynamic equilibrium. This design method improves the total power consumption of the switch since it is coupled by the permanent magnet in a normally closed position (B. Kim, 2007).

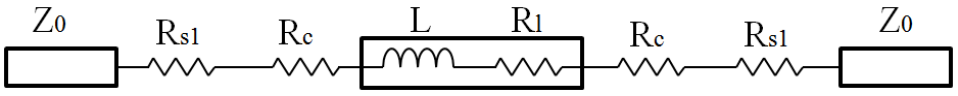
Electrical Modeling of the Switch

Since the MEMS switches are a part of the complete circuit, they need to be modeled to observe their effects on the performance of the LNA. For this, electrical models are developed for the MEMS switches and analyzed.

When the switch is in the ON state, it is termed as the "down state" of the switch and when it is in the OFF state, it is termed as the "up state". Initially, the switch is in the down state when no actuation voltage is applied. In this case, the gold contact is pulled down by the permanent magnet and a physical contact is established to the conduction path.

The electrical equivalent model of the MEMS switch in the down state is shown in Figure 18. The gold conduction path is modeled as a transmission line (t-line) with impedance Z_0. The t-line loss is given by R_{s1}, the contact resistance by R_c and the gold contact is modeled by an inductor L in series with a resistor R_l.

Figure 18. Down state electrical model of the MEMS switch.



The total force exerted on the switch is dependent on the intensity of the magnetic field produced by the permanent magnet, the volume of the ferromagnetic material embedded on the bridge and the spring constant of the flexible bridge (B. Kim, 2007). The net force acting on the switch at equilibrium is given by,

$$F_{coil} + F_{spring} = F_{magnet} \qquad (13)$$

The force exerted by the magnet on the beam in the down state is given by,

$$F_z = \frac{dw_m}{db} \qquad (14)$$

Where, w_m is the total energy in the magnetic fields and b is the gap between the two.

The variable magnetic energy is dominated by the energy shown in the following equation.

$$W_m = \mu_0 H_{gap}^2 bA/2 \qquad (15)$$

Where, A is the area of the permanent magnet surface.

The force is, therefore, given by,

$$F_z = \frac{\mu_0 H_{gap}^2 bA}{2} \qquad (16)$$

Since the nickel beam is 1000 µm long, 100 µm wide and 4 µm thick, the uniform pressure required to bend a doubly clamped beam is given by the following equation.

$$P = \left(\frac{\pi^4}{3}\right)\left(\frac{EH^3}{L^4}\right)c + \left(\frac{\pi^4}{4}\right)\left(\frac{EH}{L^4}\right)c^3 \qquad (17)$$

Where, E = Young's modulus of nickel,

H = Thickness (Height) of the beam,

L = Length of the beam and

C= Deflection of the beam.

The series inductance (L) of the gold contact is given by (D. M. Pozar, 1998),

$$L = \frac{Z_h \beta l}{\omega} \qquad (18)$$

Where, Z_h = Impedance of the t-line,

β = Phase constant,

l = Length of the t-line and

ω = Angular frequency.

The contact resistance (R_c) depends on the size of the contact area, the mechanical force applied and the quality of the metal-to-metal contact (D. Hyman, 1999). The MEMS series switch resistance between the contact areas is dependent on its length and width and is obtained by calculating the loss of a t-line with the same dimensions as the MEMS switch and using the equation (20).

$$\alpha = \frac{R_{s1}}{2Z_0 l}. \qquad (19)$$

The total switch resistance is given by,

$$R_s = 2 \times R_c + 2 \times sR_{s1} + R_l. \qquad (20)$$

In the up state, the switch can be modeled as shown in Figure 19. In this state, capacitive effects dominate the electrical behavior of the switch. A net capacitance, also known as the up state capacitance, is present and is composed of a series capacitance (C_s) between the t-line and the switch metal and a parasitic capacitance (C_p) between the open ends of the t-line. The total up state capacitance is given by,

$$C_u = \frac{C_s}{2} + C_p. \qquad (21)$$

C_s is composed of a parallel plate component ($C_{pp} = \frac{\varepsilon A}{b}$) and a fringing component which is around 30-60% of C_{pp} (G. M. Rebiez, 2003). C_p is computed using specialized MEMS software packages like MEMSPro.

Figure 19. Up state electrical model of the MEMS switch.

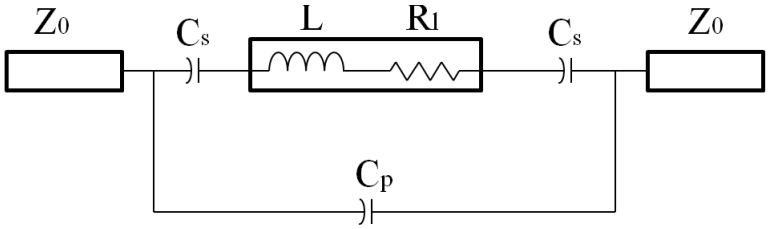
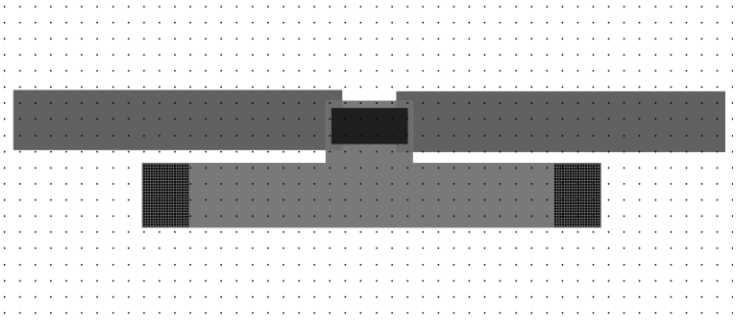


Figure 20. Layout of the MEMS switch in MEMSPro.



In order to perform calibration, the MEMS switches should either turn ON or OFF when required to interface specific tuning circuit components to the LNA. To automate the process, the specific MEMS switches that should be activated are to be determined by the system. To assist the system with this, a MEMS switch matrix which looks like the one shown in Figure 21 is stored in the LUT.

Figure 21. MEMS switch matrix.

[M[1], M[2], M[3], M[4], M[5], M[6]],

Where, M[i], i = [1, 6] is the respective MEMS switch.

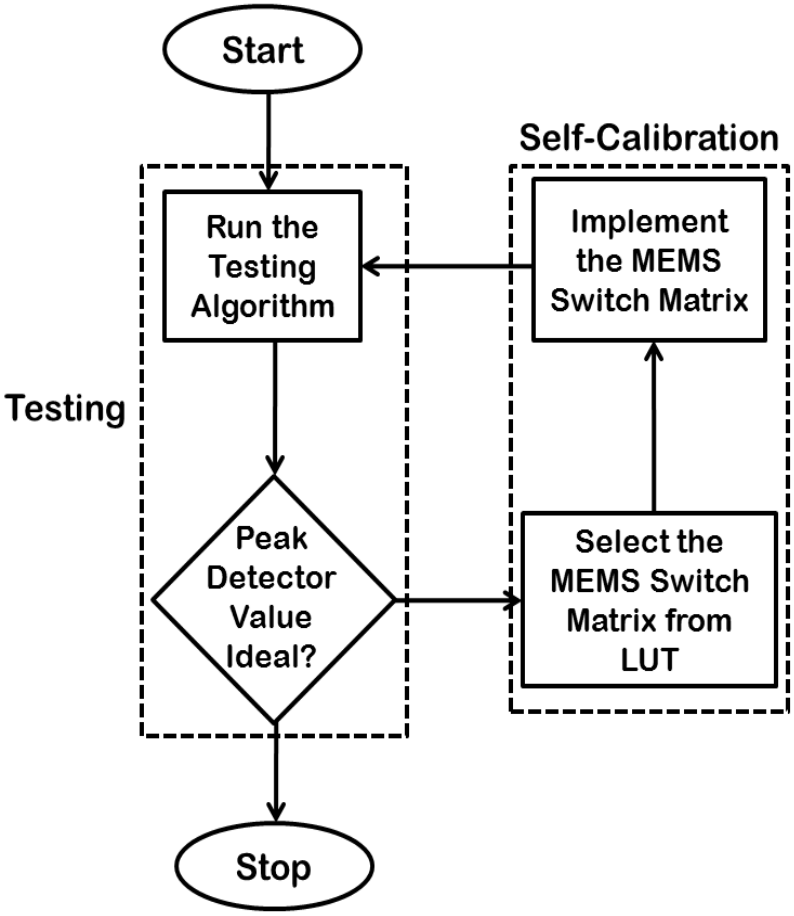
In the case of a faulty LNA, the MEMS switches to be activated for performing calibration are pre-determined for the respective fault and stored in the LUT next to the value of the corresponding $V_{test}(i)$. If a MEMS switch is activated, a "1" is stored in its place; else a "0" is stored. Logic "1" is equivalent to 5 V and logic "0" is equivalent to 0 V.

Self-Calibration Procedure

The self-calibration procedure employs an "elect-and-select" process. This process occurs after the testing process. Once the LNA is deemed to be faulty and the corresponding $V_{test}(i)$ value is determined, then the respective MEMS switch matrix stored next to it is implemented. Some $V_{test}(i)$ might have multiple MEMS switch matrix definitions in which case each matrix is implemented in successive order until the right match is found. Since, in this case, a series of MEMS switch combinations are briefly elected in succession until the right combination is found and selected; this process is termed as elect-and-select.

The complete testing and calibration procedure is shown in a flowchart format in Figure 22.

Figure 22. Flowchart of testing and calibration procedure.



CHAPTER 5

3D-TSV STACKING TECHNIQUE

Introduction

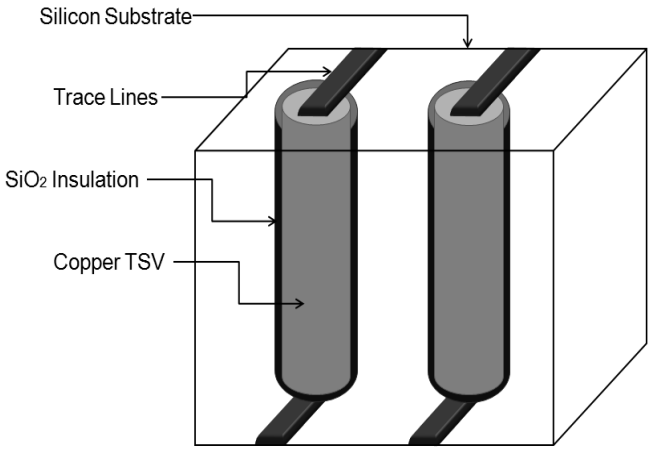
3D packaging is considered to be the new frontier of chip fabrication considering the innumerous advantages it has to offer. Current technologies used for stacking multiple dies are wire bonding, flip chip, etc. These technologies are advantageous in certain applications and are not applicable to a general application set. For example, applications such as cellular telecommunications and portable consumer electronics require flip-chip packaging for its small form factor and high speed whereas, in applications with more than 100 I/Os, wire bonding is preferred for its compatibility with the existing infrastructure, flexibility and material/substrate costs (P. Elenius, 2000). But there are several disadvantages with these technologies. Flip chip packaging requires flat surfaces to mount the dies which is often very difficult to maintain as the surrounding temperature varies. In wire bonding, it is difficult to stack more than three dies because of an increase in wire density which might lead to mutual inductance effects among the wires. Hence, there is need for a packaging technology which can overcome the disadvantages of the current technologies.

3D-TSV technology is believed to be the most promising solution to overcome the disadvantages of the current technologies. It provides many advantages like physical size reduction, shorter interconnect length, faster operating speeds, lower power consumption, etc. (S. Kannan, 2010).

Theory

TSV is emerging as an effective technique for scaling, packaging and continuing the drive to attain high density and high performance in ICs. A TSV is essentially a hole in a substrate filled with a conducting material like copper, tungsten, etc. to form a path from the top face of the substrate to the bottom face in order to act as an interconnect. Figure 23 shows a typical arrangement of TSVs in the silicon substrate.

Figure 23. TSV arrangement in silicon substrate.



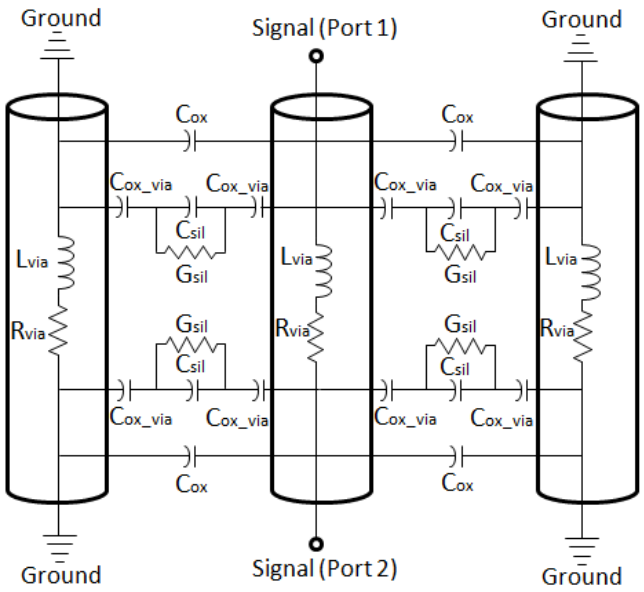
Some of the widely used techniques to drill holes in the substrate are Deep Reactive Ion Etching (DRIE) and Laser Drilling. In DRIE (Bosch Process (M. Peuch, 2007)), the substrate is bombarded with Sulfur Hexafluoride (SF_6) to form nearly-vertical trenches. Next, a SiO_2 layer is formed around the walls of the trench to act as an insulator between the conductor and the

substrate. Then, a conducting material like copper or tungsten is filled into the trench. DRIE process can achieve higher micrometer (> 100 µm) TSV dimensions but is not a good choice for lower micrometer (< 50 µm) and nanometer ranges. In laser drilling, Ytterbium lasers are commonly used for drilling holes in the substrate. Laser drilling can achieve lower micrometer TSV dimensions and can also drill trenches at angles with higher speed and precision in comparison to DRIE. The disadvantage with laser drilling, however, is its high power consumption and cost of operation.

Electrical Modeling of TSV

Electrical modeling of a TSV paves way for understanding the parasitics within and de-embedding them at the time of performing measurements. Since the TSV is considered for high-frequency applications, the modeling is performed in a coplanar waveguide manner to enable power measurements. Figure 24 shows the equivalent electrical model of a TSV (S. Kannan, 2010).

Figure 24. Equivalent electrical model of a copper TSV.



The dimensions of the TSV are as follows: Height of the TSV (h_{TSV}) = 90 µm, diameter of the TSV (D_{TSV}) = 75 µm, thickness of SiO_2 (t_{ox}) = 0.1 µm, distance between two TSV (d) = 100 µm. Parasitic values were calculated from the following expressions.

Substrate capacitance between via, $C_{sil} = \frac{\varepsilon_0 \varepsilon_r A}{d}$. (22)

Where,

ε_0 = Permittivity of free space,

ε_r = Relative permittivity of silicon,

A = Surface area of the via,

Conductance of substrate, $G_{sil} = \frac{\pi\sigma}{\ln(\frac{d}{2a} + (\sqrt{\frac{d^2}{2a^2} - 1}))}$. (23)

Where,

σ = Resistivity of silicon.

Capacitance of the oxide around the via, $C_{ox\_via} = \frac{4\varepsilon_0 \varepsilon_r t_{si}(r_{via} - t_{ox})}{t_{ox}}$. (24)

Where,

t_{si} = Thickness of silicon (height),

t_{ox} = Thickness of oxide (SiO_2).

Surface SiO_2 and fringing capacitance between two via, $C_{ox} = ((\frac{2}{C_{ox\_via}} + (\frac{\varepsilon_0 \varepsilon_r A}{d})^{-1}))^{-1}$. (25)

Resistance of the via, $R_{via} = R_{tin} + \frac{t_{si}}{4\sigma_{cu} r_{via}^{2}}$. (26)

Where, R_{tin} = Resistance of the tin contact= $\frac{t_{diffusion}}{4\sigma_{tin} r_{via}^{2}}$, (27)

$t_{diffusion}$ = Thickness of tin contact diffusion,

σ_{tin} = Conductivity of tin,

σ_{cu} = Conductivity of copper,

r_{via} = Radius of the via.

Inductance of the via, $L_{via} = (\frac{\mu}{\pi}) \times \ln(\frac{d}{2a} + (\sqrt{\frac{d^2}{2a^2} - 1})) \times t_{si}$. (28)

Where, μ = Permeability of silicon.

Proposed architecture

In order to optimize the usage of available on-chip real estate, the complete RF circuitry is designed on two dies. Die 1 consists of the MEMS switch matrix and Die 2 consists of the LNA, the peak detector and the tuning circuit. These dies are stacked using 3D-TSV procedure as shown in Figure 25 (S. S. Evana, 2011).

Figure 25. Stacking of dies using TSV.

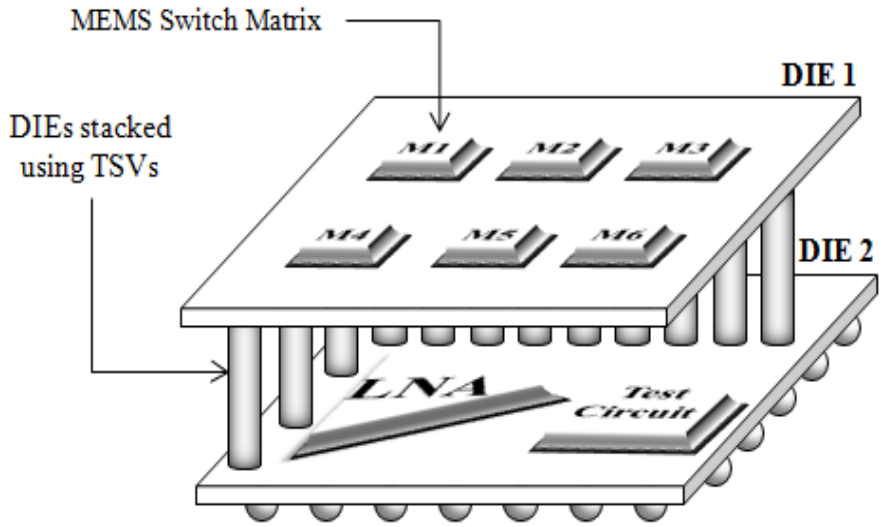
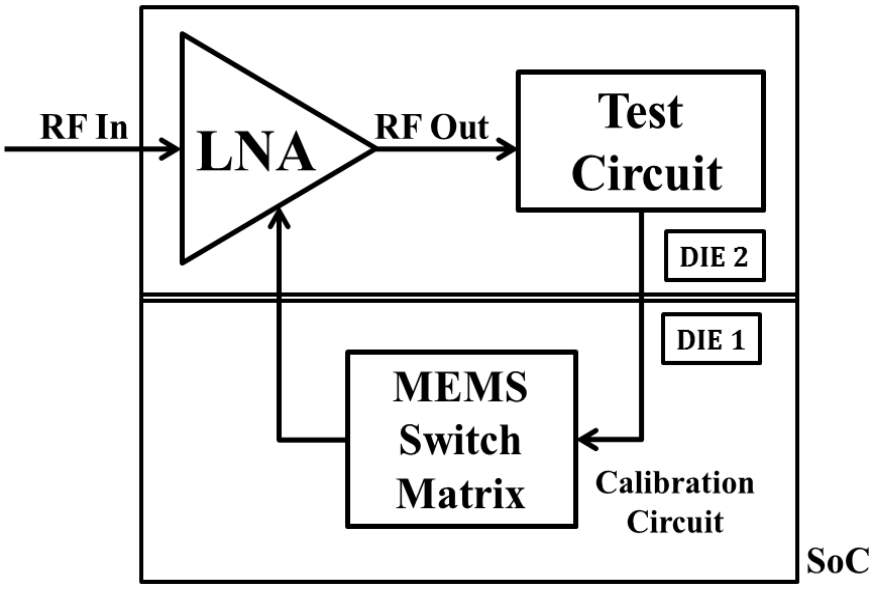


Figure 26. Composition of DIE 1 and DIE 2.

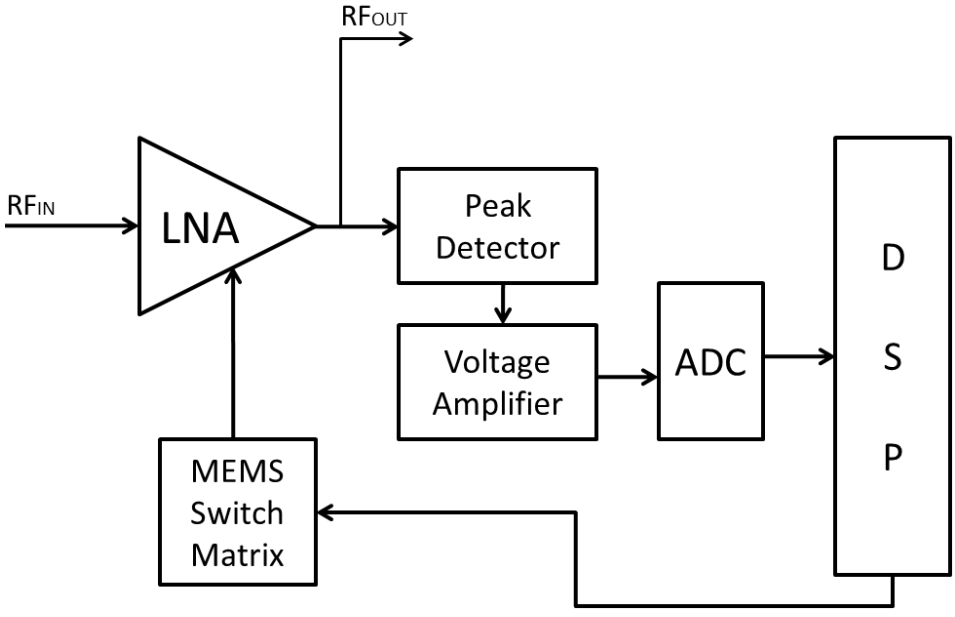


CHAPTER 6

RESULTS AND DISCUSSION

The LNA, the peak detector, the voltage amplifier and the tuning circuit were designed in Agilent's Advanced Design System (ADS). The electrical equivalent models of the MEMS switch and TSV were included in the final model and simulations were performed. Figure 27 shows the block diagram of the complete system.

Figure 27. Block diagram of the complete test and calibration setup.



Calculation of TSV Parasitics

The parasitics of the TSV were calculated and the component values of the LNA were adjusted to suit the inclusion of these parasitics into the final circuit. The TSV parasitics are calculated as shown below.

Capacitance of silicon between the via, $C_{sil} = \frac{\varepsilon_0 \varepsilon_r A}{d}$.

Where, $\varepsilon_0 = 8.854 \times 10^{12}$ Fm^{-1},

$\varepsilon_r = 3.9$

$A = \pi \times r_{TSV} \times h_{TSV} = 1.06 \times 10^{-8}$ m^2.

Therefore, C_{sil} = 3.88 fF.

Conductivity of silicon, $G_{sil} = \frac{\pi\sigma}{\ln(\frac{d}{2a} + (\sqrt{\frac{d^2}{2a^2} - 1}))}$ = 39.6 1/Ωm (per unit length).

Where, σ = 10 Ωcm.

Capacitance of SiO_2 around via, $C_{ox\_via} = \frac{4\varepsilon_0 \varepsilon_r t_{si}(r_{via} - t_{ox})}{t_{ox}}$ = 5.36 pF.

Where, t_{si} = 90 µm.

Surface SiO_2 and fringing capacitance between two via,

$C_{ox} = \left(\left(\frac{2}{C_{ox\_via}} + \left(\frac{\varepsilon_0 \varepsilon_r A}{d}\right)^{-1}\right)\right)^{-1}$ = 4.21 fF.

Where, ε_r = 4.5 for SiO_2.

$$R_{via} = R_{tin} + \frac{t_{si}}{4\sigma_{cu} r_{via}^{2}} = 8.75\ m\Omega$$

Where, $R_{tin} = \frac{t_{diffusion}}{4\sigma_{tin} r_{via}^{2}}$,

$t_{diffusion} = 1\ \mu m$,

$\sigma_{tin} = 66.67\ (\Omega m)^{-1}$,

$\sigma_{cu} = 401\ (\Omega m)^{-1}$.

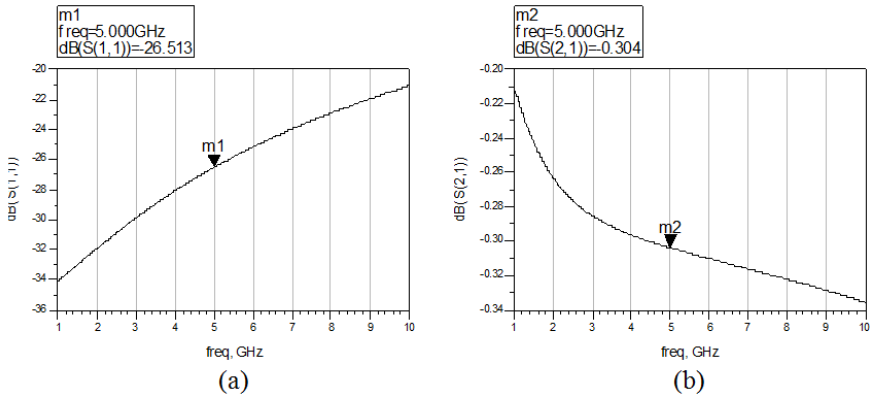
$$L_{via} = (\frac{\mu}{\pi}) \times \ln(\frac{d}{2a} + (\sqrt{\frac{d^2}{2a^2} - 1})) \times t_{si} = 28.63\ pH.$$

Where, $\mu = 4\pi \times 10^{-7}\ Hm^{-1}$.

Electrical Performance of TSV

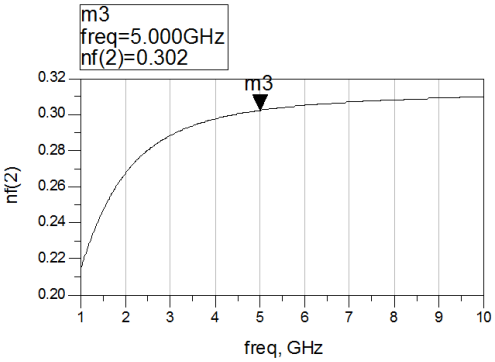
The performance of the electrical model of the TSV is validated by its S-parameters simulated in Advanced Design System (ADS). The input reflection coefficient and the transmission coefficient are as shown in Figure 28 (a) and (b) respectively. Excellent transmission is obtained using the TSV with negligible loss. Reflections are also considerably low.

Figure 28. (a). Input reflection coefficient of TSV. (b) Transmission coefficient of TSV.



Because of the presence of resistors in the equivalent model, noise is added to the signal being transmitted through the TSV. However, since the resistor values are small (in milliohms), the noise level is negligible and does not affect the overall performance. The noise level (in dB) at 5 GHz in the TSV is shown in Figure 29.

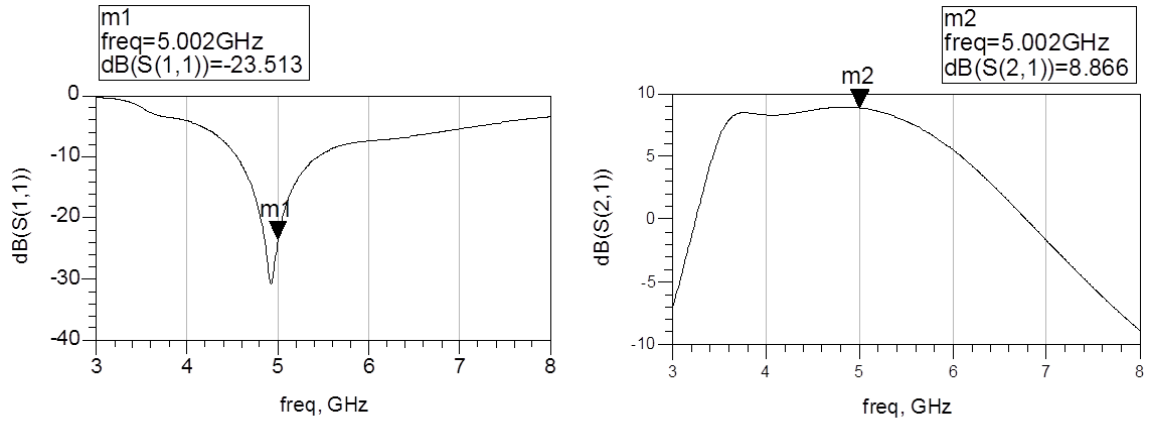
Figure 29. Noise figure of the TSV.



Effects of TSV Parasitics on LNA Performance

The presence of parasitics within the TSV causes a variation in the parameters of the LNA. The TSV parasitics at the gate inductance (L_g) and source inductance (L_s) of the LNA affect its performance as shown in Figures 30 and 31.

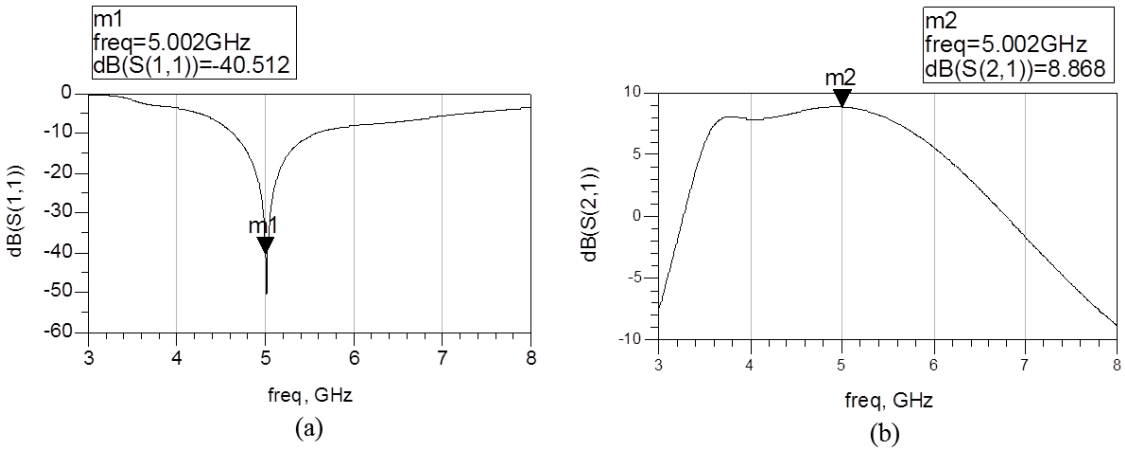
Figure 30. TSV parasitic effects at L_g on (a). Input reflection coefficient and (b). Power Gain of the LNA.



(a) (b)

As seen from Figures 38 and 39, though there is a slight degradation observed in the input reflection coefficient and the power gain of the LNA, their values are still within the individual acceptable ranges mentioned in Table 1.

Figure 31. TSV parasitic effects at L_s on (a). Input reflection coefficient and (b). Power Gain of the LNA.



(a) (b)

Calculation of MEMS Switch Parasitics

From the formulae of electrical model of the MEMS switch mentioned in chapter 4, calculations were performed as follows.

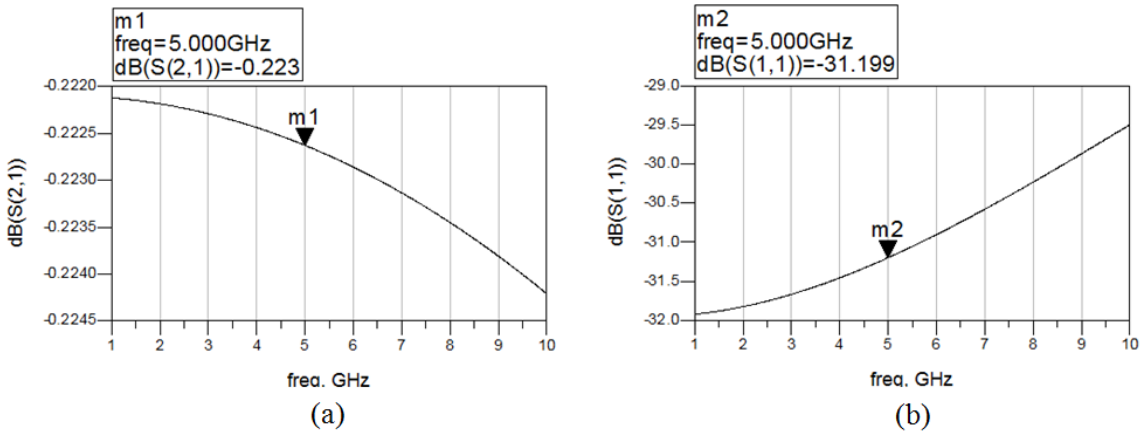
In the down state, the contact resistance (R_c) for a gold-to-gold contact is 0.9 Ω as measured in (B. Kim, 2007) for a force of 500 μN. The t-line loss (R_{s1}) and the gold contact resistance (R_l) are calculated to be 0.32 Ω and 0.15 Ω respectively. Hence, the total switch resistance (R_s) is 2.59 Ω. The series inductance (L) of the switch is calculated to be 36 pH.

In the up state, the series capacitance (C_s) is 6.5 fF and the parasitic capacitance (C_p) is 2.4 fF. Hence, the total up-state capacitance (C_u) is obtained as 5.65 fF.

Electrical Performance of the MEMS Switch

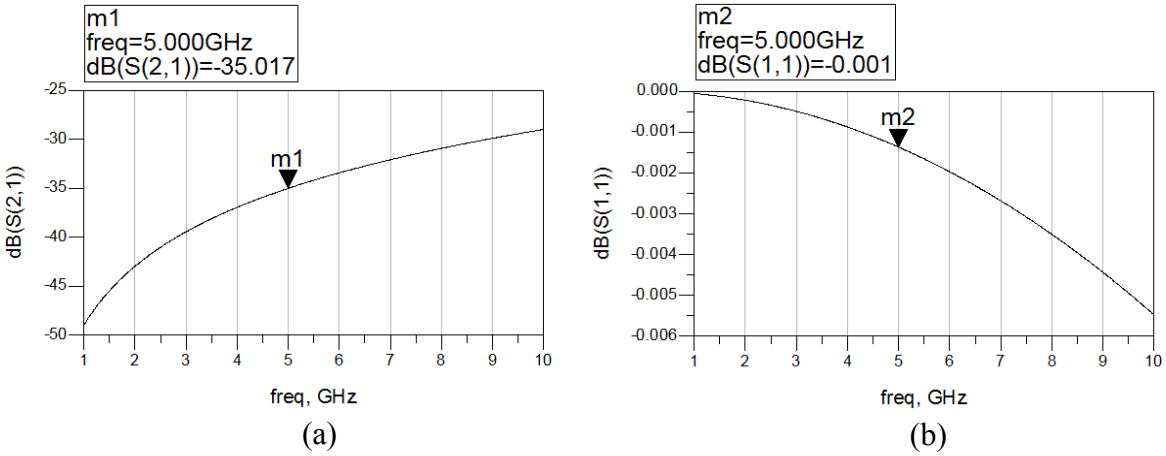
The electrical model of the MEMS switch was designed in ADS and its S-parameters were observed as shown in Figure 32 and Figure 33.

Figure 32. (a). Transmission coefficient of down state MEMS switch. (b). Input reflection coefficient of the down state MEMS switch.



The MEMS switch in down state had excellent transmission and reflection performance. The transmission coefficient and the input reflection coefficient were found to be -31.2 dB and -0.22 dB respectively at 5 GHz. This implies most of the signal given at the input port of the switch is transmitted to the output port.

Figure 33. (a). Transmission coefficient of up state MEMS switch. (b). Input reflection coefficient of the up state MEMS switch.



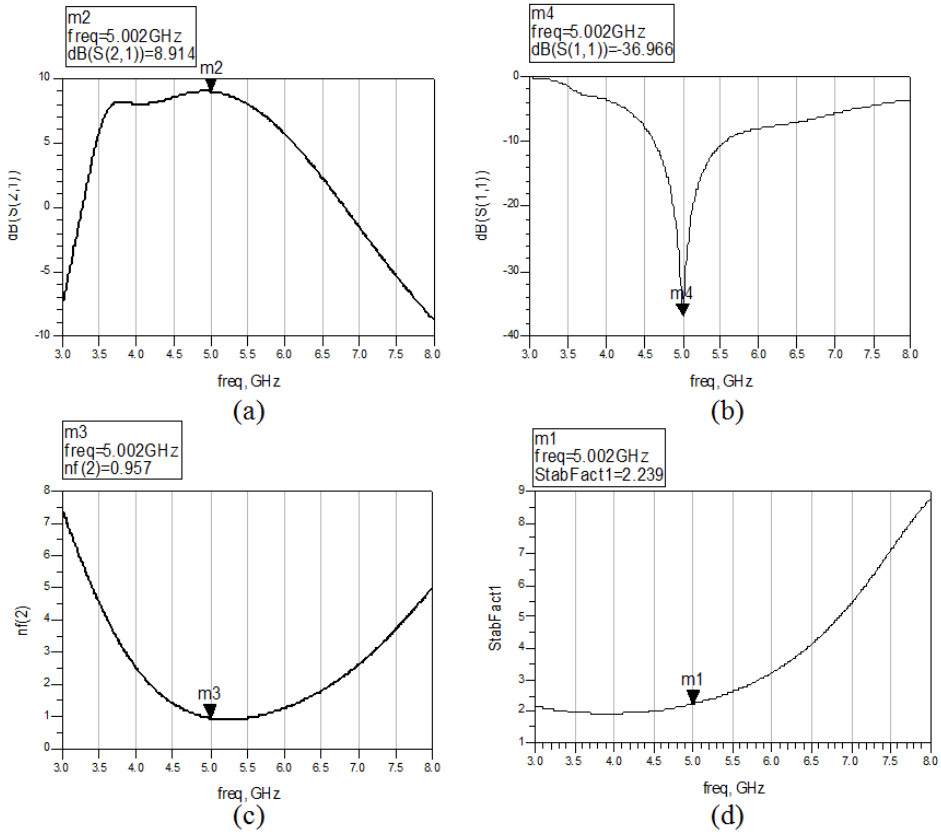
(a) (b)

In the up state, the MEMS switch showed excellent isolation. The transmission coefficient and the input reflection coefficient were found to be -35 dB and 0 dB respectively at 5 GHz. This implies that no signal transmission occurs in this state.

LNA Ideal Performance

The input reflection coefficient, output power gain, noise figure and stability factor of the LNA under ideal conditions is as shown in Figure 34. The component values of the LNA were adjusted to accommodate the TSV and MEMS switch parasitics.

Figure 34. (a). Transmission coefficient (b). Input reflection coefficient (c). Noise figure and (d). Stability factor of the LNA in ideal state.



Fault Cases of the LNA

Case 1:

If a fault is induced into the LNA at C_g by reducing it by 40%, then the resultant gain and noise figure are as shown in Figure 35. Gain is reduced to 6.98 dB from 8.9 dB and the noise figure is increased to 2.44 dB from 0.96 dB. By following the testing procedure mentioned in chapter 5, the respective MEMS switch matrix chosen is [0, 0, 0, 1, 1, 0]. From the switch matrix it is seen that the switches M[4] and M[5] are activated. The gain response after calibration is compared with the ideal response and is shown in Figure 36.

Figure 35. (a). Transmission coefficient and (b). Noise figure of the LNA for a fault induced at C_g.

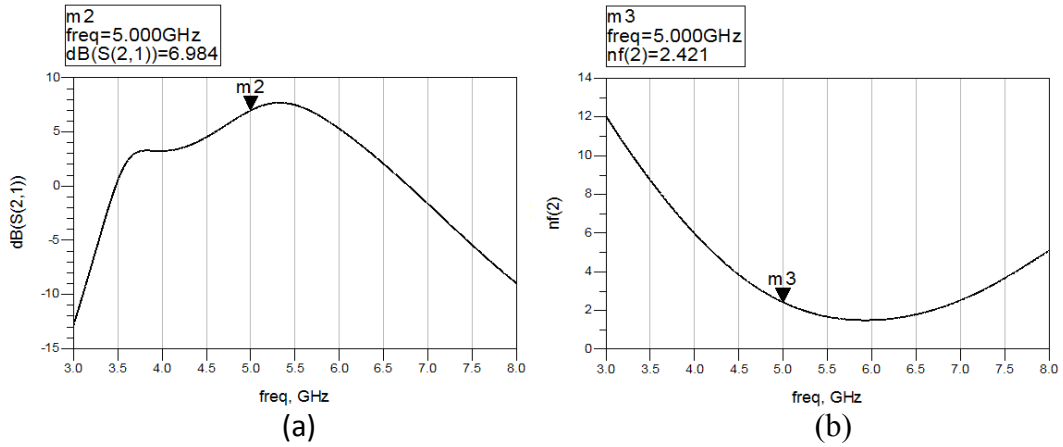
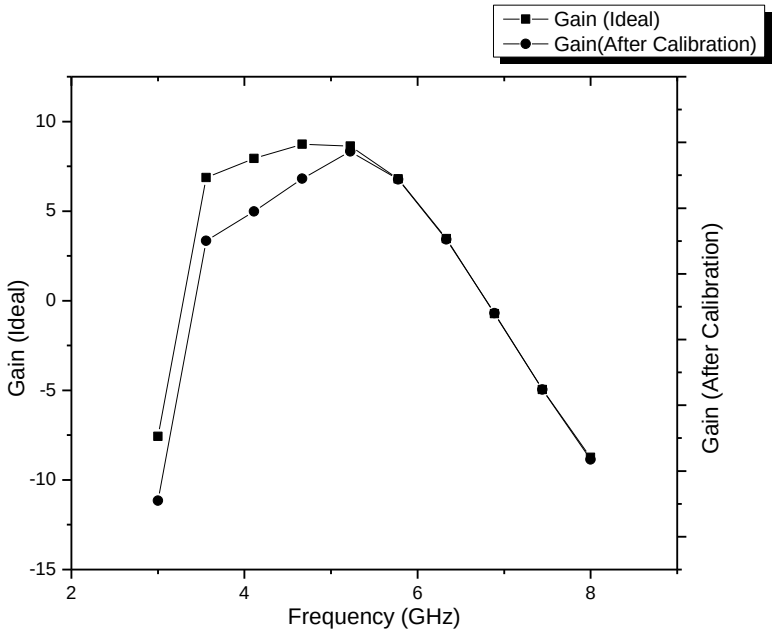
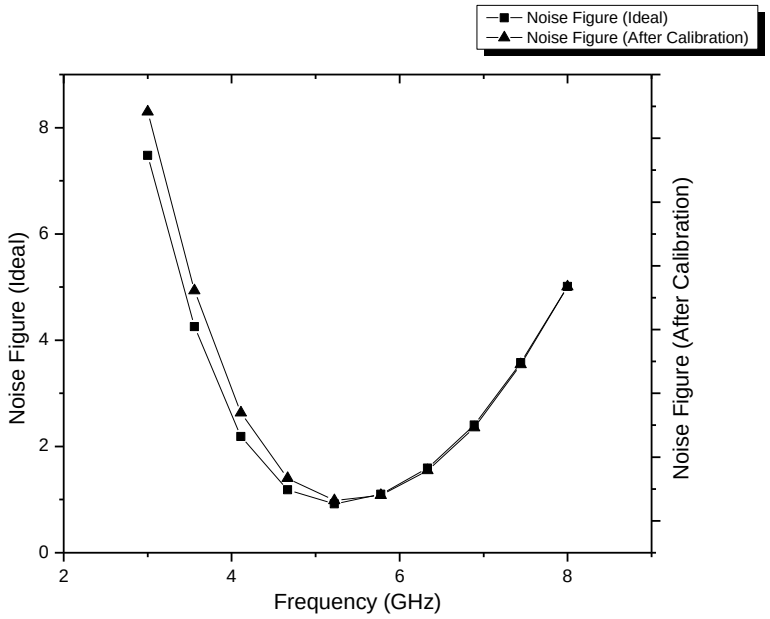


Figure 36. Plot of gain after calibration in comparison with ideal gain for Case 1.



As seen in Figure 36, the ideal and post-calibration curves are almost in agreement at 5 GHz. For frequencies less than 5 GHz, a maximum difference of 4 dB is observed between the two curves for the frequency sweep, but are almost equal at and after 5 GHz. The noise figure is retained inside the acceptable range as well, as seen in Figure 37.

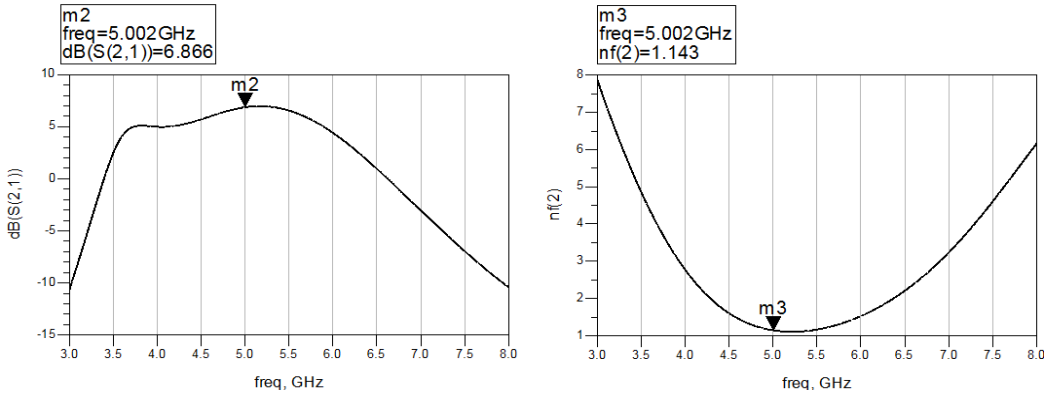
Figure 37. Plot of noise figure after calibration in comparison with ideal noise figure for Case 1.



Case 2:

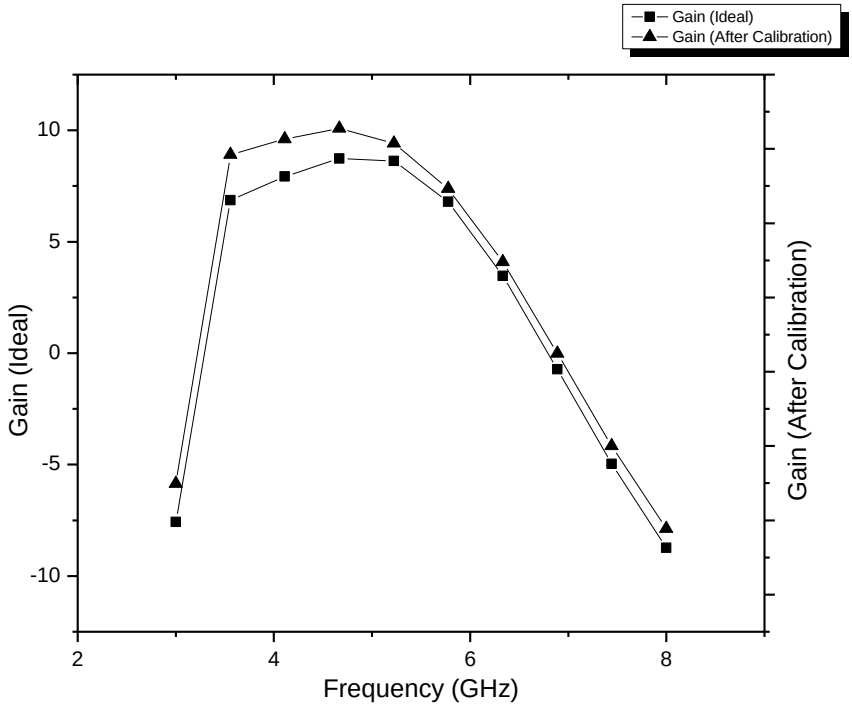
If L_s increases by a factor of 1.6, then the gain drops to 6.86 dB and the noise figure rises to 1.14 dB. Noise figure is less than 1.5 dB so it is in the acceptable range, but the gain is out of range. The respective plots are shown in Figure 38.

Figure 38. (a). Transmission coefficient and (b). Noise figure for a fault induced at L_s.



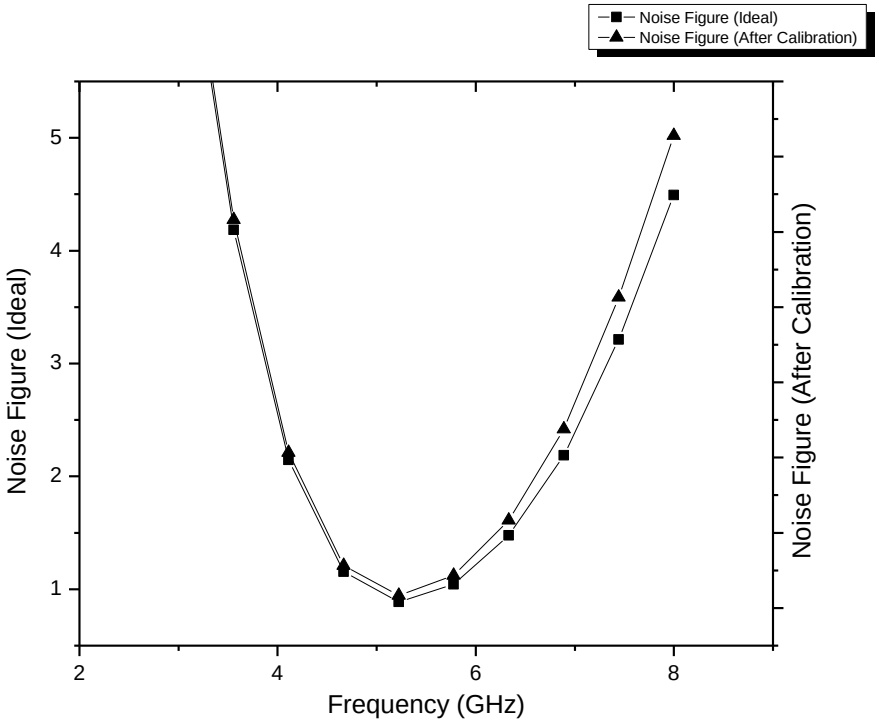
After testing, the respective MEMS switch matrix for this case is [1, 1, 0, 0, 0, 0]. Hence, the switches M[1] and M[2] are activated. Figure 39 shows the ideal gain curve against the post-calibration gain curve.

Figure 39. Plot of gain after calibration in comparison with ideal gain for Case 2.



As seen from Figure 39 the gain curves in the ideal state and after calibration are in a good agreement. A maximum difference of 1 dB is observed at 5 GHz and is well within the requirement range. Noise figure is also retained well within the acceptable range. After calibration, the noise figure stands at 0.88 dB and hence, is 0.5 dB lesser than the ideal value. Figure 40 shows the comparison plot between ideal and post-calibration noise figure value.

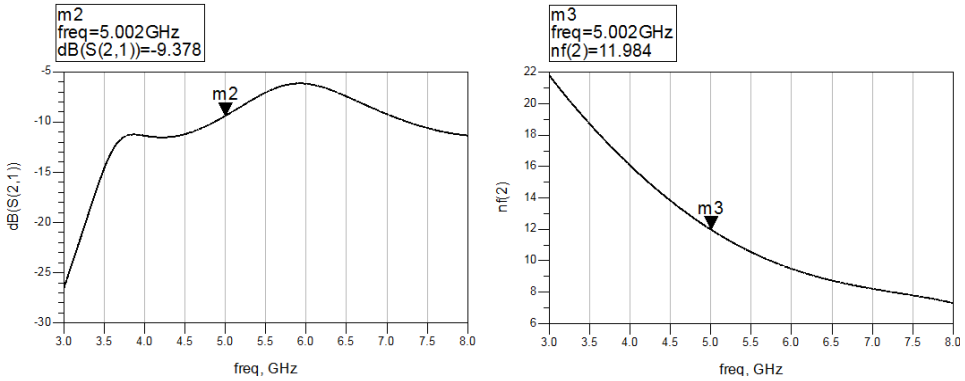
Figure 40. Plot of noise figure after calibration in comparison with ideal noise figure for Case 2.



Case 3:

If C_g decreases by 50%, L_g decreases by 52% and L_s increases by a factor of 1.87, then the gain and noise figure vary by drastic amounts as shown in Figure 41.

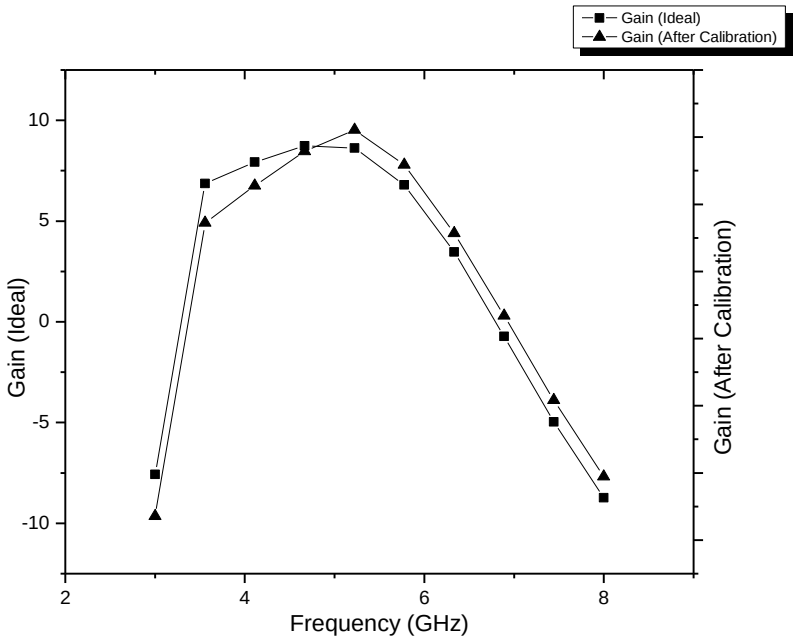
Figure 41. (a). Transmission coefficient and (b). Noise figure for a fault induced at C_g, L_g and L_s.



(a) (b)

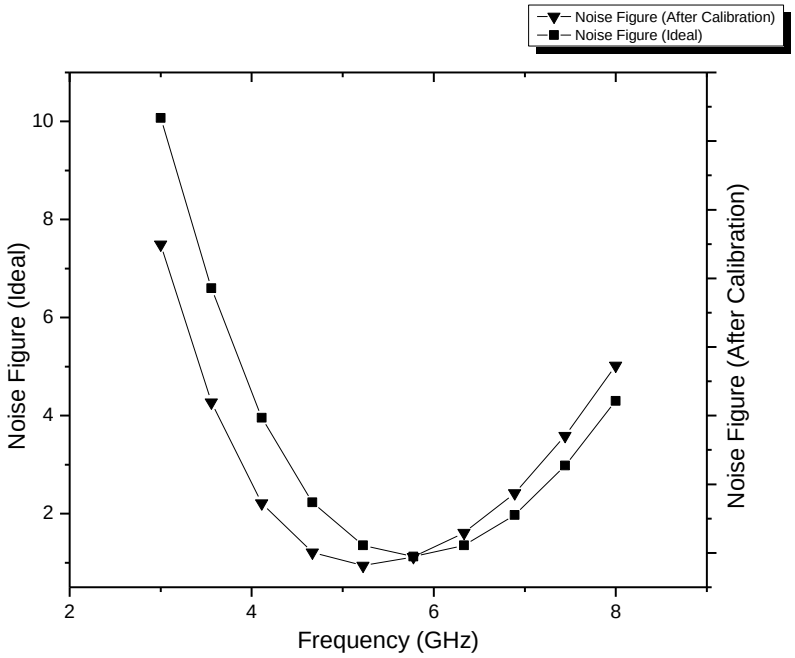
Higher reflections occur in this case because of an increase in impedance mismatch. This leads to a decrease in the LNA gain. Due to the increase in input reflection coefficient and decrease in the input impedance, the minimum noise figure shoots up causing a rise in the total amplifier noise which in turn leads to a higher system noise figure.

Figure 42. Plot of gain after calibration in comparison with ideal gain for Case 3.



These component variations are identified at the time of testing and the corresponding switch matrix is chosen. In this case, the switch matrix is [1, 1, 1, 1, 1, 0]. All the MEMS switches except M[6] are activated in order to get the LNA parameters back into their acceptable ranges. After the respective switches are turned on, the gain of the LNA goes higher than its ideal value by about 0.6 dB. The noise figure, though higher than the ideal value by 0.5 dB, is still acceptable since it is less than 1.5 dB which is the acceptable limit. Figure 42 and Figure 43 show the post-calibrated gain and noise figure graphs plotted in comparison with their ideal equivalents respectively.

Figure 43. Plot of noise figure after calibration in comparison with ideal noise figure for Case 3.

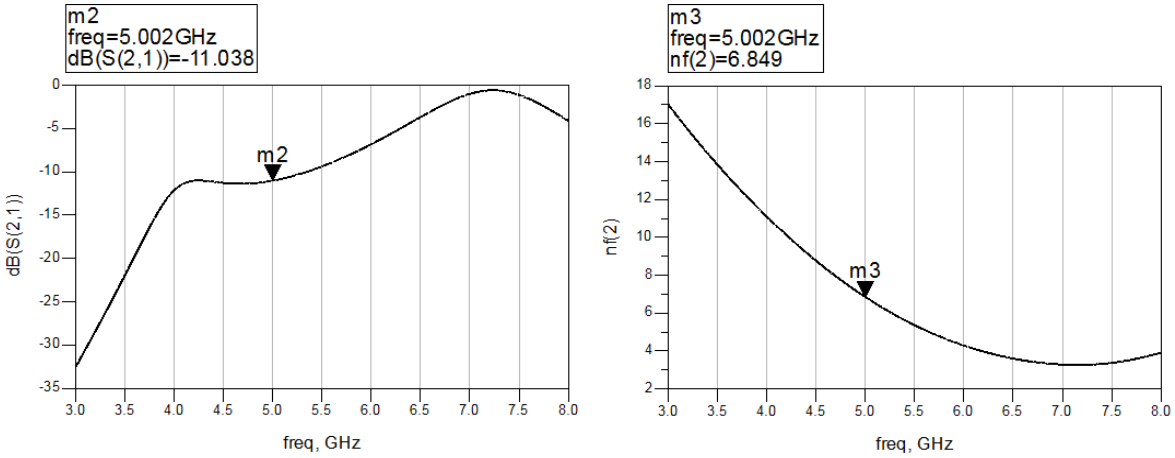


Higher gain is generally acceptable with the exception of this resulting in a higher noise figure. Since gain and noise figure are rated considerably higher among the parameters of the LNA that share highly sensitive tradeoff levels, it is often difficult to retain one in the presence of the other. However, in this case, both the parameters are comfortably placed in their acceptable ranges.

Case 4

If C_g decreases by 46%, L_g decreases by 40%, L_s increases by a factor of 1.45 and L_d decreases by 65%, then the variation of gain and noise figure with frequency are plotted and are shown in Figure 44.

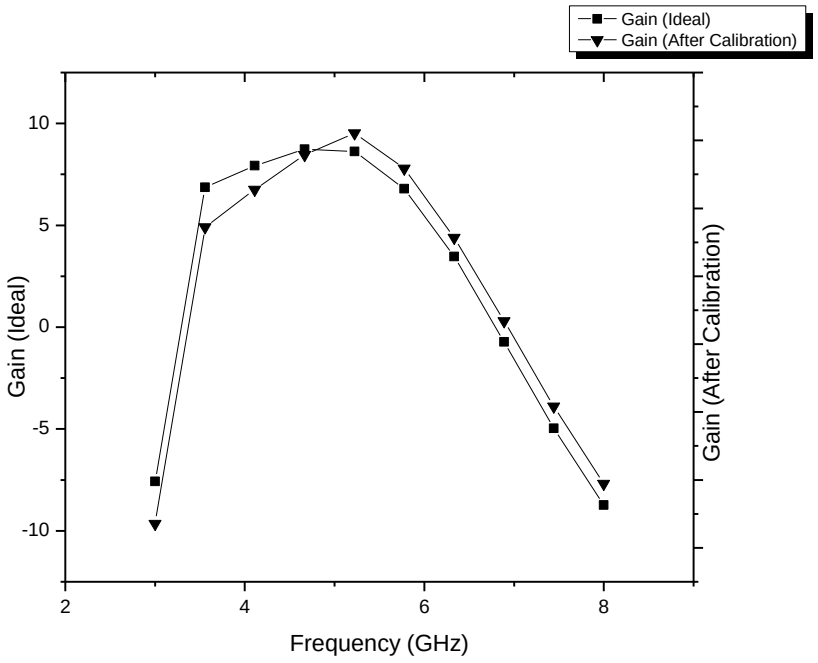
Figure 44. (a). Transmission coefficient and (b). Noise figure for a fault induced at C_g, L_g, L_s and L_d.



(a) (b)

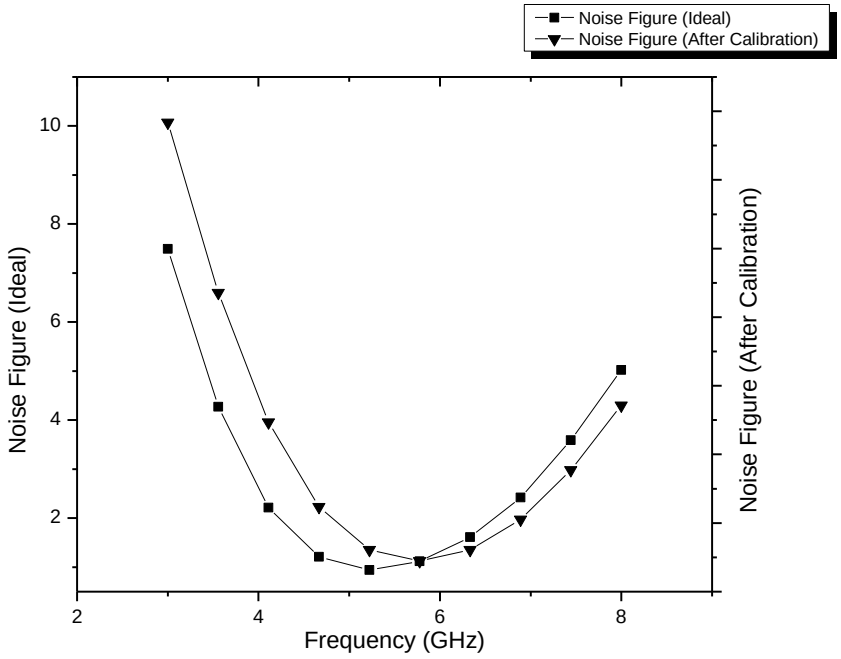
This case is among one of the worst possible faults and deteriorates the LNA performance by a great amount. The gain of the LNA is reduced to -11 dB which implies a huge impedance mismatch that results in reflecting back the entire received signal at the input of the LNA. The noise figure ascends to more than 6 dB which corresponds to higher noise levels at the output of the LNA. Both, the gain and the noise figure, are not desirable at these values. Hence, from the testing procedure, the respective MEMS switches to be activated to calibrate the LNA back to its operating region are determined. The required switch matrix looks like [1, 1, 1, 1, 1, 1], which implies all the MEMS switches are to be activated in this case. The gain and noise figure after calibration are compared to their ideal counterparts and are shown in Figure 45 and Figure 46 respectively.

Figure 45. Plot of gain after calibration in comparison with ideal gain for Case 4.



After calibration, the gain of the LNA is in close agreement with the ideal gain value at 5 GHZ. The calibrated value is about 0.8 dB higher than the ideal value and is acceptable. The noise figure, after calibration, is higher than the ideal value by almost 0.4 dB but is well within the acceptable range.

Figure 46. Plot of noise figure after calibration in comparison with ideal noise figure for Case 4.



CHAPTER 7

CONCLUSION AND FUTURE WORK

A novel testing and self-calibration schemes have been proposed in this work. These schemes are integrated with the designed 5 GHz LNA on a single chip and help in improving its performance across process variations. The test circuitry includes a peak detector to convert the RF output of the LNA into a DC voltage and a voltage amplifier to amplify the peak detector output. The voltage amplifier output is digitized by the ADC and the result is compared with the LUT stored in the DSP to check for the ideality of the LNA. If the LNA is found to be non-ideal, then the respective MEMS switch matrix from the LUT is implemented resulting in self-calibration of the LNA. This process results in the LNA reconfiguring its gain and noise figure without significant degradation in linearity, stability and impedance match.

The use of MEMS to cater to the need of switching is found to be highly reliable. Their high isolation levels in the OFF state ensured no leakage and excellent operation in the ON state with very low parasitic additions ensured near-ideal conduction. The use of MEMS switches in self-calibration enabled correction of gain and noise figure to their acceptable ranges of > 8 dB and < 2 dB respectively.

The use of 3D-TSV technology to stack two dies, one with MEMS switches and the other with RF circuitry, reduced the complexity of fabrication and efficiently optimized the use of real estate. Better signal integrity is achieved with TSV interconnects than the conventional wire bonds because of their smaller lengths and lesser parasitic effects.

The MEMS based test and self-calibration schemes proposed in this work along with the 3D-TSV stacking technique can be extended to the entire front-end of the RF receiver system. The stages after the LNA, like the mixer and the band-pass filter can also utilize these techniques to reconfigure themselves and help maintain the complete RF front-end in the near-ideal operating region.

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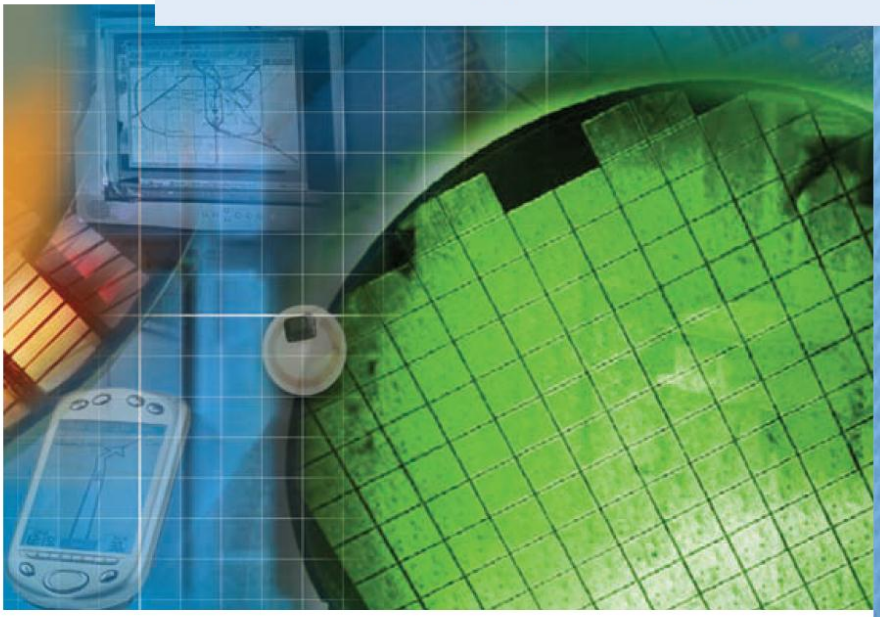
APPENDIX A

FOUNDRY

RF CMOS FOUNDRY

RF CMOS
0.18 MICRON TECHNOLOGY

Atmel's 0.18 micron RF CMOS process technology provides a low-cost solution for high-performance RF applications.



Key Features

- 1.8V CMOS Transistors
- 3.3V I/O
- Embedded EEPROM
- Low Leakage MOS
- Isolated NMOS
- Analog Poly Resistors
- N+ & P+ S/D Resistors
- MIM Capacitor
- Inductor
- 4 – 6 Interconnect Metal Layers
- Shallow Trench Isolation

Key Benefits

- Low Power
- Low Cost
- High Speed
- On-Chip Trimming Capabilities
- Large Selection of Passive Components

Application Segments

- Wireless Phone
- WiMedia
- WiLAN
- ZigBee™
- Bluetooth™
- High Speed Data Transfer
- 3G

ATMEL

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
TEL 1 (408) 441-0311
FAX 1 (408) 487-2600

Regional Headquarters
Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
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0.18 µm RF CMOS Key Process Features	
Core Voltage	1.8V
I/O Voltages	3.3V
Substrate/Well Formation	9 ohm/cm p-type bulk / Triple Well
Isolation	Shallow Trench Isolation
Gate Oxide Thickness	27Å (1.8V I/O) / 63Å (3.3V I/O)
Metal Pitch	0.48 µm
Single Poly EEPROM	12 µm²
Inductor	4 µm AlCu

0.18 µm RF Characteristics	
F_t	58 GHz
F_{max}	65 GHz
High Value Poly Resistor	1000 ohm/sq
MIM Capacitor	1.60 fF/µm²
H/A Varactor	1.60 fF/µm² @ 1.8V
Inductor	Q = 15 @ 2 GHz

Development Support

Atmel's process design kit (PDK) provides the critical tools necessary for analog and RF design. Extensive silicon-verified RF models increase the probability of first pass success for our customers.

- Comprehensive EDA tools
- SRAM Compiler
- NVM
- Standard Cell Libraries
- I/O Libraries
- ESD Libraries

Advanced Backend Services

Atmel offers full backend support. We provide test program development and production testing services of wafers and assembled packages. Atmel has experience in standard, custom, and advanced packaging including stacked die and other System-in-Package (SiP) solutions, which we make available to our customers. Through our silicon and package-level qualification and characterization programs, customers achieve an enhanced level of confidence in their systems long-term performance.

MPW and Low Cost Prototyping

Atmel's Multi-Project Wafers (MPW) give our customers a lower cost, efficient method to verify their 0.18 um RF CMOS designs and prototypes. Atmel also supports engineering runs for pre-production design verification. These allow our customers maximum flexibility to validate their systems overall design performance.

Benefits of Foundry Service

Atmel is a worldwide leader in providing IC system solutions. Our 0.18 um RF CMOS process technology provides our customers with all of the key transistor and passive components necessary to design a complete System-on-Chip (SoC) solution. Our silicon-verified models combined with frequent MPW scheduling and superior customer service reduces cost and time-to-market. Atmel's experience in high-volume manufacturing and leadership in advanced packaging provides our customers with low-cost turnkey solutions to include custom and System-in-Package (SiP) capability. All these features make Atmel the IC Foundry of choice for fabless companies looking to gain a competitive advantage in the marketplace.

Please send an inquiry to atmelfoundryusa@atmel.com for more information about this technology or other Atmel IC Foundry products.

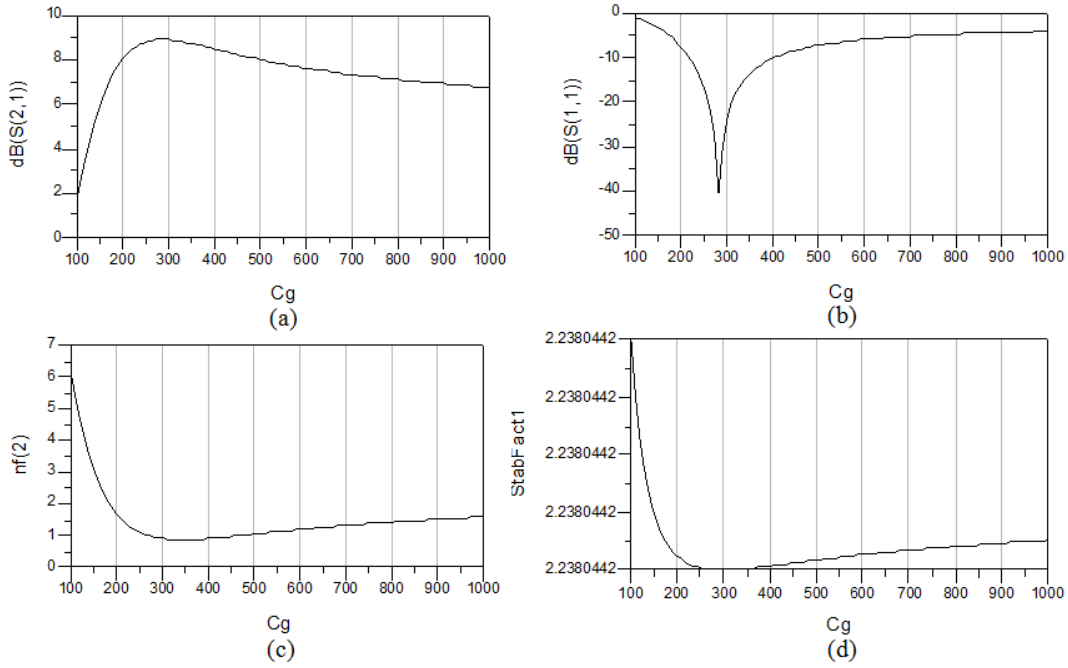
5136B-05/06/1K

APPENDIX B

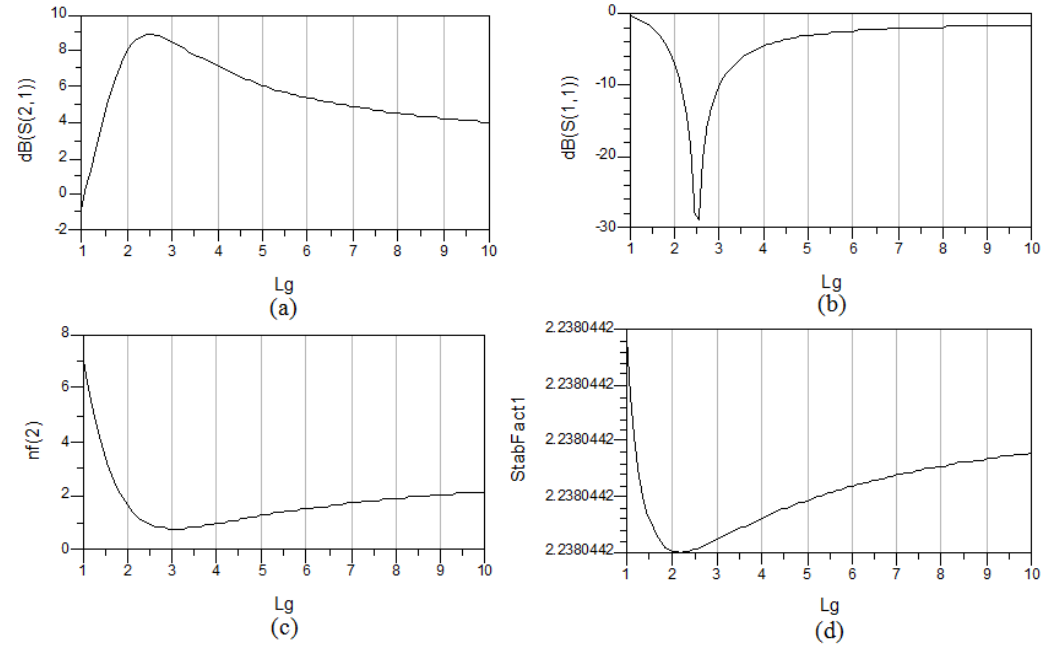
Variation of LNA parameters with the components

(a). Power Gain (b). Input Reflection Coefficient (c). Noise Figure (d). Stability Factor.

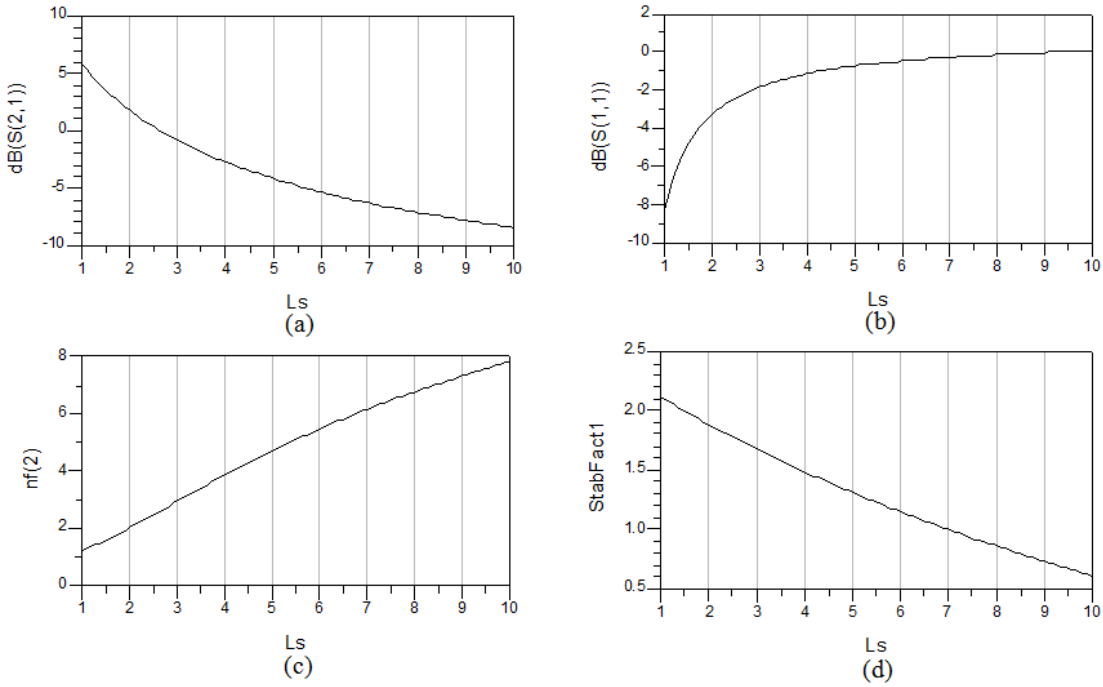
1. Variation with gate capacitor (C_g)(fF):



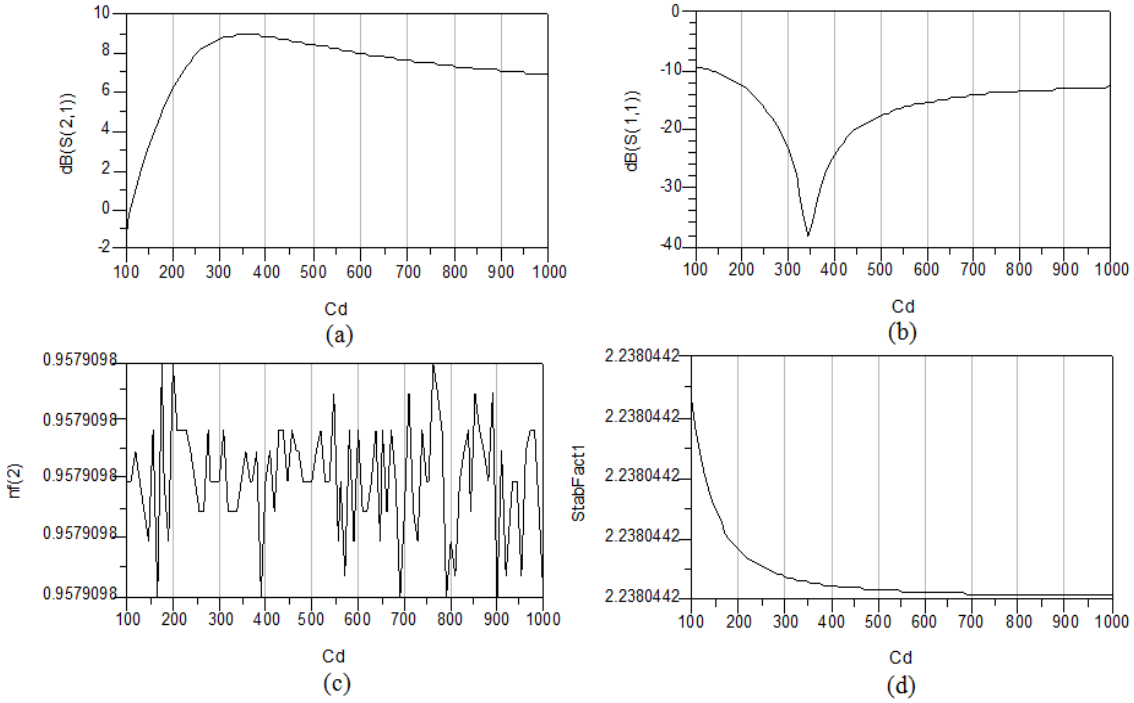
2. Variation with gate inductor (L_g)(nH):



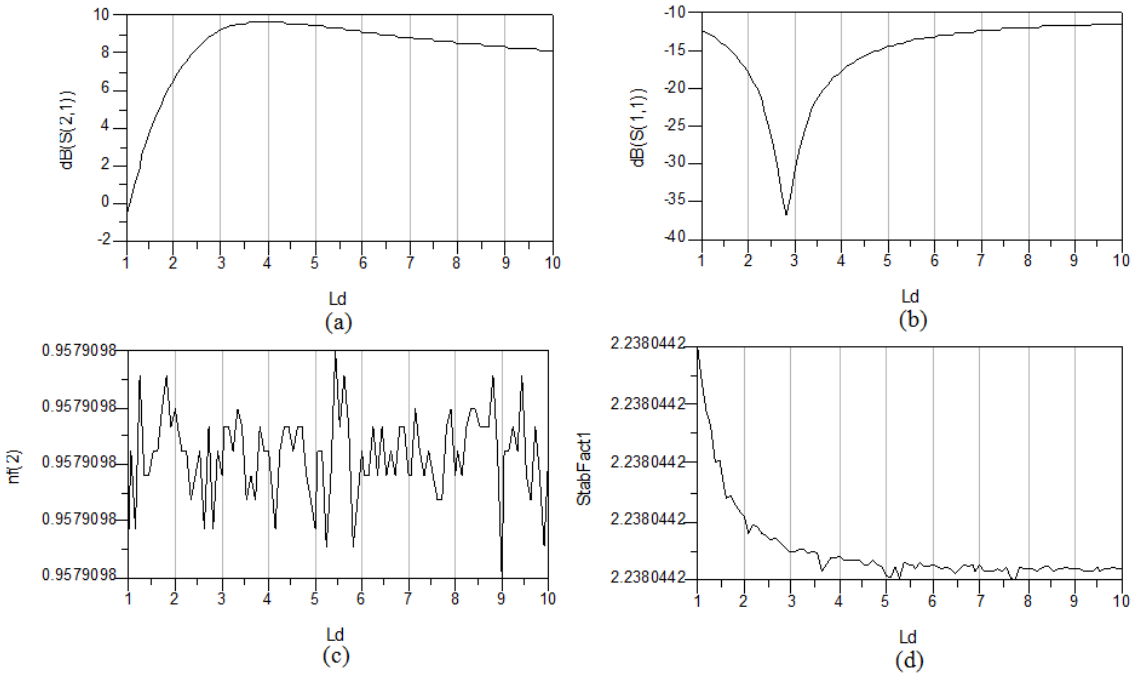
3. Variation with source inductor (L_s)(nH):



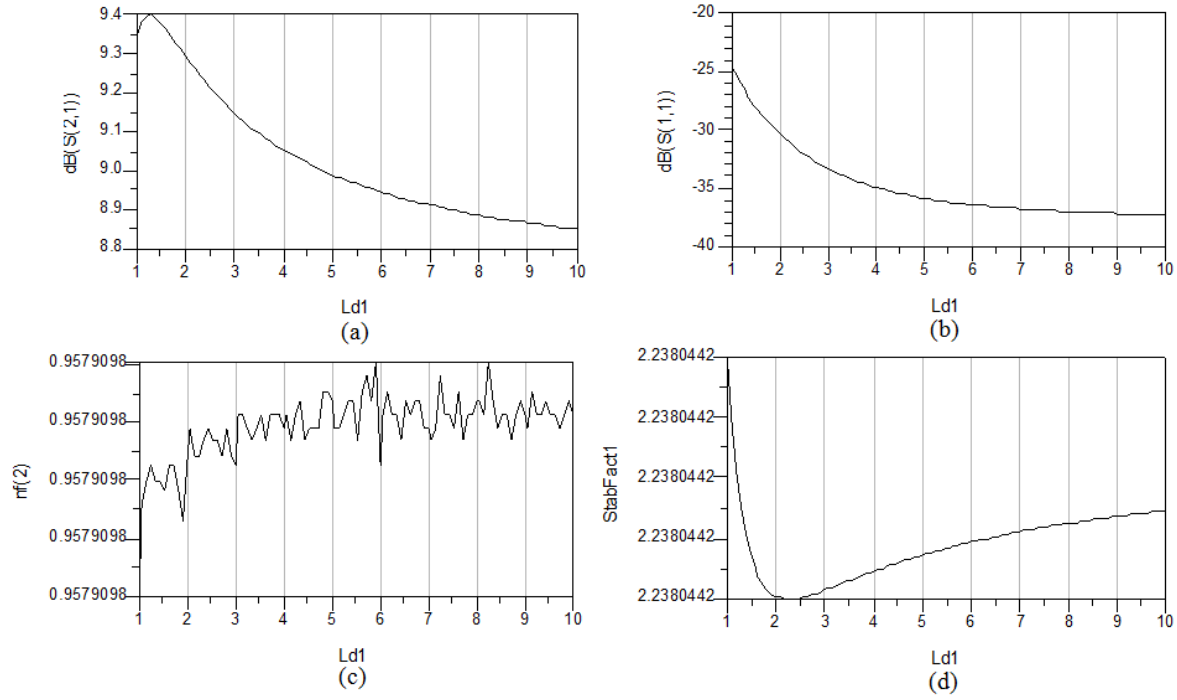
4. Variation with drain capacitor (C_d)(fF):



5. Variation with drain inductor (L_d)(nH):



6. Variation with drain inductor (L_{d1})(nH):



APPENDIX C

Look-Up Table:

Component	Percentage Change	$V_{test}(i)$ (mV)	MEMS Switch Matrix
Ideal	None	762	None
C_g	10% decrease	756	None
C_g	20% decrease	726	[0,0,0,1,1,0]
C_g	30% decrease	672	[0,0,0,1,1,0]
C_g	40% decrease	612	[0,0,0,1,1,0]
C_g	50% decrease	504	[0,0,0,1,1,0]
C_g	60% decrease	378	[0,0,0,1,1,0]
L_g	10% decrease	744	None
L_g	20% decrease	684	None
L_g	30% decrease	582	[0,0,1,0,0,0]
L_g	40% decrease	456	[0,0,1,0,0,0]
L_g	50% decrease	342	[0,0,1,0,0,0]
L_g	60% decrease	240	[0,0,1,0,0,0]
L_g	70% decrease	162	[0,0,1,0,0,0]
L_s	20% increase	690	None
L_s	30% increase	666	[1,1,0,0,0,0]
L_s	40% increase	642	[1,1,0,0,0,0]
L_s	50% increase	618	[1,1,0,0,0,0]
L_s	60% increase	600	[1,1,0,0,0,0]
L_d	10% decrease	858	None
L_d	20% decrease	906	None

L_d	30% decrease	1045	[0,0,0,0,0,1]
L_d	40% decrease	1268	[0,0,0,0,0,1]
L_d	50% decrease	1428	[0,0,0,0,0,1]
L_d	60% decrease	1684	[1,1,0,0,0,1]
C_d	10% decrease	612	None
C_d	20% decrease	596	None
C_d	30% decrease	568	[1,1,0,0,0,0]
C_d	40% decrease	536	[1,1,0,0,0,0]
C_d	30% increase	840	None
C_d	60% increase	958	[0,0,0,0,0,1]
C_g	10% increase	756	None
C_g	20% increase	744	None
C_g	30% increase	732	None
C_g	40% increase	714	None
L_{d1}	30% decrease	756	None
L_{d1}	40% decrease	768	None
L_{d1}	60% decrease	780	None
L_{d1}	30% increase	756	None
L_{d1}	40% increase	762	None
L_{d1}	50% increase	764	None
L_g	30% increase	684	[1,1,0,0,0,0]
L_g	40% increase	678	[1,1,0,0,0,0]
L_g	50% increase	636	[1,1,0,0,0,0]

L_g	60% increase	600	[1,1,0,0,0,0]
L_g	70% increase	564	[1,1,0,0,0,0]
C_g, L_g and L_s	20% decrease, 30% decrease and 70% increase	498	[1,1,1,1,1,0]
C_g, L_g and L_s	30% decrease, 40% decrease and 60% increase	492	[1,1,1,1,1,0]
C_g, L_g and L_s	40% decrease, 30% decrease and 80% increase	486	[1,1,1,1,1,0]
C_g, L_g and L_s	20% decrease, 30% decrease and 60% increase	468	[1,1,1,1,1,0]
C_g, L_g and L_s	40% decrease, 80% decrease and 60% increase	454	[1,1,1,1,1,0]
C_g, L_g and L_s	50% decrease, 20% decrease and 70% increase	478	[1,1,1,1,1,0]
C_g, L_g and L_s	30% decrease, 60% decrease and 40% increase	484	[1,1,1,1,1,0]
L_s and L_d	50% increase and 20% decrease	680	[1,1,0,0,0,0]
L_s and L_d	50% increase and 30% decrease	724	[1,1,0,0,0,0]
L_s and L_d	50% increase and	768	[1,1,0,0,0,0]

	40% decrease		
L_s and L_d	50% increase and 50% decrease	846	[1,1,0,0,0,1]
L_s and L_d	50% increase and 60% decrease	934	[1,1,0,0,0,1]
L_s and L_d	50% increase and 70% decrease	1026	[1,1,0,0,0,1]
C_g, L_g, L_s and L_d	20% decrease, 30% decrease, 60% increase and 40% decrease	420	[1,1,1,1,1,1]
C_g, L_g, L_s and L_d	30% decrease, 30% decrease, 60% increase and 40% decrease	384	[1,1,1,1,1,1]
C_g, L_g, L_s and L_d	30% decrease, 40% decrease, 60% increase and 30% decrease	368	[1,1,1,1,1,1]
C_g, L_g, L_s and L_d	40% decrease, 40% decrease, 80% increase and 20% decrease	294	[1,1,1,1,1,1]
C_g, L_g, L_s and L_d	40% decrease, 20% decrease, 80% increase and 20% decrease	246	[1,1,1,1,1,1]
C_g, L_g, L_s and L_d	30% decrease, 30%	138	[1,1,1,1,1,1]

	decrease, 60% increase and 40% decrease		
C_g, L_g, L_s and L_d	20% decrease, 30% decrease, 60% increase and 50% decrease	154	[1,1,1,1,1,1]
C_g, L_g, L_{d1}, L_s and L_d	20% decrease, 30% decrease, 60% increase, 70% increase and 40% decrease	196	[1,1,1,1,1,1]
C_g, L_g, L_{d1}, L_s and L_d	60% decrease, 70% decrease, 60% increase, 70% decrease and 60% decrease	180	[1,1,1,1,1,1]